

LV52205MU



ON Semiconductor®

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Bi-CMOS IC

LED Boost Driver with PWM Dimming

Overview

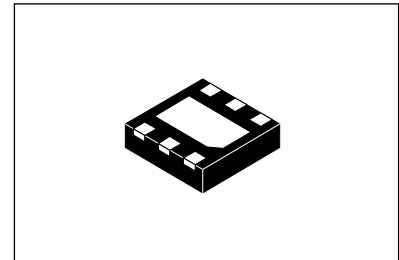
The LV52205MU is a high voltage boost driver for LED drive. LED current is set by the external resistor R1 and LED dimming can be done by changing FB voltage with PWM control.

Feature

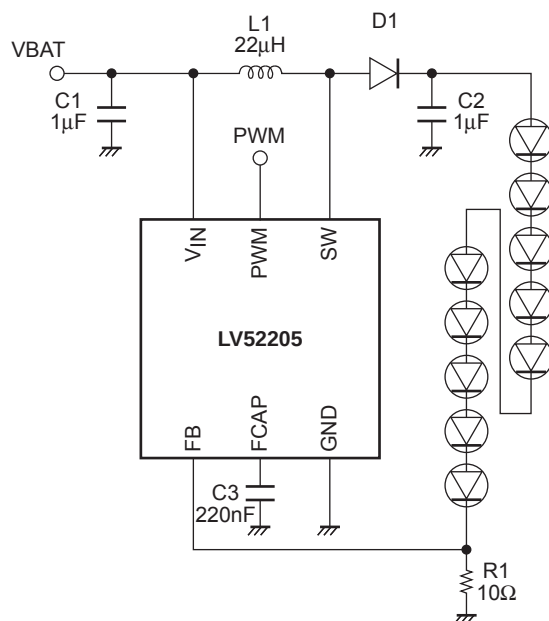
- Operating Voltage from 2.7V to 5.5V
- Integrated 42V MOSFET
- PWM dimming for Brightness Control
- 600kHz Switching Frequency

Typical Applications

- LED Display Backlight Control



UDFN6 2×2, 0.65P



ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$	V_{CC}	5.5	V
Maximum pin voltage1	$V1\text{ max}$	SW	42	V
Maximum pin voltage2	$V2\text{ max}$	Other pin	5.5	V
Allowable power dissipation	$Pd\text{ max}$	$T_a = 25^\circ\text{C}$ *1	2.05	W
Operating temperature	T_{opr}		-30 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^\circ\text{C}$

*1 Mounted on a specified board: 70mm×50mm×1.2mm (4 layer glass epoxy)

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommendation Operating Condition at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range1	$V_{CC\text{ op}}$	V_{CC}	2.7 to 5.5	V
PWM frequency	F_{pwm}		300 to 100k	Hz

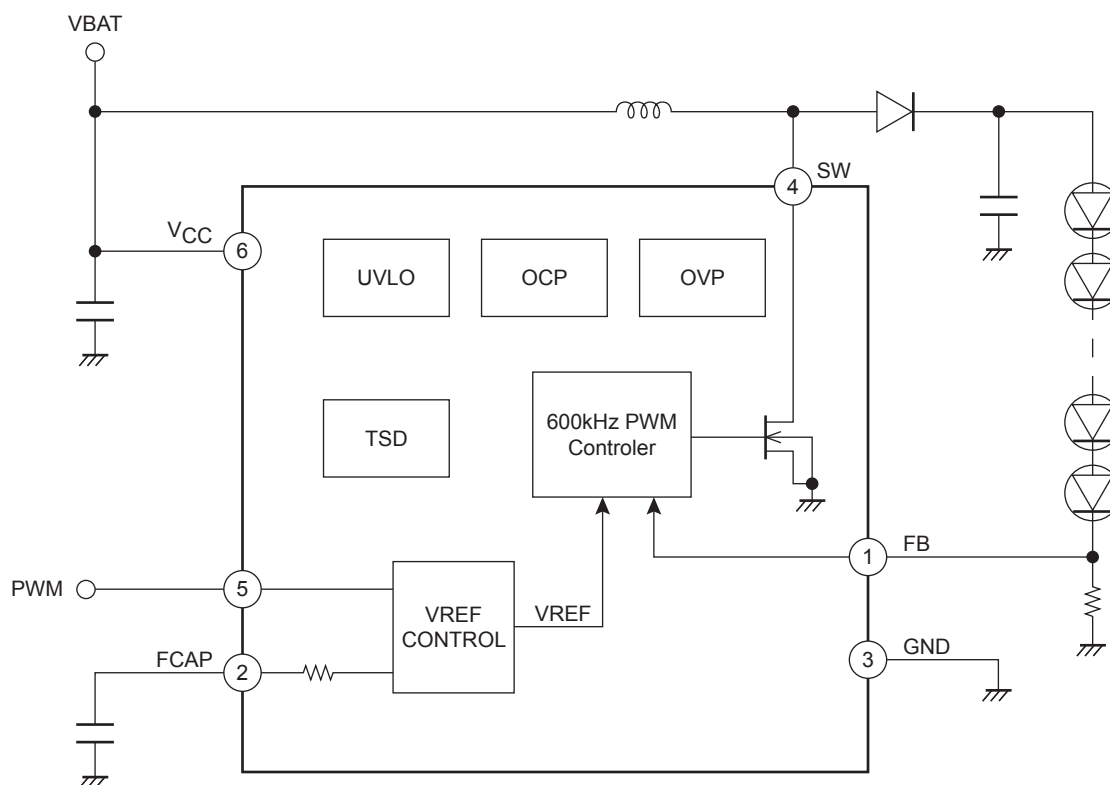
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics Analog block at $T_a = 25^\circ\text{C}$, $V_{CC} = 3.6\text{V}$, unless otherwise specified

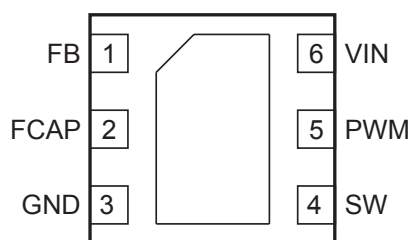
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby current dissipation	I_{CC1}	SHUTDOWN		0	5	μA
DC/DC current dissipation	I_{CC2}	$V_{OUT} = 30\text{V}$, $I_{LED} = 20\text{mA}$			1	mA
FB voltage	V_{fb}	PWM duty 100%	0.19	0.2	0.21	V
FB pin leak current	I_{fb}				1	μA
OVP voltage	V_{ovp}	SW	40	41	42	V
SWOUT ON resistance	R_{on}	$I_L = 100\text{mA}$		700		$\text{m}\Omega$
NMOS switch current limit	I_{LIM}	$V_{fb} = 200\text{mV}$		0.7		A
OSC frequency	F_{osc}			600		kHz
High level input voltage	V_{INH}	PWM	1.5		V_{CC}	V
Low level input voltage	V_{INL}	PWM	0		0.4	V
Under voltage lockout	V_{uvlo}	V_{IN} falling		2.2		V
PWM setup time from shutdown	T_{on}		20			μs
PWM low time to shutdown	T_{off}		8.9			ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Block Diagram



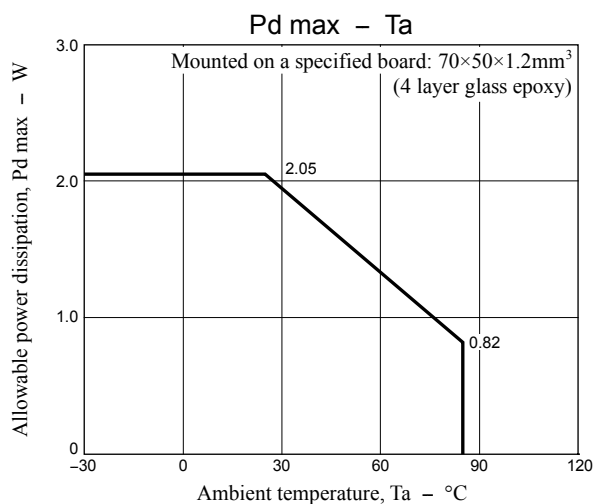
Pin Connections



Top view

Pin Function

PIN #	Pin Name	Description
1	FB	Feedback pin.
2	FCAP	Filtering capacitor terminal for PWM signal.
3	GND	Ground
4	SW	Switch pin. Drain of the internal power FET.
5	PWM	PWM dimming input (active High).
6	V _{CC}	Supply voltage.
	Expose-pad	Connect to GND on PCB.



LED Current Setting

LED current is set by an external resistor connected between the FB pin and ground.

$$I_{LED} = V_{FB}/R_{FB}.$$

The V_{FB} can be controlled by PWM signal. PWM input is converted into a near DC current by the internal resistor R that was equivalent to 60kΩ (±10%) and the external capacitor C_{FCAP} as a low pass filter with a cut-off frequency $f_c = 1/2\pi RC_{FCAP}$. The V_{FB} can be adjusted by altering the duty cycle of the PWM signal (See Fig.1).

$$V_{FB} = 200 \text{ (mV)} \times \text{PWM Duty (\%)}$$

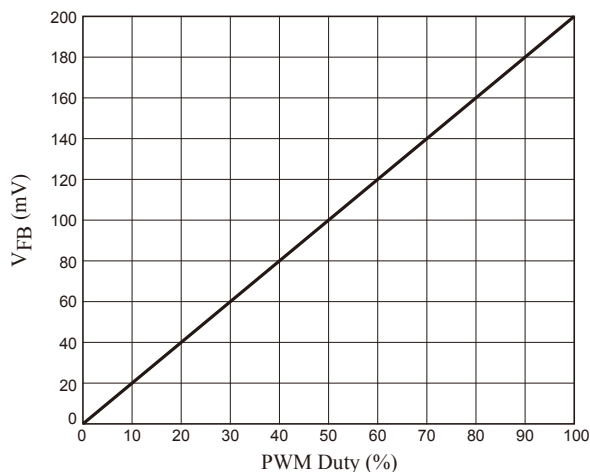


Fig1. V_{FB} vs. PWM Duty

PWM Control

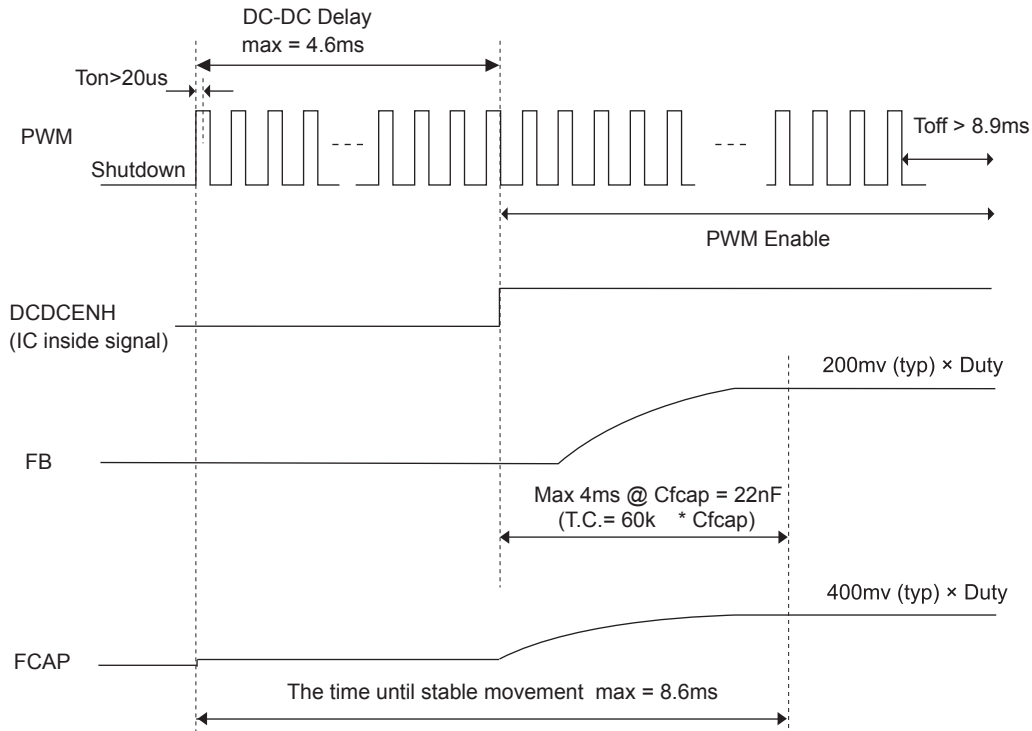


Fig2. Timing Diagram in PWM signal

Open LED Protection

If SW terminal voltage exceeds a threshold V_{ovp} (41V typ) for 8 cycles, boost converter enters shutdown mode. In order to restart the IC, PWM setup signal is required again.

Over Current Protection

Current limit value for built-in power MOS is around 0.7A. The power MOS is turned off for each switching cycle when peak current through it exceeds the limit value.

Under Voltage Lock Out (UVLO)

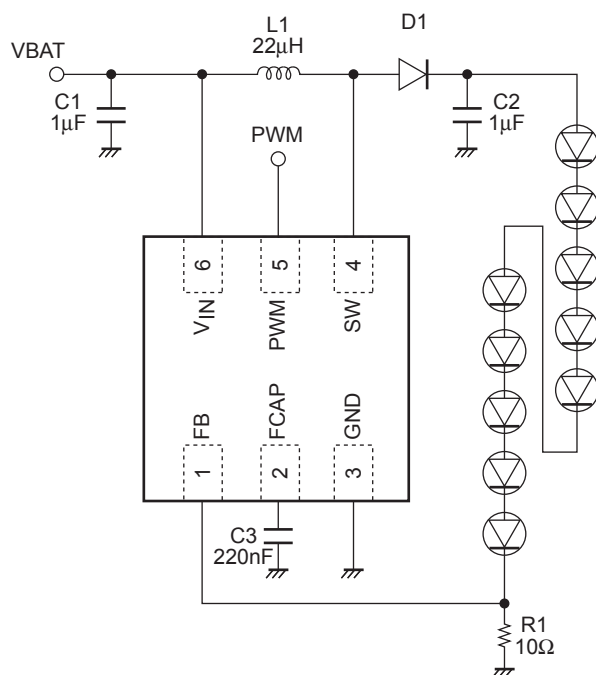
UVLO operation works when V_{IN} terminal voltage is below 2.2V.

Thermal Shutdown

When chip temperature is too high, boost converter is stopped.

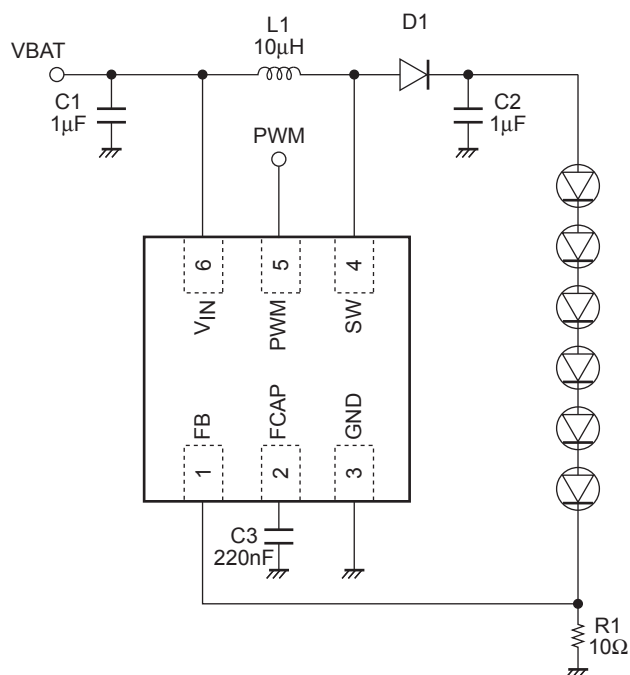
Application Circuit Diagram

10LEDs



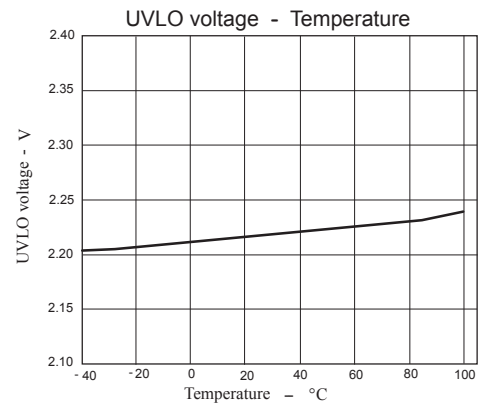
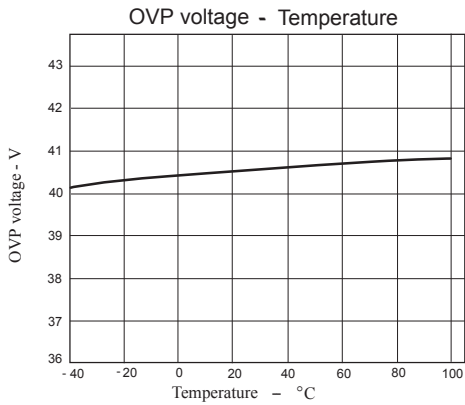
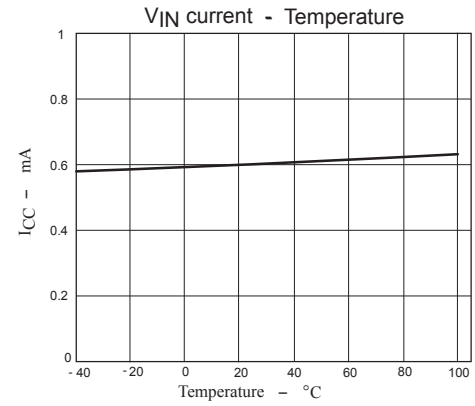
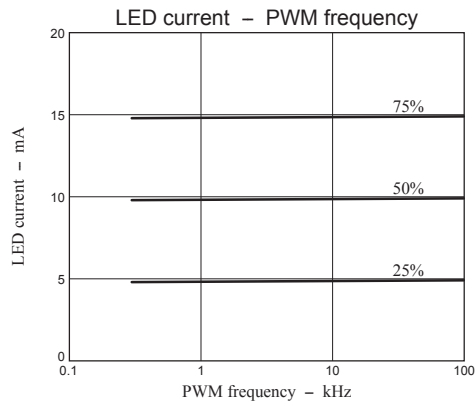
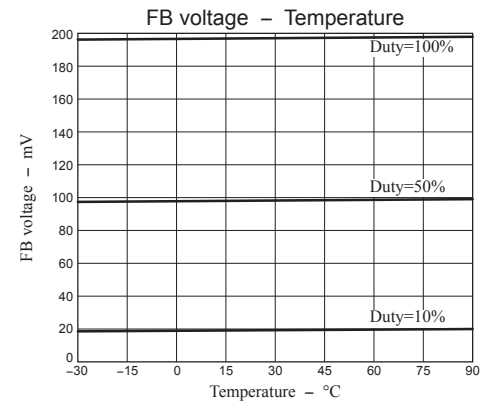
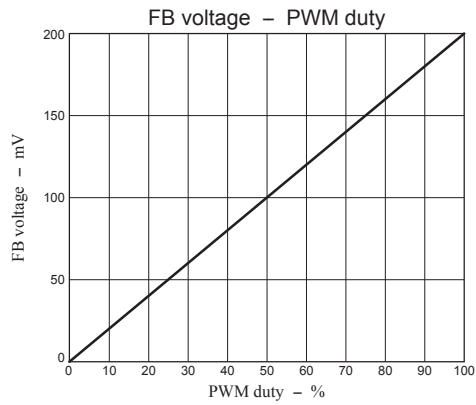
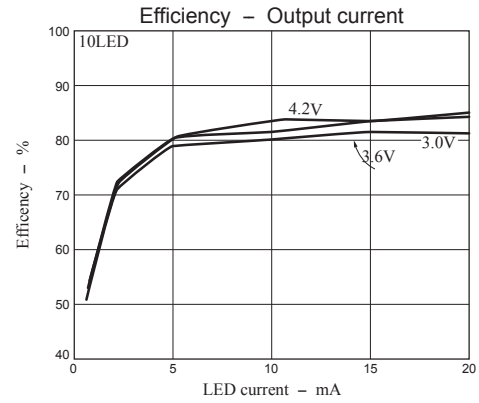
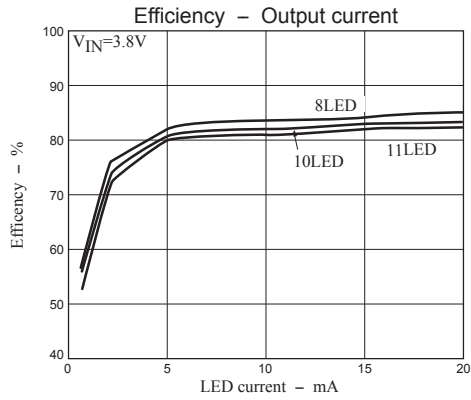
L1: VLS3012T-220M49 (TDK), VLF504015MT-220M (TDK)
 D1: MBR0540T1 (ONsemi), NSR05F40 (ONsemi)
 C2: GRM21BR71H105K (Murata), C1608X5R1H105K (TDK)

6LEDs



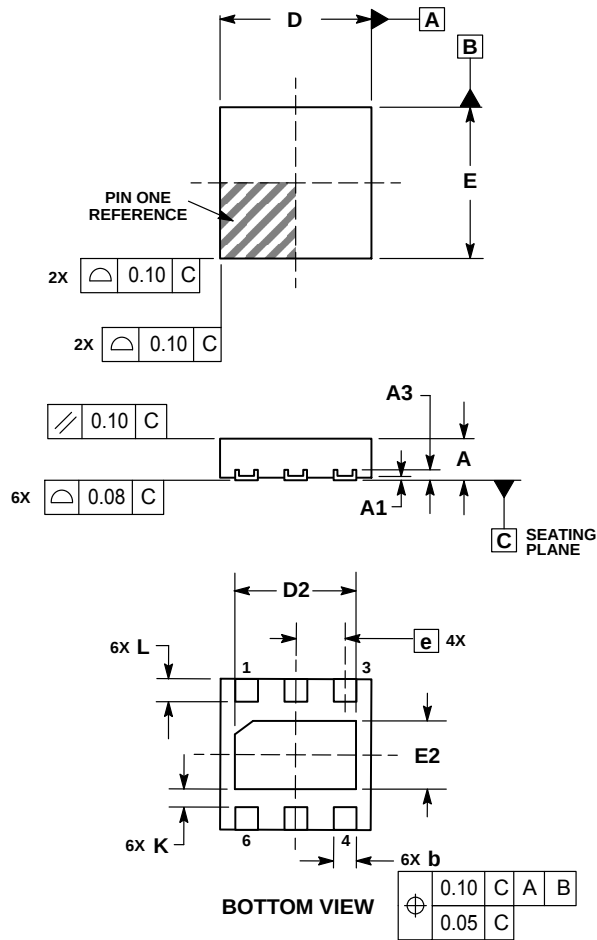
L1: VLS3012T-100M72 (TDK), VLF302512M-100M (TDK)
 D1: MBR0540T1 (ONsemi), NSR05F40 (ONsemi)
 C2: GRM21BR71H105K (Murata), C1608X5R1H105K (TDK)

Typical Characteristics ($V_{IN} = 3.6V$, $L = 22\mu H$, $T = 25^\circ C$, unless otherwise specified)



PACKAGE DIMENSIONS

UDFN6 2x2, 0.65P
CASE 517AB

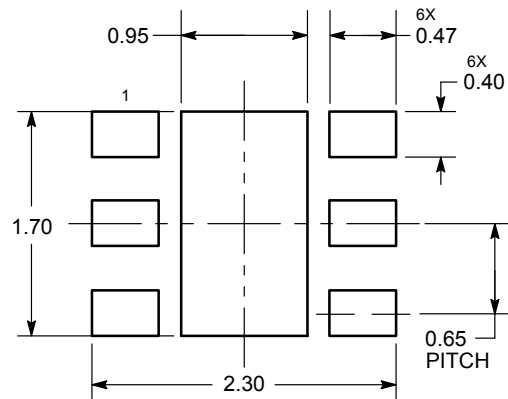


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.25	0.35
D	2.00	BSC
D2	1.50	1.70
E	2.00	BSC
E2	0.80	1.00
e	0.65	BSC
K	0.20	---
L	0.25	0.35

SOLDERING FOOTPRINT*

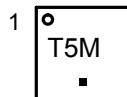


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

LV52205MU is as follows.

MARKING DIAGRAM



- T5 = Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

2.TAPE STRENGTH

2 - 1 .Tensile strength of the carrier tape : Min.10N

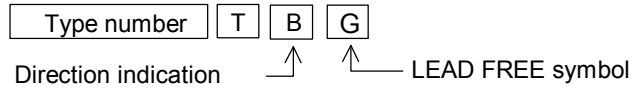
2 - 2 .Peel strength of the top cover tape

(a)Peel angle : 165° to 180° relative to the tape adhesive surface

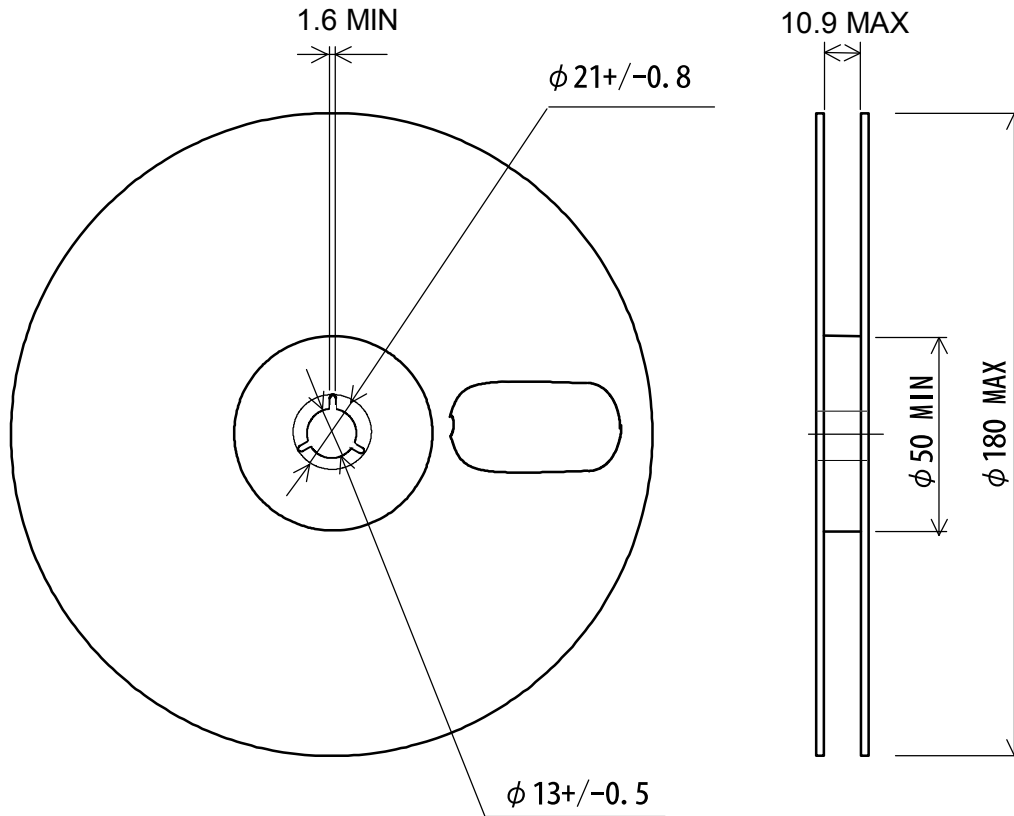
(b)Peel rate : 300mm / minute

(c)Peel of strength : 0.1N to 1.0N

3.PARTS No. ON BAR CODE LABEL



4.REEL DIMENSIONS

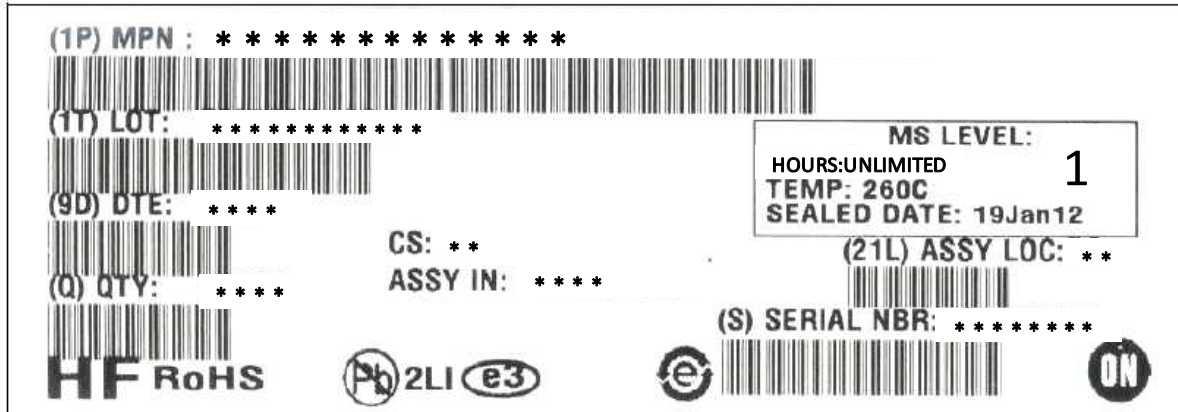


TYPE:P-RRM-08B

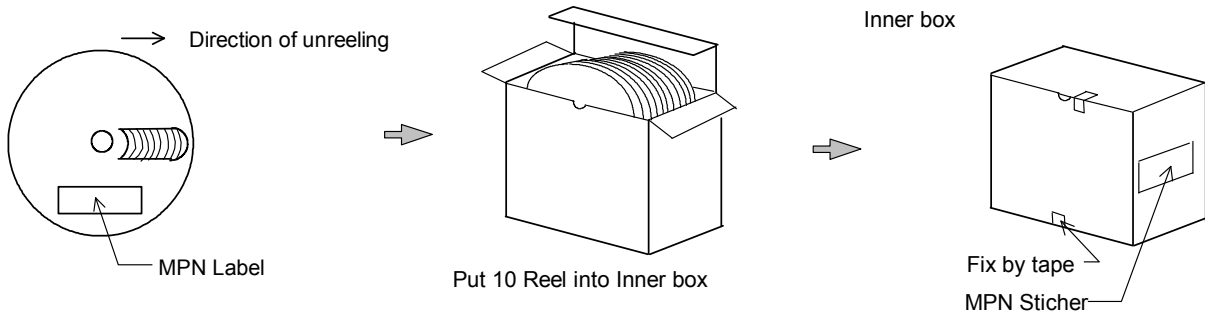
UNIT:mm

Carrier tape type number	SANYO Package code	Maximum number of ICs contained (pcs.)		Packing form
		Reel	Inner box	Inner box. B50766P001
N22986D001	UDFN6(2.0*2.0)	3,000	30,000	10 Reels contained Dimensions:mm 190 × 136 × 186

MPN Label



Packing Method



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV52205MUTBG	UDFN6 (2x2) (Pb-Free)	3000 / Tape & Reel

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