Telink

Telink Semiconductor

B80 Hardware Design Guideline

2023-10

Scope

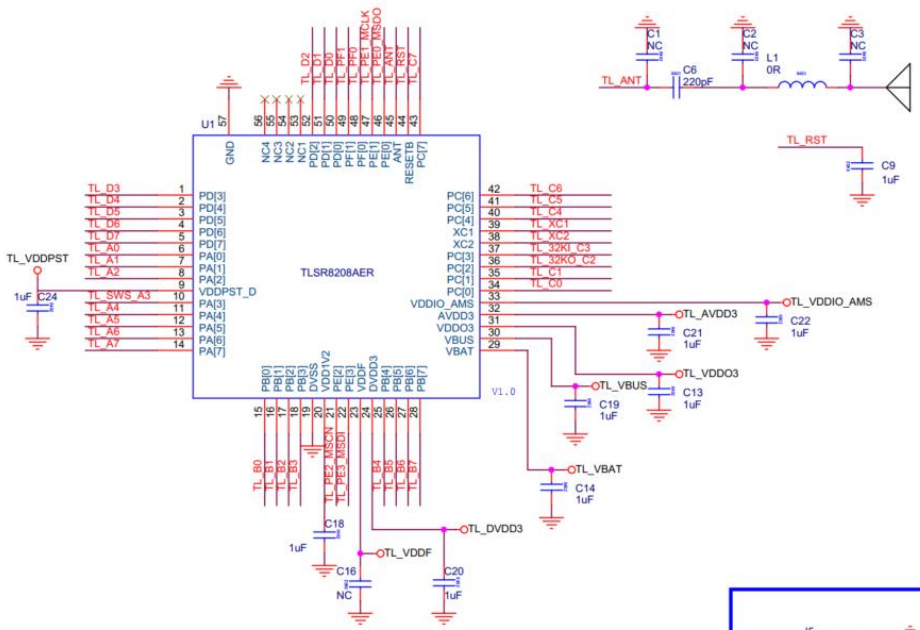
- Chip`s datasheet is the basic reference file of hardware design. This document will go through datasheet with hardware engineer and supplement some details. It will speed up projects after reading the document.
- Considering that the chip`s datasheet will be continuously updated, if there is any difference between this document and the chip`s datasheet, please refer to the latest version of the chip specifications.
- The version and link of the chip`s datasheet mentioned in this document are as follows:
  - DS_TLSR8208-E_Datasheet for Telink Bluetooth LE SoC TLSR8208
    - http://wiki.telink-semi.cn/wiki/chip-series/TLSR8208-Series/
    - TLSR8208A is taken as an example to describe. And the content mentioned in the file applies to the B80 chipset serials.

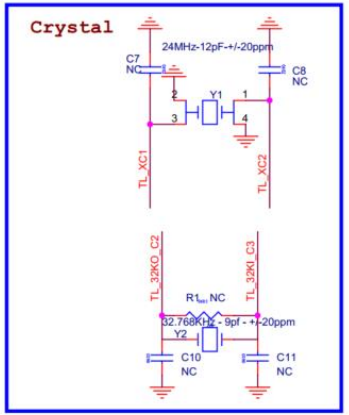
Schematic Design Guideline

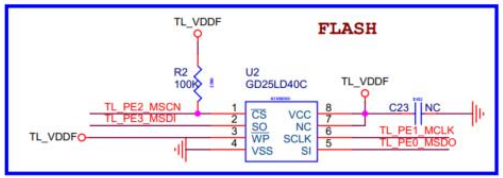
Reference Schematic

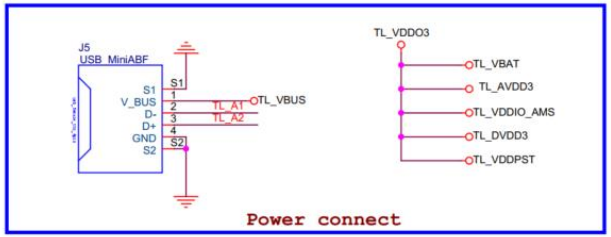
- Reference Schematic:
  - Refer to chapter 14 (reference design).
  - TLSR8208A`s reference design are listed here.
    - Schematic and BOM are listed together.
  - The schematic is the design of minimum core system
    - Easy to copy into other designs.
    - Easy to count the cost at the stage of design-in.

Power supply : USB

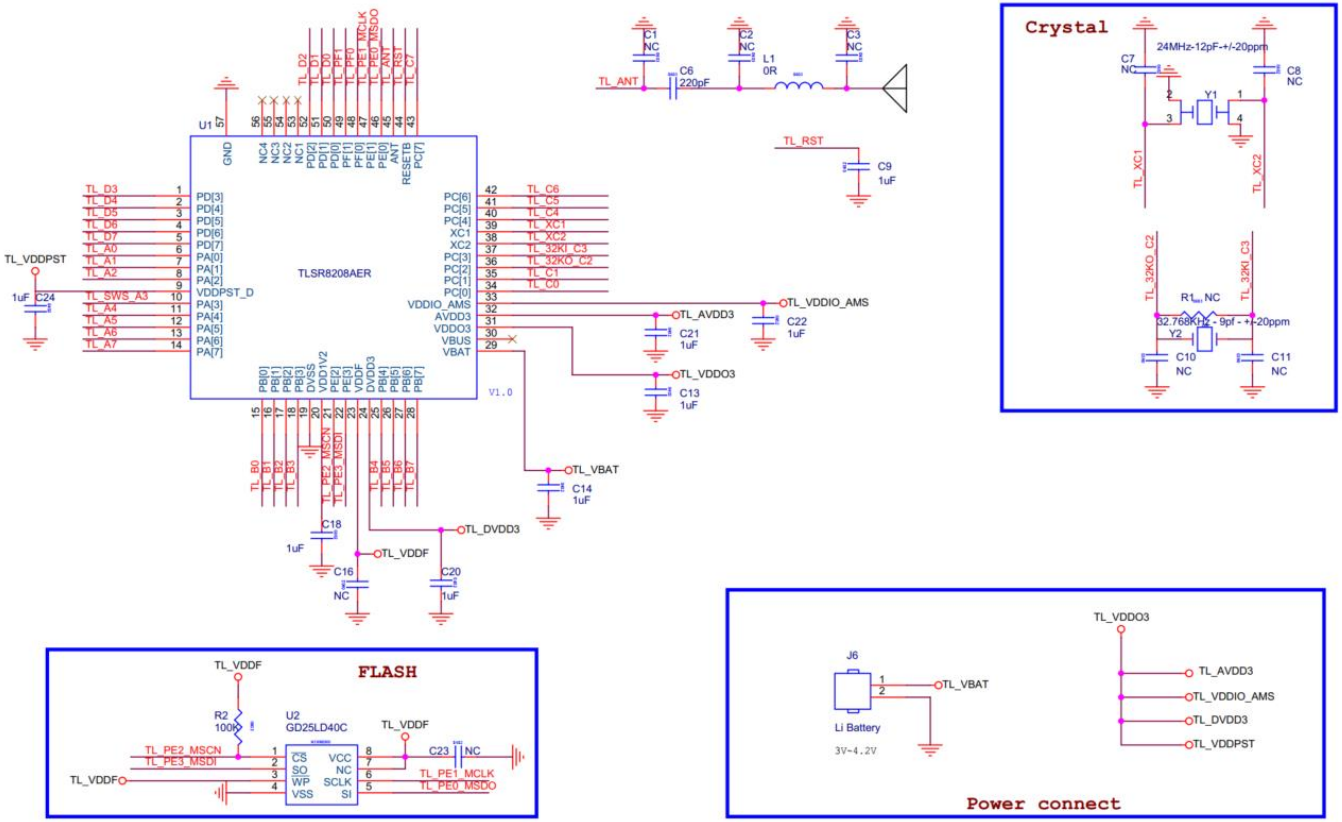




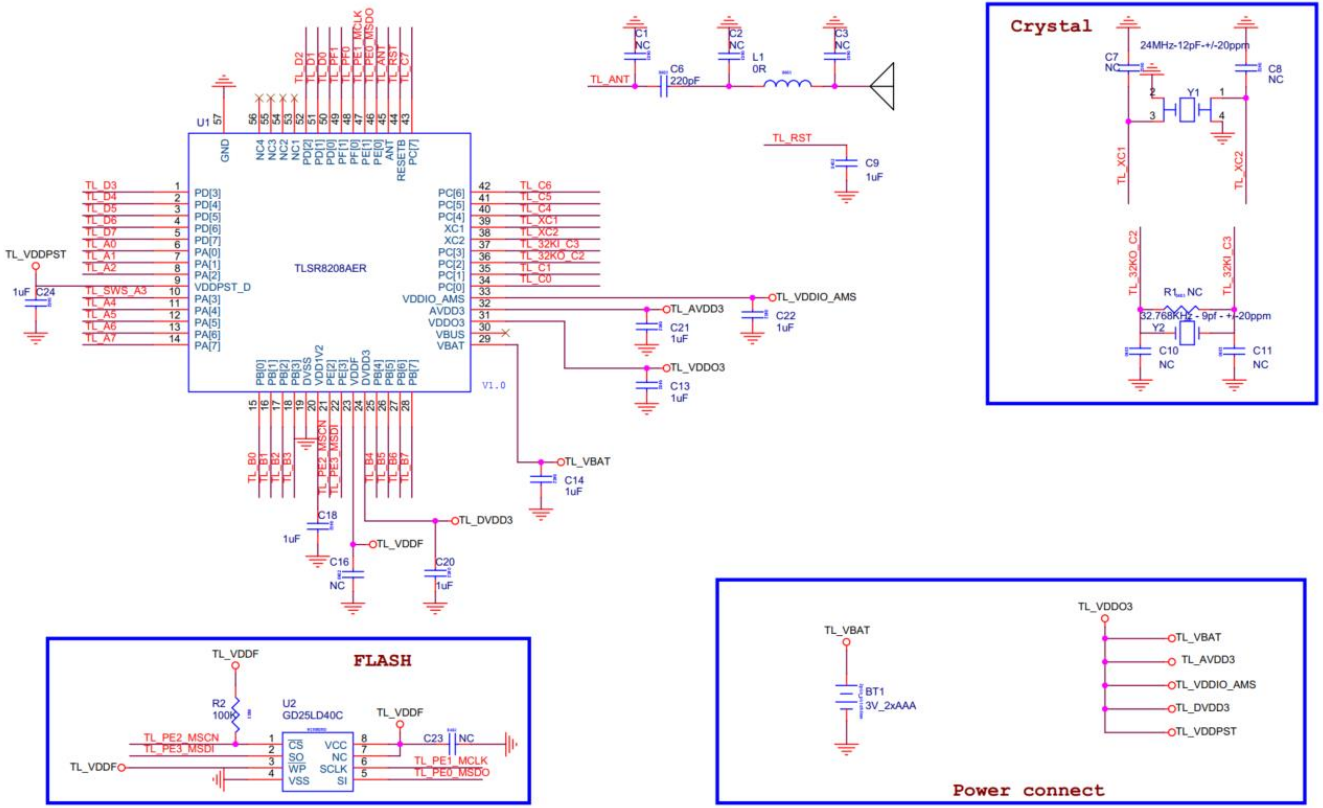




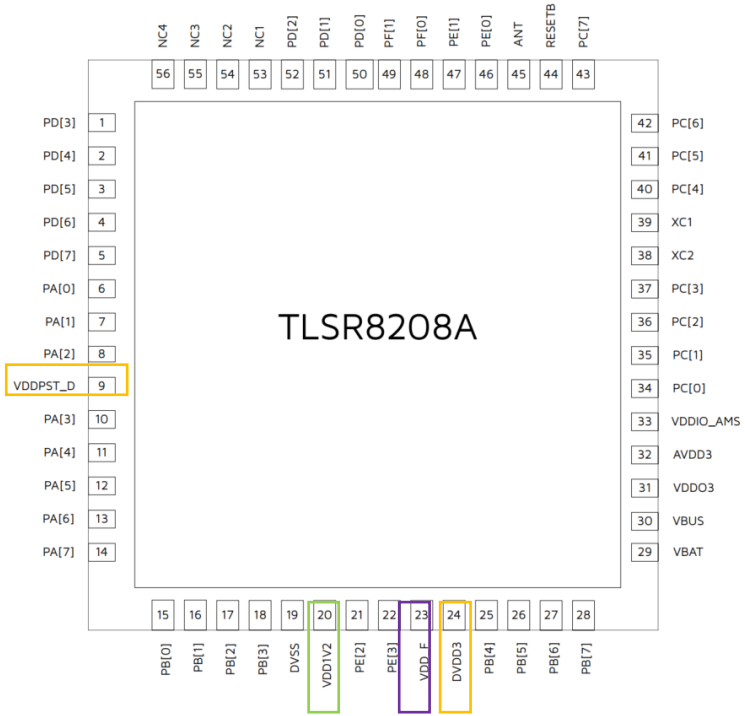
Power supply : Li battery



Power supply : 2xAAA battery

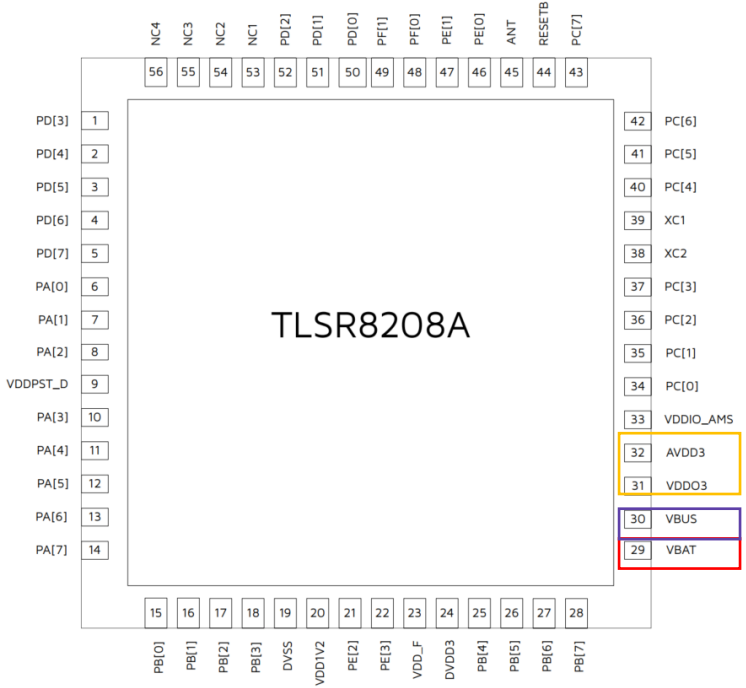


Pin layout - Power Supplies: Part A



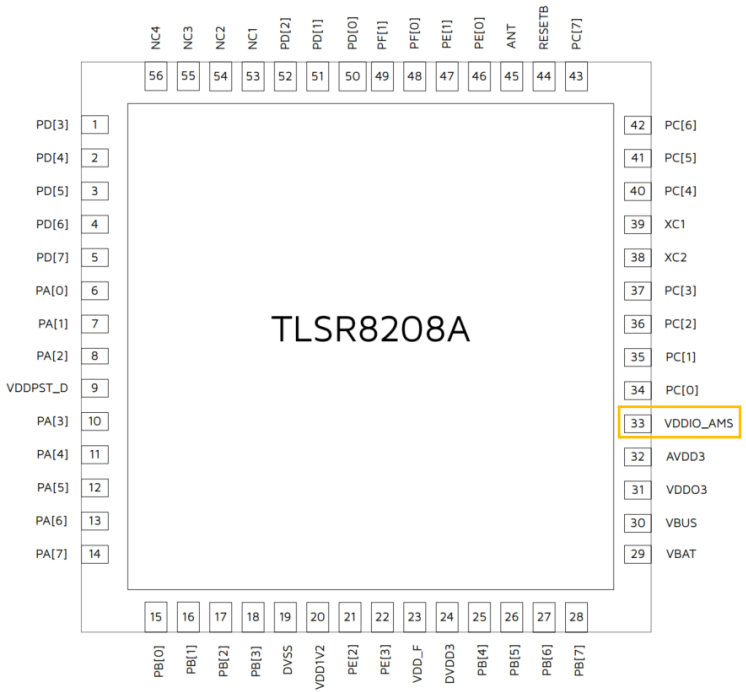
- PIN9(VDDPST_D)
  - Only packaged out on TLSR8208A which is used by ESD.
  - A decoupling capacitor, 1uF, is needed.
- PIN20(VDD1V2)
  - It is used by Digital core.
  - A decoupling capacitor, 1uF, is needed.
- PIN23(VDD_F)
  - It is used by external flash.
  - The decoupling capacitor is not needed because the capless LDO is included inside.
- PIN24(DVDD3)
  - It is used by digital LDO and need to connected with VDDO3
  - A decoupling capacitor, 1uF, is needed.

Pin layout - Power Supplies: Part B



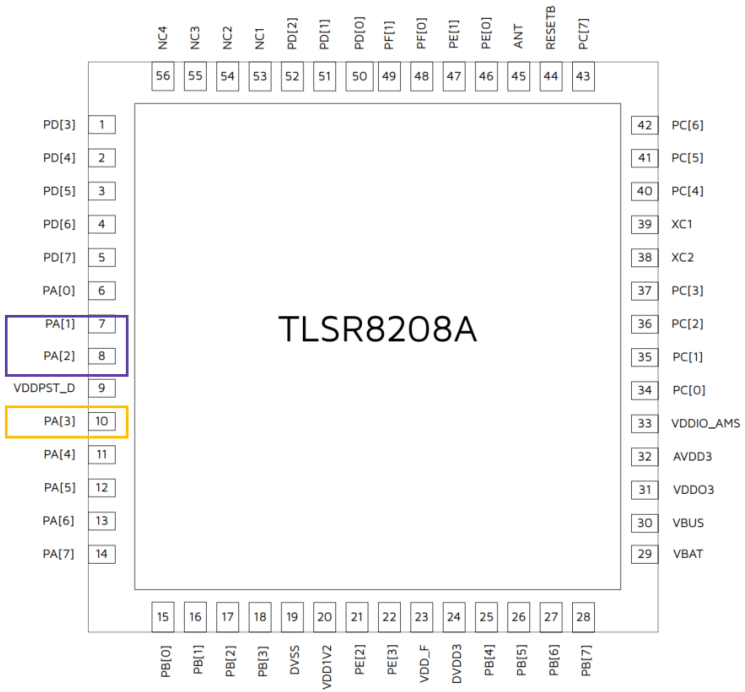
- PIN29(VBAT)
  - Battery positive terminal. A decoupling capacitor, 1uF, is needed.
- PIN30(VBUS)
  - 5V VBUS power supply of USB.
    - In this case, VDDO3,AVDD3,VDDIO_AMS,DVDD3,VDDPST,VBAT need connect together
  - A decoupling capacitor, 1uF, is needed.
- PIN31(VDDO3)
  - Power supply output as Li/USB application.
  - A decoupling capacitor, 1uF, is needed.
- PIN32(AVDD3)
  - It is used for analog modules, connected with VDDO3
  - A decoupling capacitor, 1uF, is needed.

Pin layout - Power Supplies: Part C



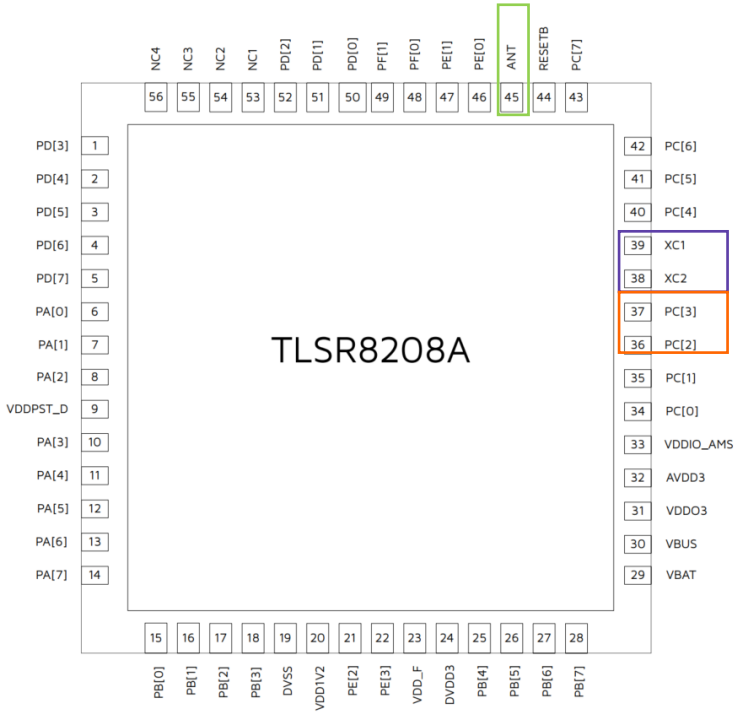
- PIN33(VDDIO_AMS)
  - It is used for ADC and IO, connected with VDDO3
  - A decoupling capacitor, 1uF, is needed.

Pin layout – Debug Port



- PIN10(PA3/SWS)
  - Download Pin and must be connected to a test point which is used to download FW.
- PIN1(PA1_DM)/PIN2(PA2_DP)
  - It is USB interface.
  - Recommend to connect to test points for capturing log when FW works.

Pin layout – RF Part: Part A

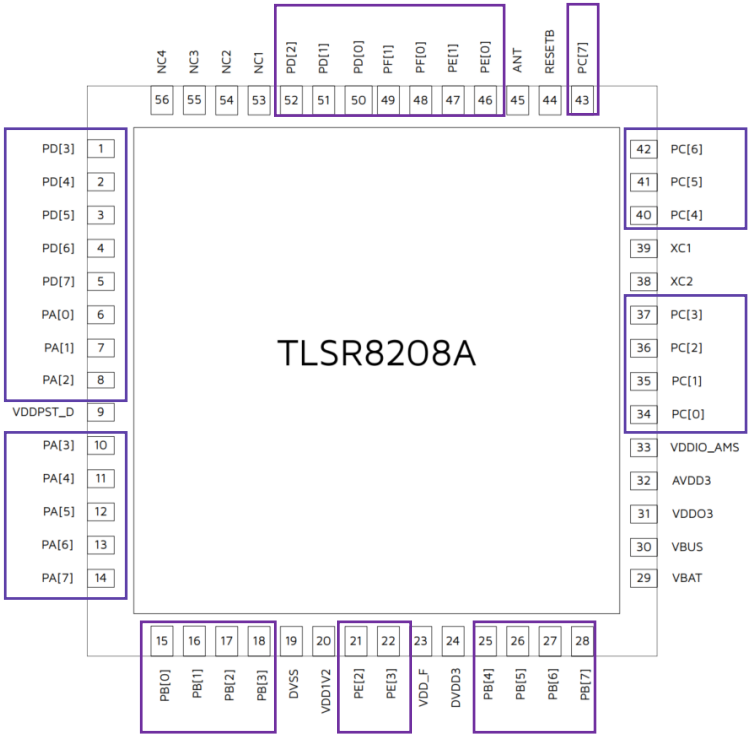


- RF Port
  - PIN45(ANT) is RF port.
  - A 4th-order LC filter is recommend to use for certification. The detail will be introduced in the next page.
- 24Mhz Crystal
  - PIN38(XC2), PIN39(XC1) connect 24Mhz crystal.
  - Usually recommended specification: 24Mhz – 12pF - +/-20ppm
    - Sometimes try different kind of 24Mhz crystal with different load capacitor, such as 10pf, 15pf because of different PCB layout to get lower frequency offset.
    - For some BLE projects, it is recommended to use the same type of crystal for TX/RX and to verify and calibrate the frequency bias according to different PCBs.
- 32.768K crystal
  - PC2 and PC3 can be used to connect external 32.768Khz crystal.

Pin layout – RF Part: Part B

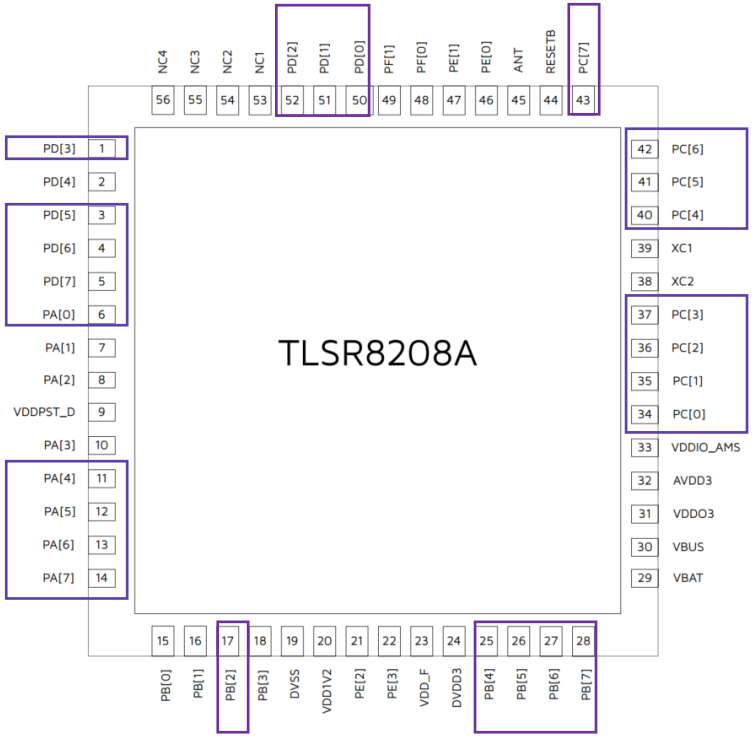
- A Π type filter is used for matching to pass certification, the values of which are flexibly adjustable corresponding to layout.
  - A 4th-order LC filter can be more easy to pass certification
- Firstly, use VNA (Vector Network Analyzer) to do RX matching.
  - Customers must power on DUT, and use EMI tool to configure chip into RX mode, then tune RX matching.
- After RX test is finished, SA (Spectrum Analyzer) should be used to check TX harmonic.
  - If harmonics do not meet the requirements, re-do RX matching. Use the VNA to adjust component value to meet the impedance matching requirements, and then check TX harmonic again.
- It is recommend to mount a shielding box on PCBA for certification if customer can afford the cost. It is easy to pass certification and save time.
- TLSR8208A development board has passed FCC certification.
  - FCCID: OEOTLSR8208ADK56D

Pin layout – GPIO : Part A



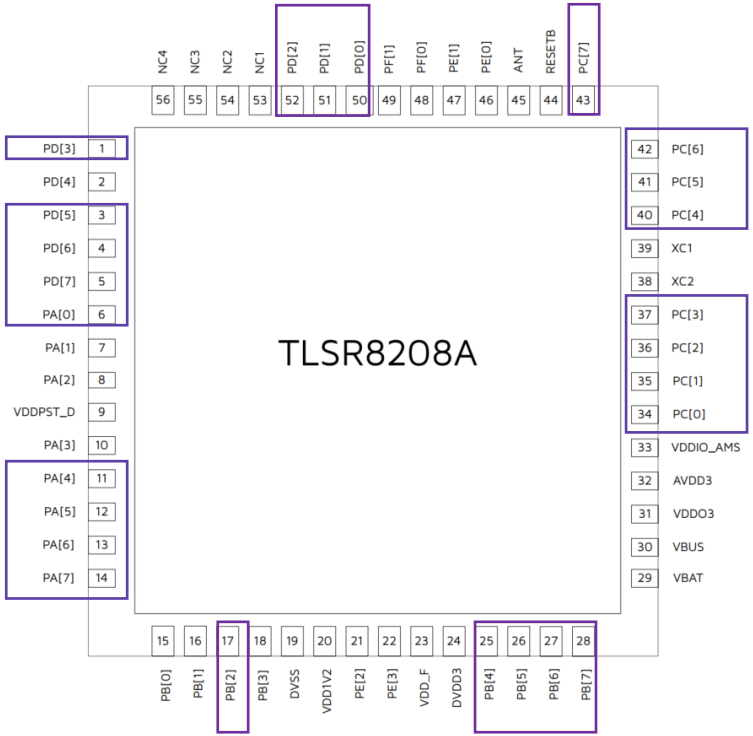
- Refer to chapter 7.1.
- All GPIO pins have configurable pull-up resistor and pull-down resistor.
  - Pull-up resistor: 10K/1M
  - Pull-down resistor: 100K
- All GPIO pins(except below) can be independently configured as high-level/low-level wakeup source.
  - The initial status of PB[0], PB[1], PB[3], PD[4], PF[0] and PF[1] at power up or after sleep wake-up is SPI function, so these pins are not recommend to use as wakeup source
- Two kinds of driving strength
  - PA[0,4:7], PC[0:7], PD[0:7], PE[0:3], and PF[0:1]: maximum = 4 mA ,minimum = 2 mA
  - PA[1:3], and PB[0:7]: maximum = 8 mA , minimum = 4 mA

Pin layout – GPIO : Part B



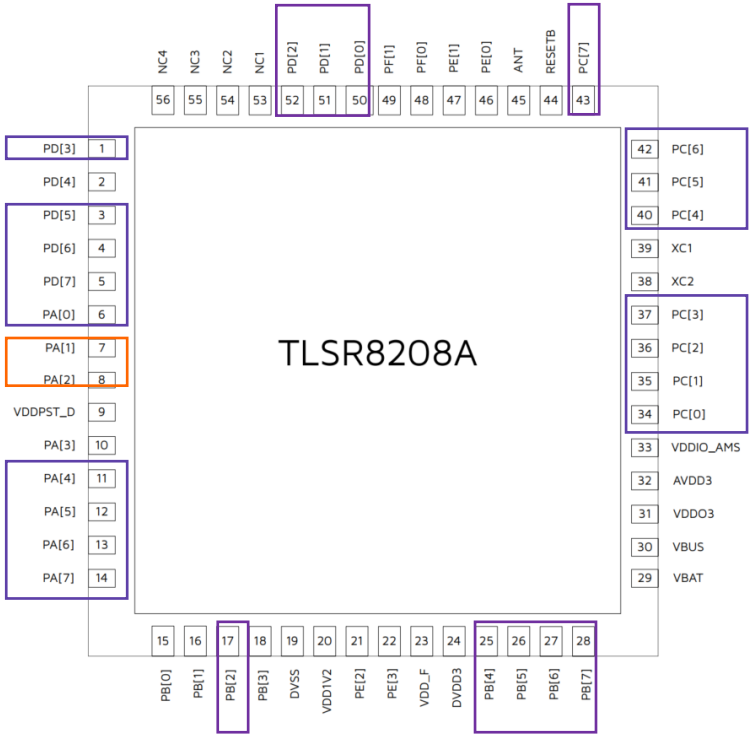
- Support all functions
  - PA0,PA4~PA7, PB2,PB4~PB7, PC0~PC7, PD0~PD3,PD5~PD7
  - "All functions" include 32 functions: WIFI_DENY_I, BLE_STATUS, BLE_ACTIVITY, SPI_CN_IO, SPI_CK_IO, SPI_MOSI_IO,SPI_MISO_IO, SWM_IO, TX_CYC2PA, RX_CYC2LNA, ANT_SEL2, ANT_SEL1, ANT_SEL0, UART_RTX_IO, CLK_7816,I2C_SDA_IO, I2C_SCL_IO, UART_RX_I, UART_TX, UART_RTS, UART_CTS_I, PWM5_N, PWM4_N, PWM3_N, PWM2_N,PWM1_N, PWM0_N, PWM5, PWM4, PWM3, PWM1, PWM0

Pin layout – PWM



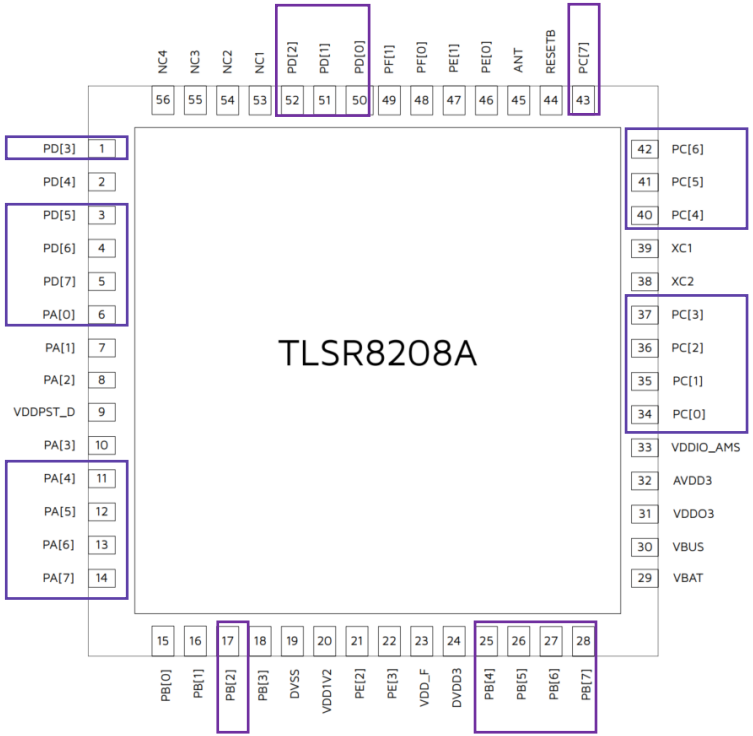
- Refer to chapter 8.
- Up to 6 PWM output channels. Each PWMx (x=0~5) has its corresponding inverted output pins, PWMx_N pin.
- PWM0 supports five modes, including Continuous mode (normal mode, default), Counting mode, IR mode, IR FIFO mode, IR DMA FIFO mode. PWM1~PWM5 only support Continuous mode.
- PWM0 pins, including PWM0 and PWM0N, can be used as IR driver pin.
- All the following pins can be used as PWMx (0~5) or PWMx_N (0~5)
  - PA0,PA4~PA7, PB2,PB4~PB7, PC0~PC7, PD0~PD3,PD5~PD7

Pin layout – UART



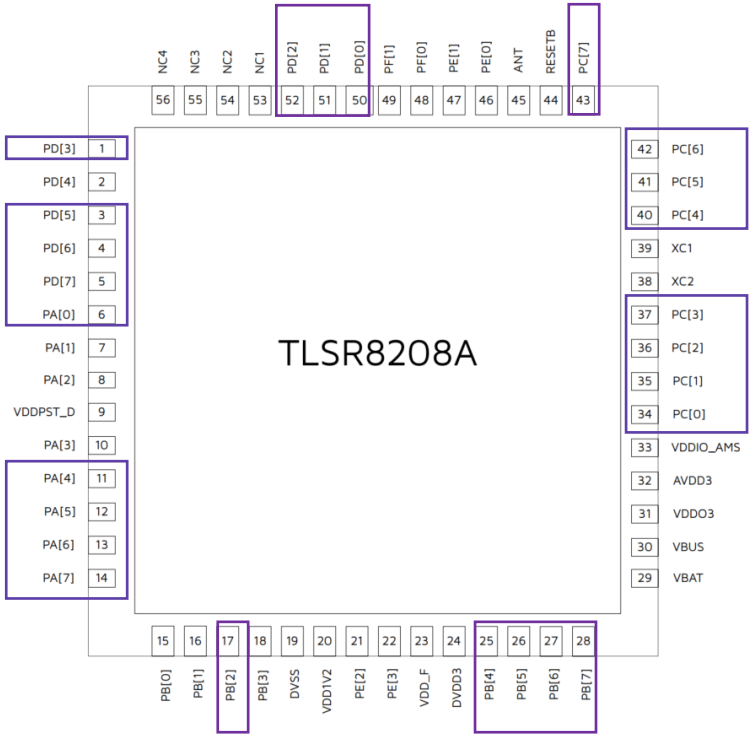
- Refer to chapter 7.5.
- Supports general UART interface and 7816 UART interface.
- All the following pins can be used as UTX/URX/CTS/RTS
  - PA0,PA4~PA7, PB2,PB4~PB7, PC0~PC7, PD0~PD3,PD5~PD7
- PA1:URX, PA2:UTX

Pin layout – I2C



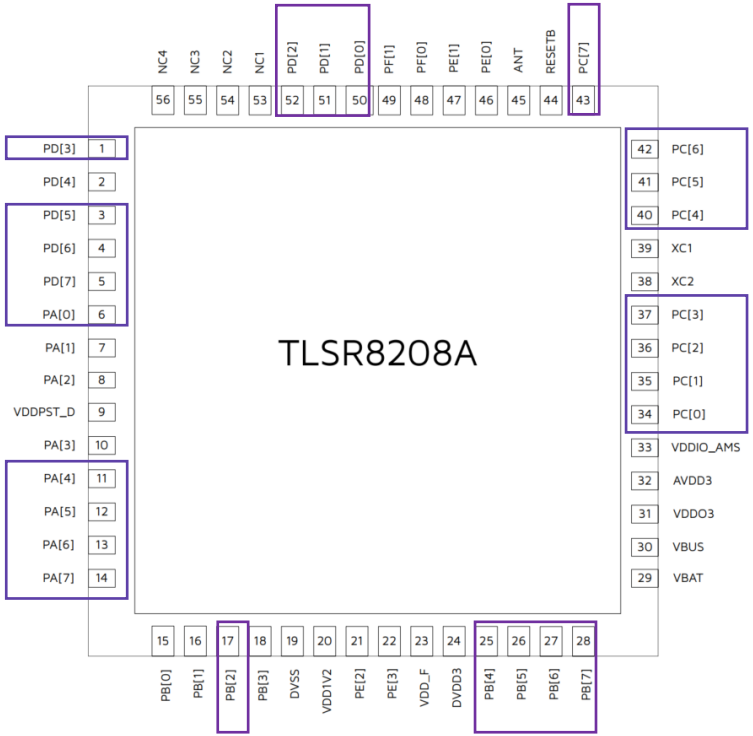
- Refer to chapter 7.3.
- Any SCK and SDA can be used in combination
- Support master and slave mode
- All the following pins can be used as SCK/SDA
  - PA0,PA4~PA7, PB2,PB4~PB7, PC0~PC7, PD0~PD3,PD5~PD7
- For supporting up to 400K bit/s, external pull-up resistors must be added.

Pin layout – SPI : Part A



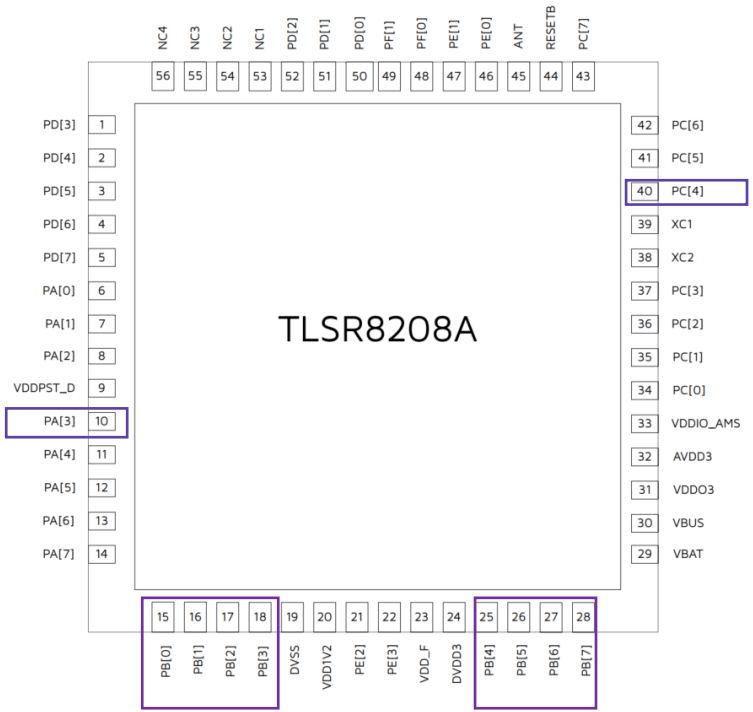
- Refer to chapter 7.4.
- The features of SPI are listed as following:
  - Supports SPI Master/Slave mode
  - Supports Dual line, Quad line and 3 line I/O SPI interface
  - Supports LCD driving with SPI ports
  - Supports DMA transmission
- All the following pins can be used as CK/CN/ MOSI/MISO
  - PA0,PA4~PA7, PB2,PB4~PB7, PC0~PC7, PD0~PD3,PD5~PD7

I2C and SPI Usage



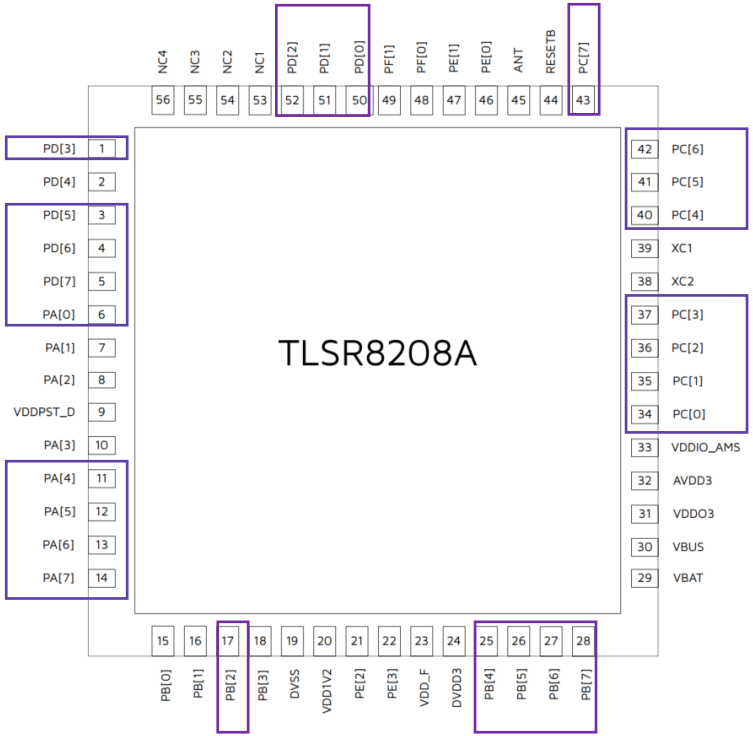
- Refer to chapter 7.3.5.
- I2C hardware and SPI hardware modules in the chip share part of the hardware, as a result, when both hardware interfaces are used, the restrictions listed within this section need to be taken into consideration.
- I2C and SPI hardware cannot be used as Slave at the same time.
- The other cases are supported, including:
  - I2C Slave and SPI Master can be used at the same time.
  - I2C Master and SPI Slave can be used at the same time.
  - I2C and SPI can be used as Master at the same time.

Pin layout – ADC



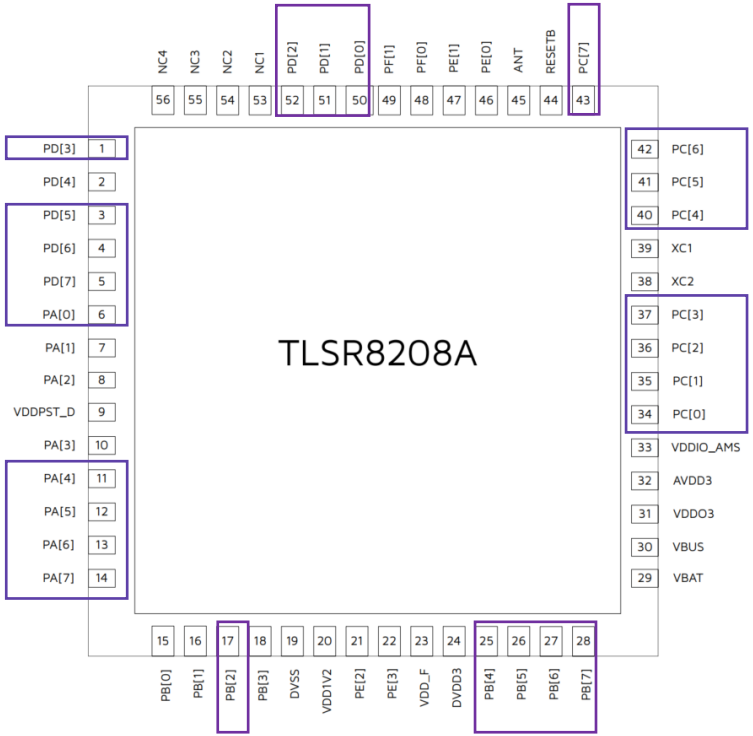
- Refer to chapter 11.
- Supports up to 10 detect pins, including PB0~PB7, PA3, PC4.
  - If using ADC pin for voltage detection , input voltage cannot exceed VDDIO+200mv.
- If the system is powered by two AAA batteries or lithium battery, the system can directly detect the voltage of VBAT.

Pin layout – RF front-end & Antenna Select Pins



- External RF front-end pins
  - TXCYC is used to control the PA (Power Amplifier) of external RF Front-end
  - RXCYC is used to control the LNA of external RF Front-end
  - All the following pins can be used as TXCYC/ RXCYC
    - PA0,PA4~PA7, PB2,PB4~PB7, PC0~PC7, PD0~PD3,PD5~PD7
- Antenna Select Pins:
  - One groups of SEL<0:2> are used to select one of up to eight external antennas. The selected antenna channel is connected to the RF_IO pin.
  - All the following pins can be used as ATSEL<0:2>
    - PA0,PA4~PA7, PB2,PB4~PB7, PC0~PC7, PD0~PD3,PD5~PD7

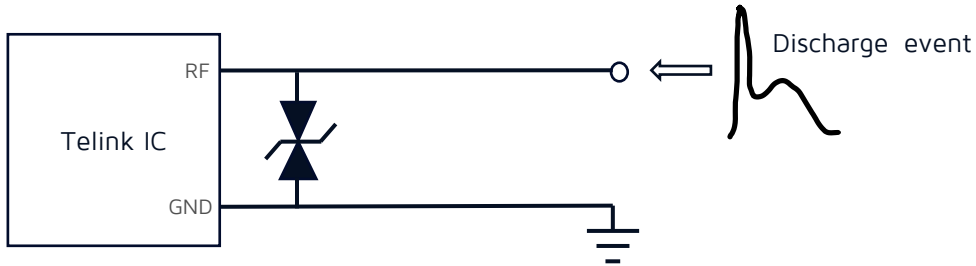
Pin layout –Quadrature Decoder



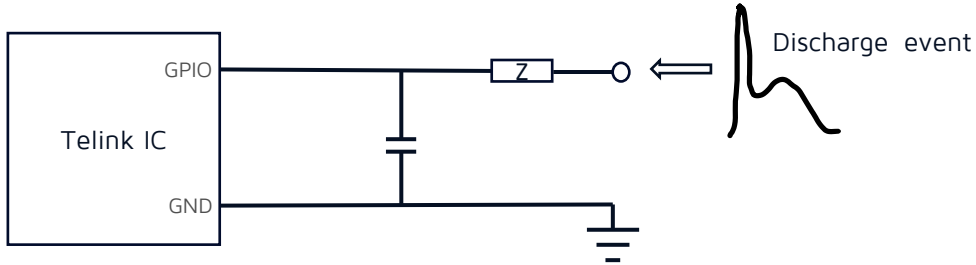
- Refer to chapter 10.
- All the following pins can be used as QDEC
  - PA2,PA3, PB6,PB7,PC2,PC3 ,PD6,PD7

ESD protection

- If the product has high requirements for ESD protection, the TVS components are generally selected for the RF ports.
  - The TVS component is in a high impedance state by default. When the discharge event occurs, it changes to a low impedance state, quickly releasing the current while clamping the voltage within the normal range.



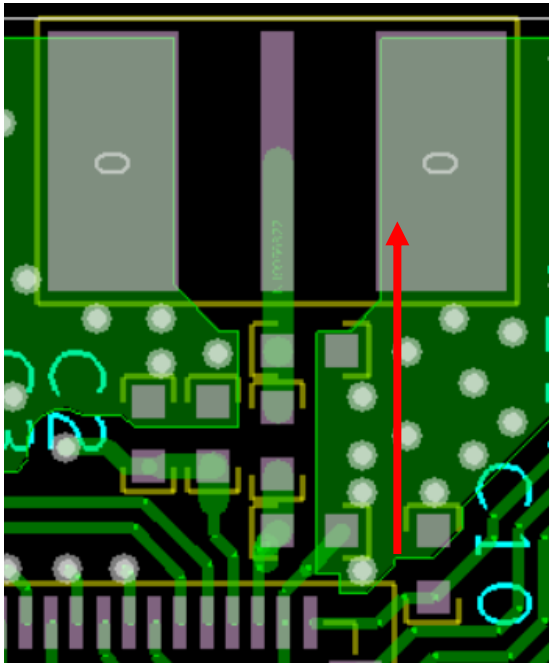
- Resistor or LPF networks can be used for ESD protection of low-speed signals.
  - It can effectively reduce the voltage and current through the GPIO port.

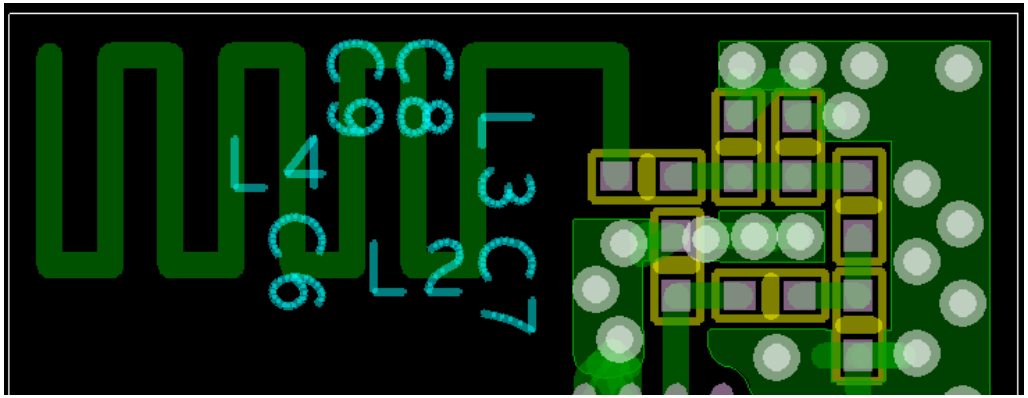


PCB Design Guideline

RF layout

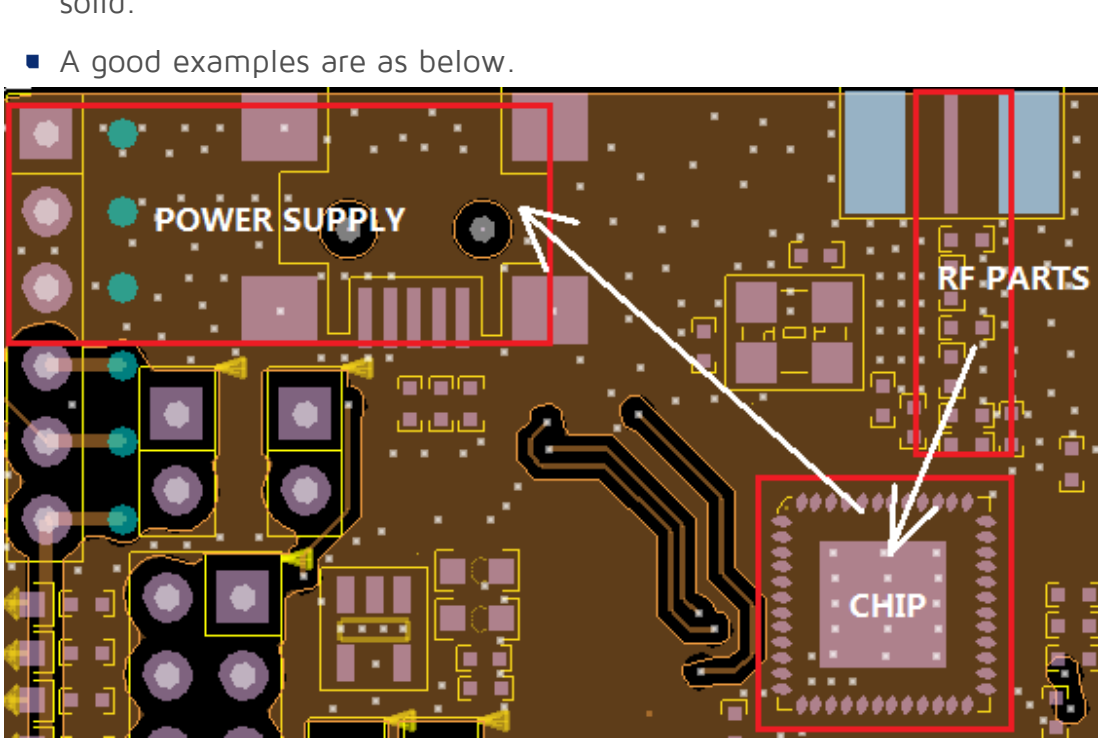
- The components on the RF path MUST be placed one by one. and they MUST be placed close to each other, no stub.
- It the area is not enough, can fold it, but MUST use ground and via to shield RF trace.

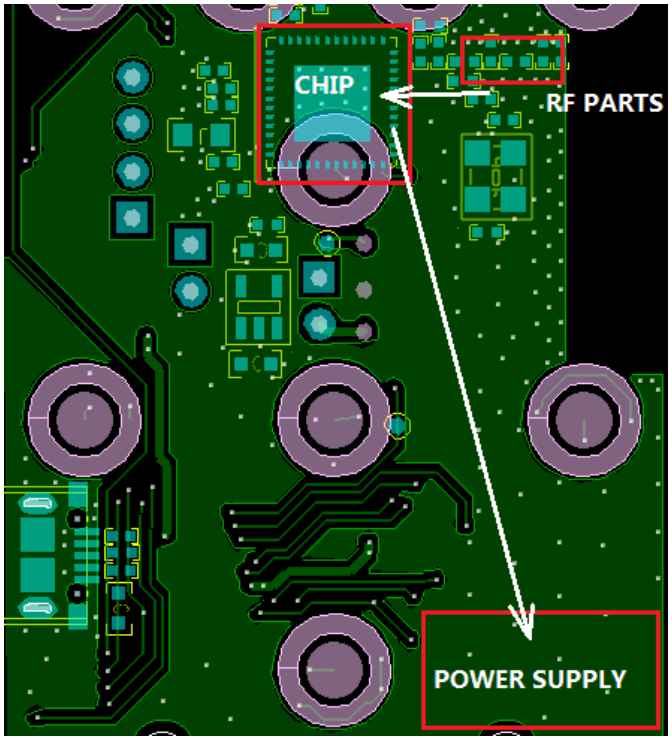




Solid Ground Plane

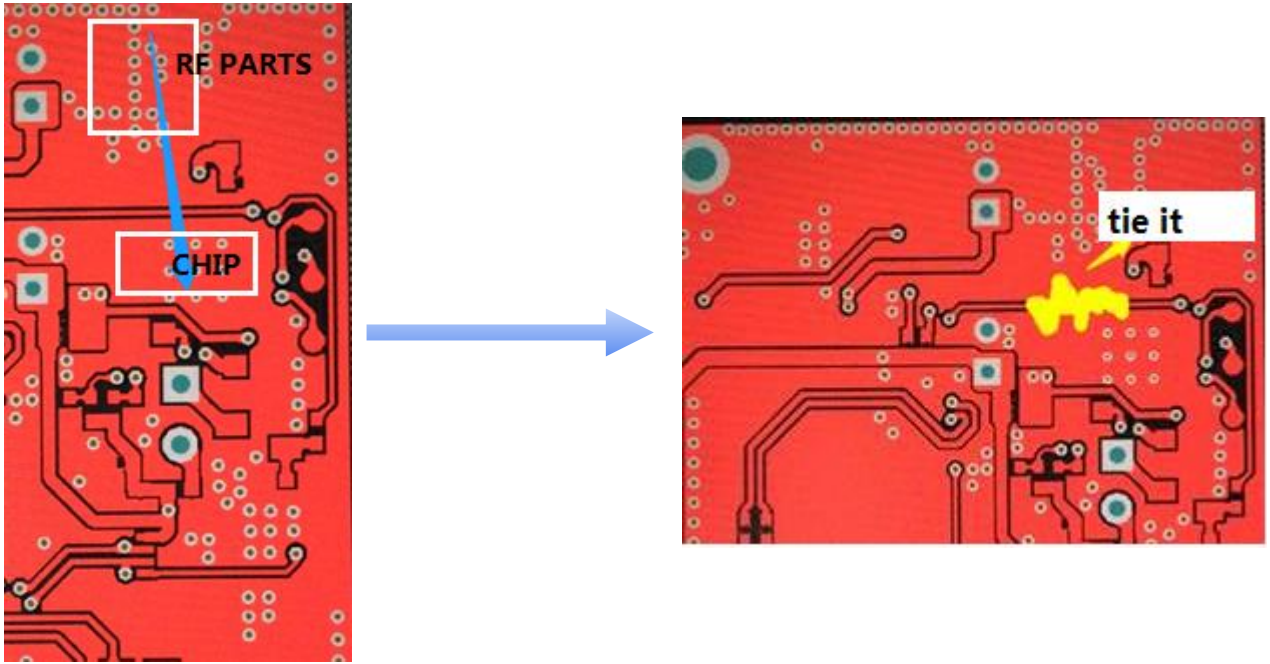
- The ground plane MUST be wide, solid. The ground plane from power supply to chip, then at last to RF parts MUST be solid.
- A good examples are as below.





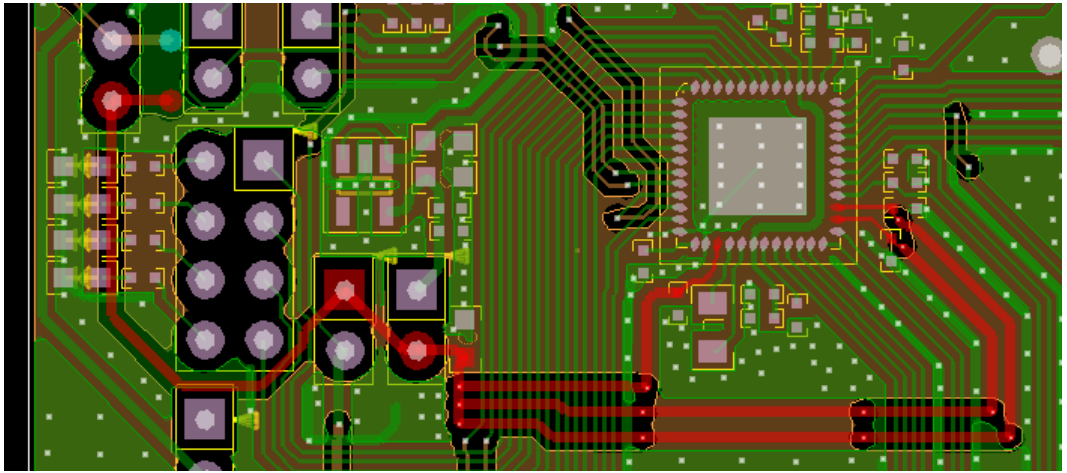
Solid Ground Plane(Cont)

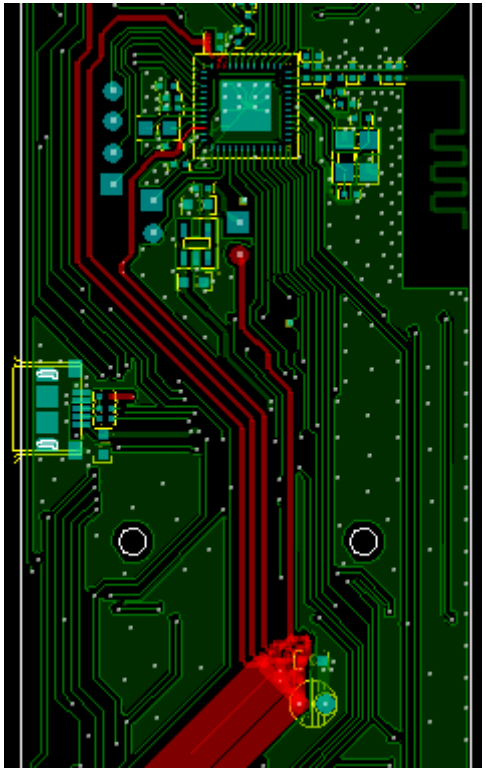
- A bad example is as below.
  - Ground plane between RF parts and chip is cut off, the rx performance is greatly affected.
  - Tie them together, the RX performance matches the data on the datasheet.



Star connection

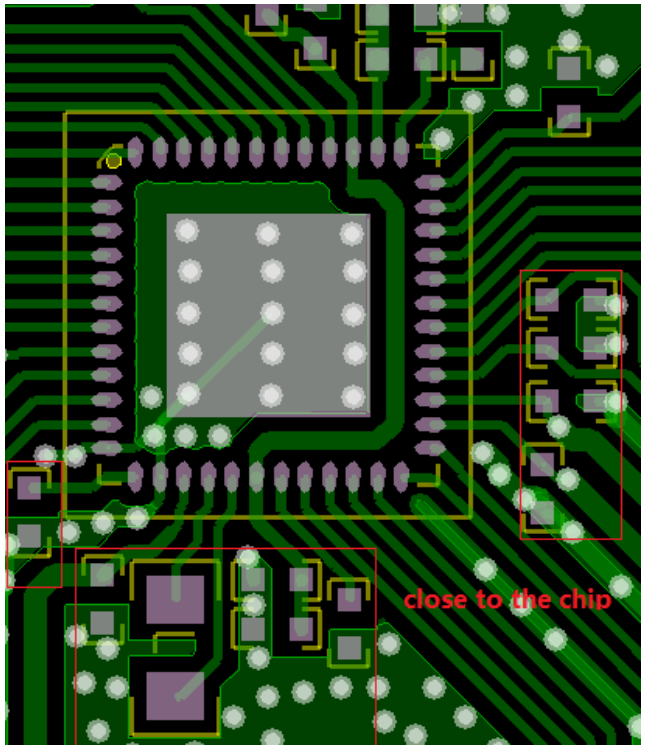
- Power supply should be connected in star-type connection.
  - If there is no audio function, can connect them together.

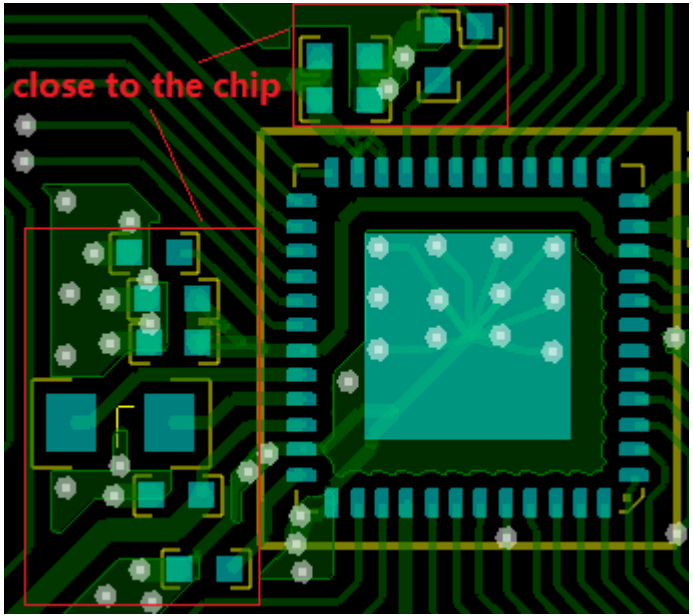




Decoupling capacitor

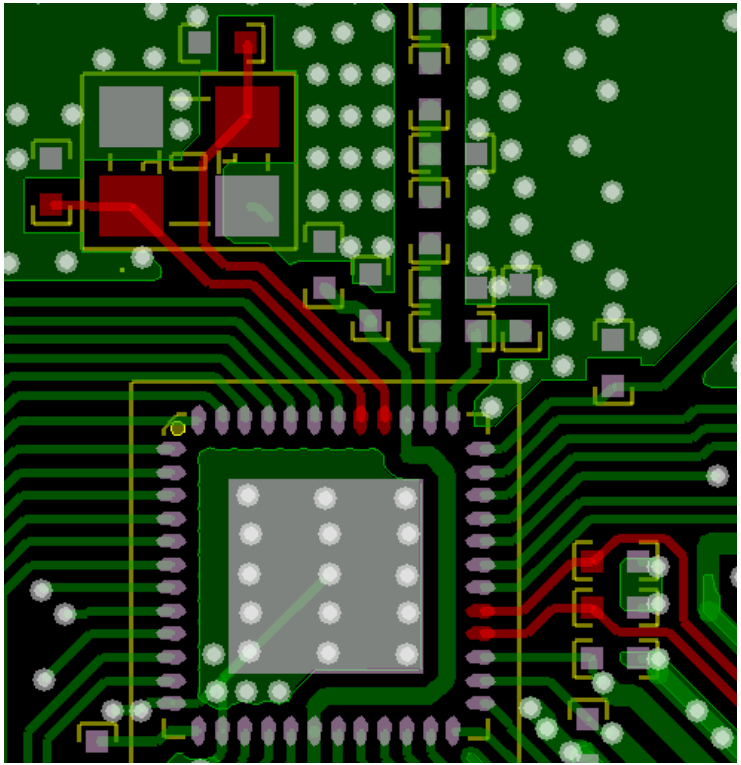
- Decoupling capacitors MUST be placed close to power pins.

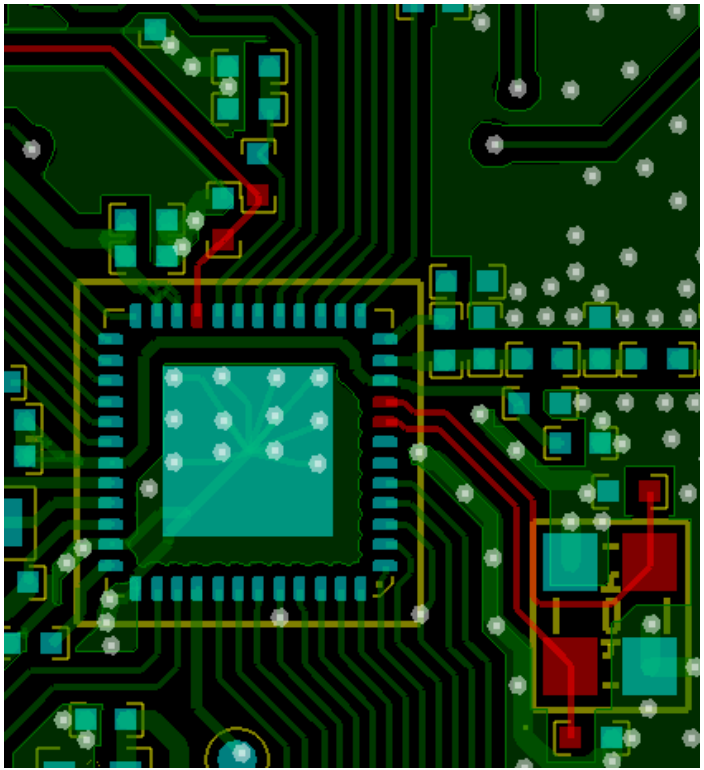




Key traces

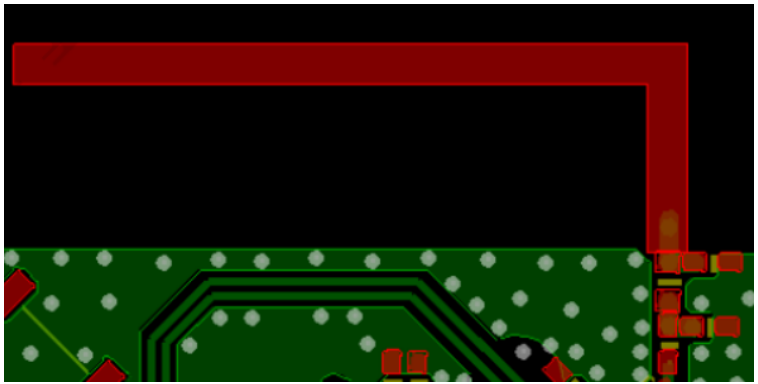
- To avoid EMI issue, some important parts such as crystal, audio trace, mic trace and usb trace MUST be shielded by GND and via.





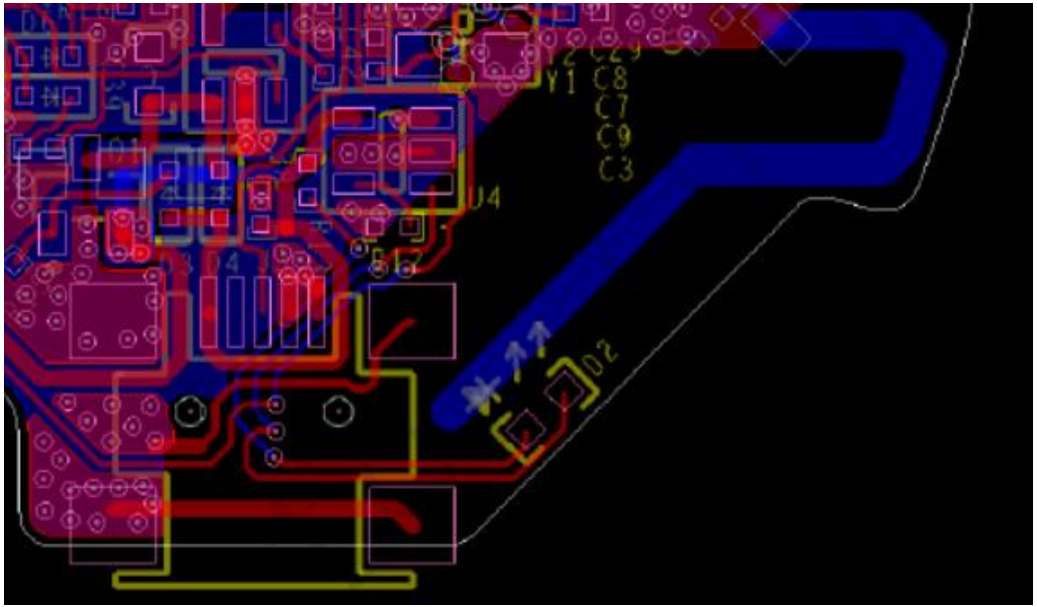
Antenna – common requirement

- Antenna trace width shouldn`t be too narrow in order to decrease loss.
- Line width should be 0.5mm or above, generally it`s recommended to be 0.5mm or 1mm.
- Top and bottom of antenna location should not be covered by GND.
- The distance between antenna and GND should be 3mm or above.
- Generally antenna length is 20mm~30mm. The smaller the GND is, the longer the antenna should be.



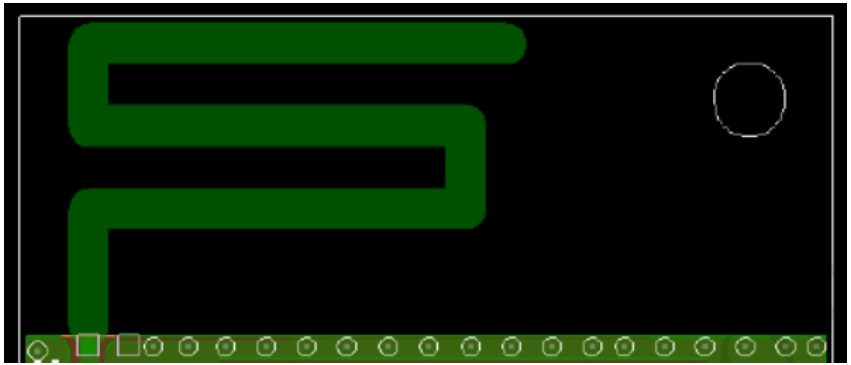
Antenna – keep away others

- Keep PCB antenna far away from metal, battery, or other components, such as 3mm or 5mm.
- A bad example is showed as below. The antenna is too close to USB connector.



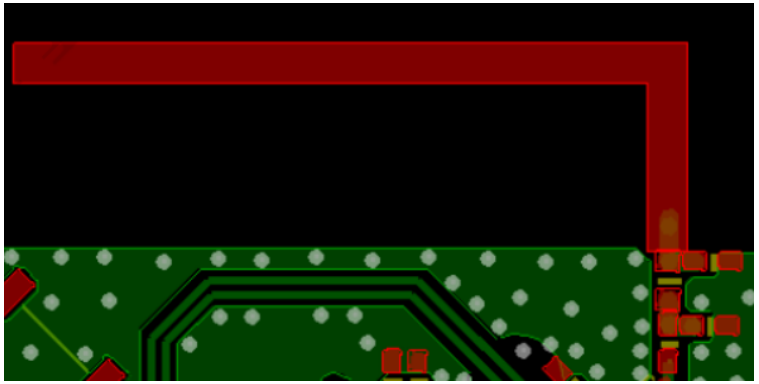
Antenna – don`t exposed to others

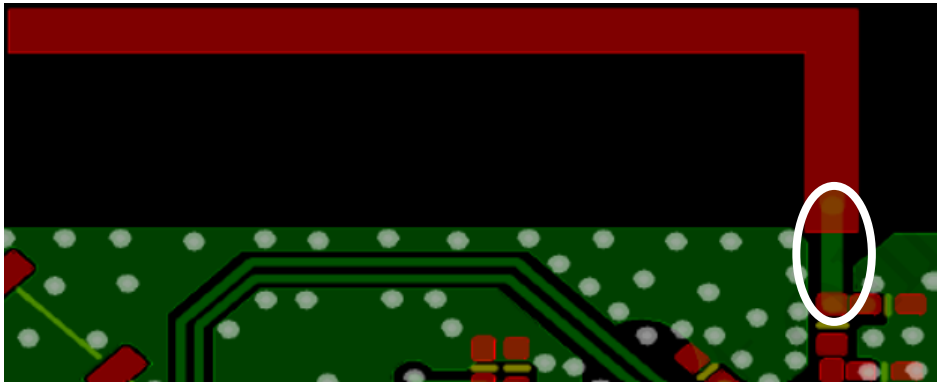
- There MUST be a row of via holes along the antenna on the side parallel to GND. Do not directly expose trace or pad to the antenna.
- The left is a good example. The right is a bad example.



Antenna – matching components

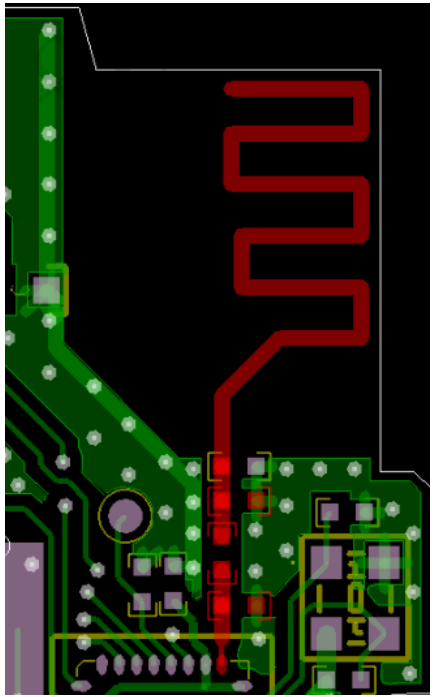
- Antenna matching components should be placed at the boundary of antenna and GND without shrink inward or expand outward.
- The left is a good example. The right is a bad example.

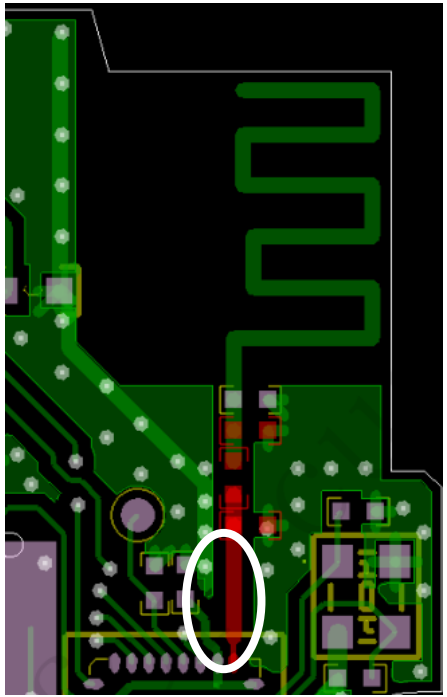




Antenna – impedance design

- The RF line to the antenna port should be short. If RF trace can`t be designed shortly, it must be designed as 50ohm micro-strip line.
- The left is a good example. The right is a bad example.





Change Logs

- 2022.01.12
  - Initial version
- 2022.02.09
  - Added IO description
- 2023.02.23
  - Added power supply
- 2023.10.16
  - Added ESD protection
- 2023.11.03
  - Update pin32 and pin33 description.

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