

OptiMOS™3 Power-Transistor

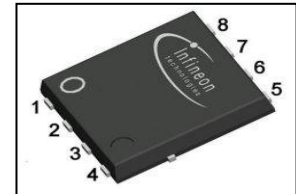
Features

- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC¹⁾ for target applications
- N-channel; Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% Avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

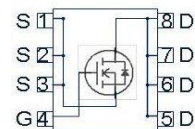
Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	9.3	mΩ
I_D	49	A

PG-TDSON-8



Type	Package	Marking
BSC093N04LS G	PG-TDSON-8	093N04LS



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$	49	A
		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$	31	
		$V_{GS}=4.5\text{ V}$, $T_C=25\text{ °C}$	40	
		$V_{GS}=4.5\text{ V}$, $T_C=100\text{ °C}$	26	
		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^{2)}$	13	
Pulsed drain current ³⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	196	
Avalanche current, single pulse ⁴⁾	I_{AS}	$T_C=25\text{ °C}$	40	
Avalanche energy, single pulse	E_{AS}	$I_D=40\text{ A}$, $R_{GS}=25\text{ Ω}$	10	mJ
Gate source voltage	V_{GS}		±20	V

¹⁾ J-STD20 and JESD22

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	35	W
		$T_A=25\text{ °C}$, $R_{\text{thJA}}=50\text{ K/W}^{(2)}$	2.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}	bottom	-	-	3.6	K/W
		top			20	
Device on PCB	R_{thJA}	6 cm ² cooling area ⁽²⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}$, $I_{\text{D}}=1\text{ mA}$	40	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{D}}=14\text{ }\mu\text{A}$	1.2	-	2	
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}}=40\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{\text{DS}}=40\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=20\text{ V}$, $V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}$, $I_{\text{D}}=20\text{ A}$	-	11.0	13.7	mΩ
		$V_{\text{GS}}=10\text{ V}$, $I_{\text{D}}=40\text{ A}$	-	7.8	9.3	
Gate resistance	R_{G}		-	1	-	Ω
Transconductance	g_{fs}	$ V_{\text{DS}} >2 I_{\text{D}} /R_{\text{DS(on)max}}$, $I_{\text{D}}=40\text{ A}$	34	67	-	S

⁽²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁽³⁾ See figure 3 for more detailed information

⁽⁴⁾ See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V},$ $f=1\text{ MHz}$	-	1400	1900	pF
Output capacitance	C_{oss}		-	340	450	
Reverse transfer capacitance	C_{rss}		-	16	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V},$ $I_D=30\text{ A}, R_{G,ext}=1.6\text{ }\Omega$	-	3.6	-	ns
Rise time	t_r		-	2.4	-	
Turn-off delay time	$t_{d(off)}$		-	16	-	
Fall time	t_f		-	2.8	-	

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=20\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	4.9	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	2.3	-	
Gate to drain charge	Q_{gd}		-	2.0	-	
Switching charge	Q_{sw}		-	4.6	-	
Gate charge total	Q_g		-	18	24	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V
Gate charge total	Q_g	$V_{DD}=20\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	8.6	11.4	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }10\text{ V}$	-	17	-	
Output charge	Q_{oss}	$V_{DD}=20\text{ V}, V_{GS}=0\text{ V}$	-	13	-	

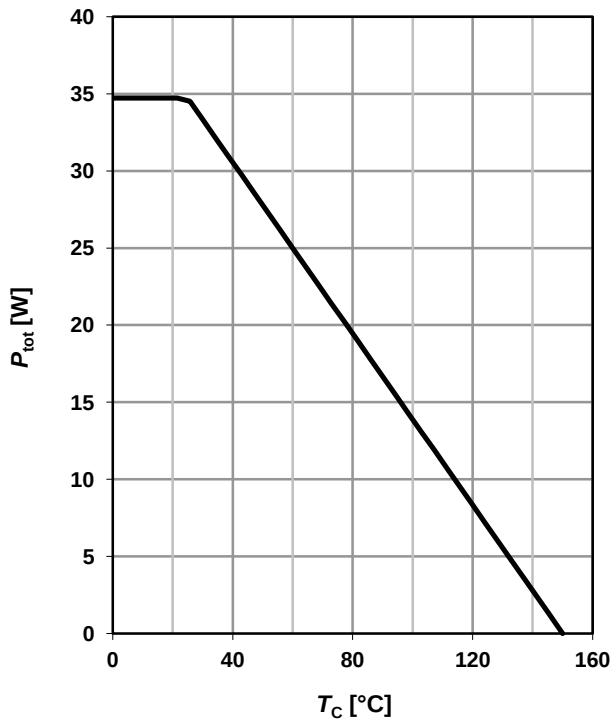
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	29	A
Diode pulse current	$I_{S,pulse}$		-	-	196	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=40\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.9	1.2	V
Reverse recovery charge	Q_{rr}	$V_R=20\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	15	-	nC

⁵⁾ See figure 16 for gate charge parameter definition

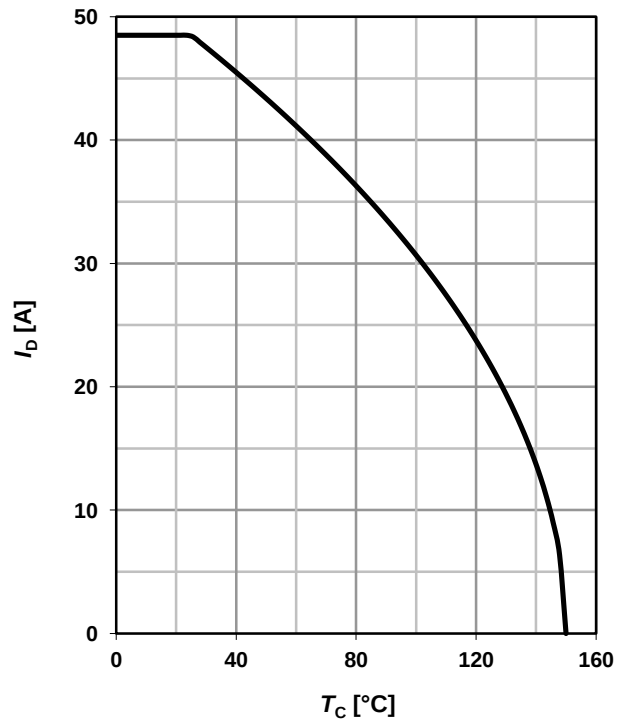
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

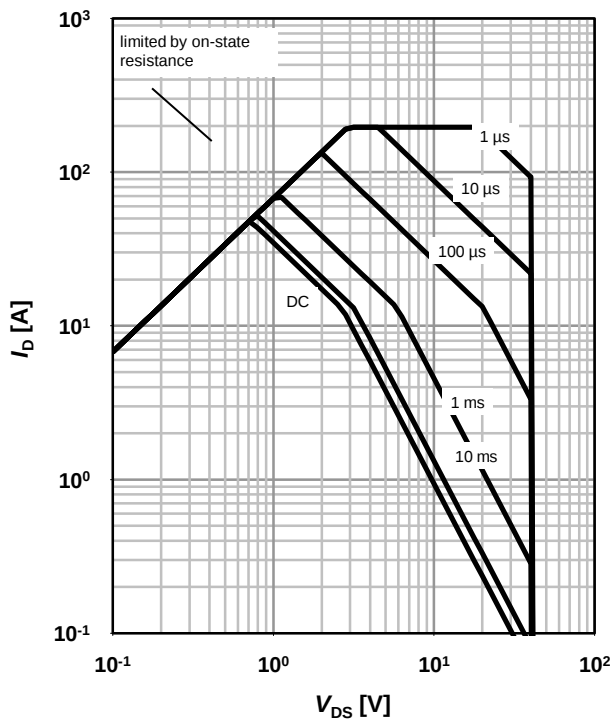
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

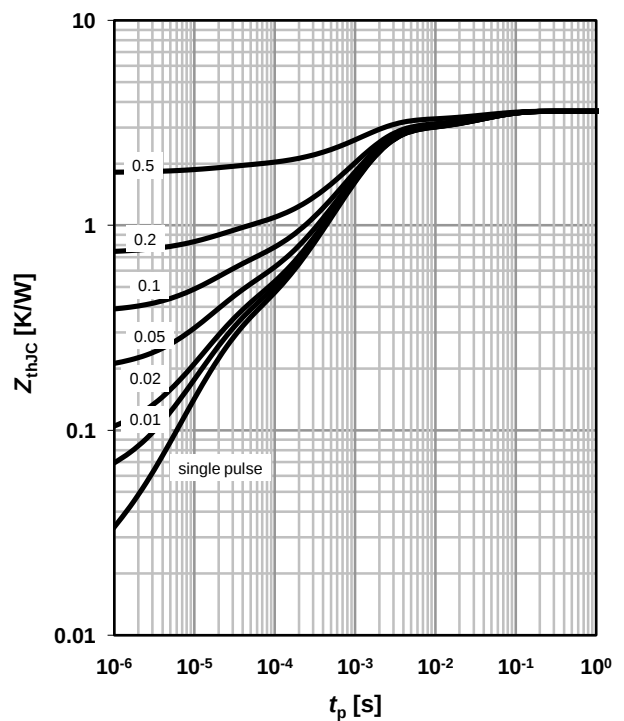
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

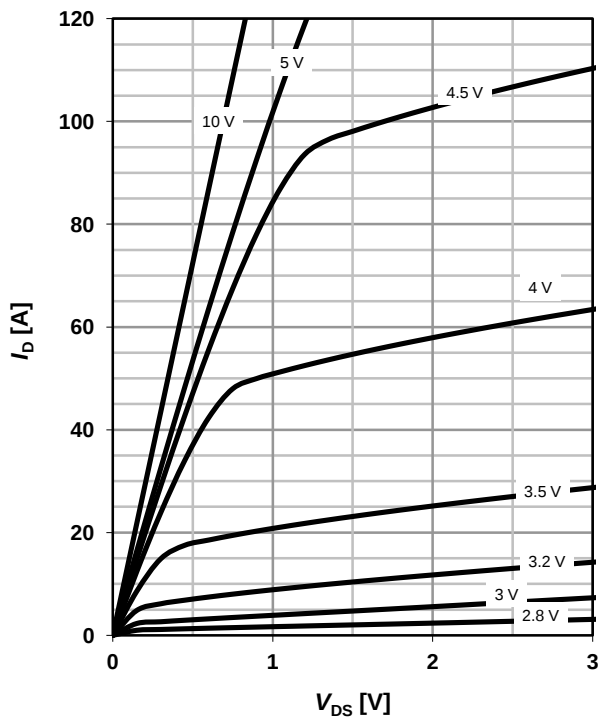
parameter: $D = t_p / T$



5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

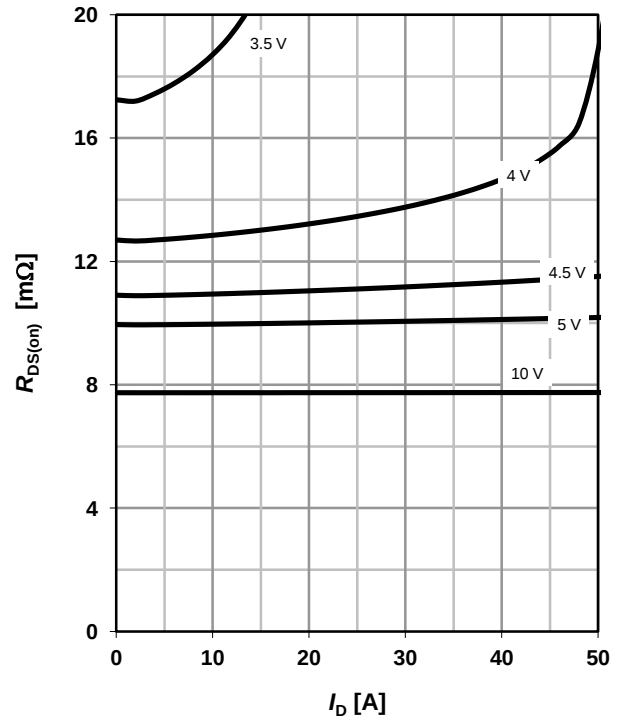
parameter: V_{GS}



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

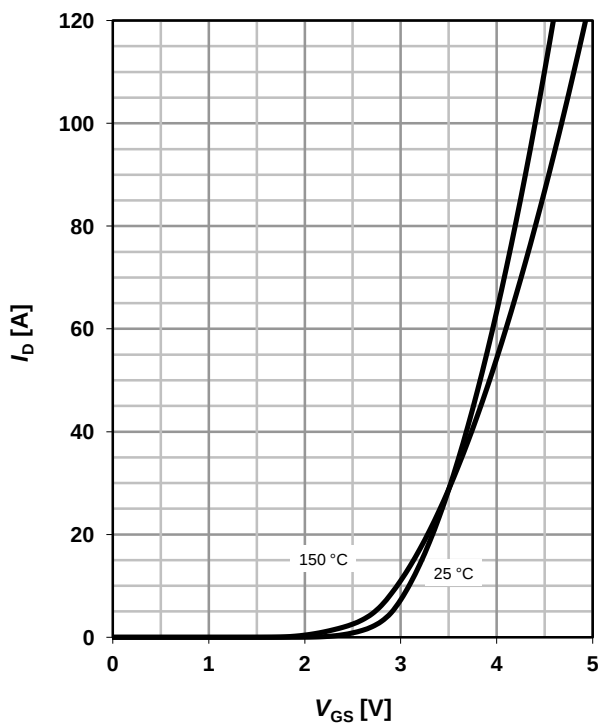
parameter: V_{GS}



7 Typ. transfer characteristics

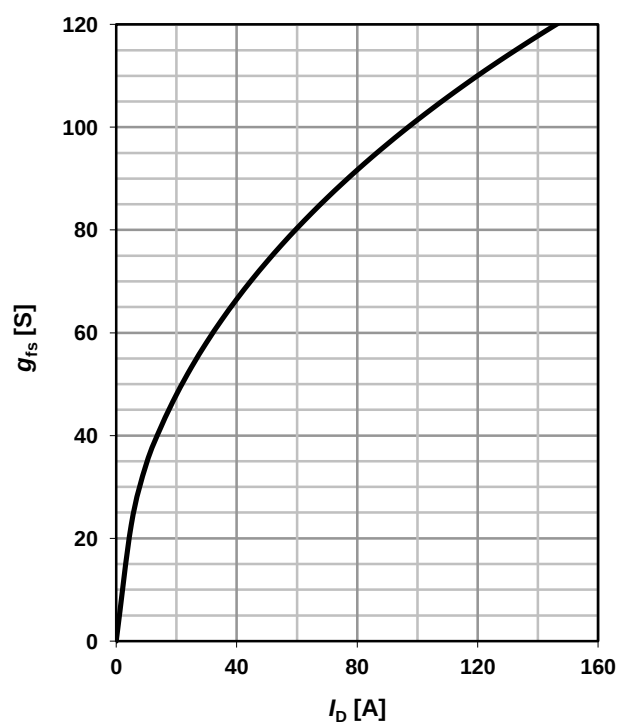
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)\max}$$

parameter: T_j



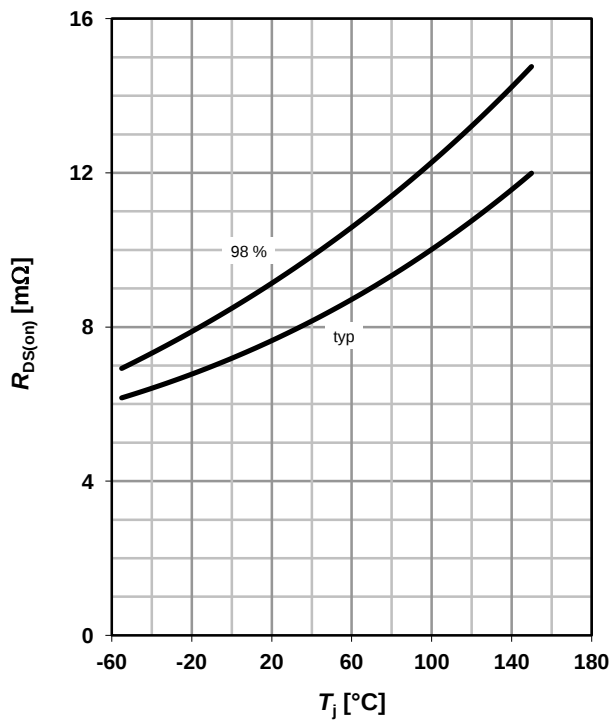
8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$



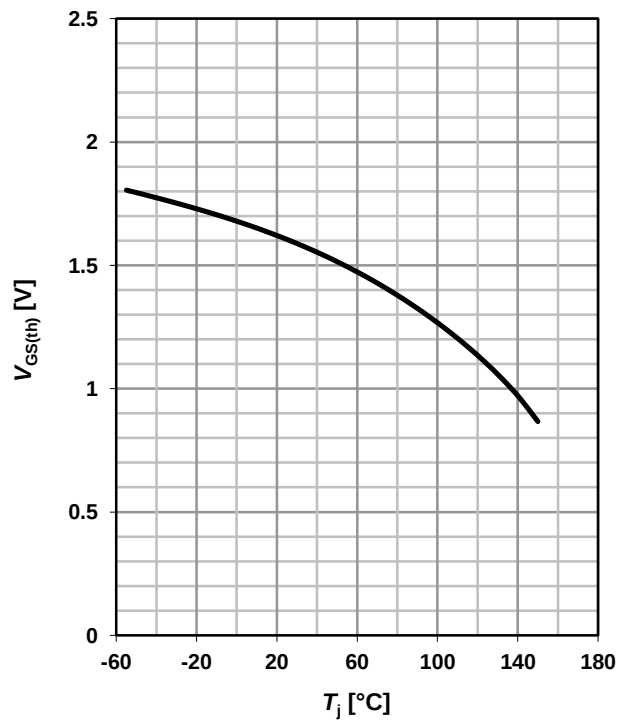
9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = 40 \text{ A}; V_{GS} = 10 \text{ V}$$



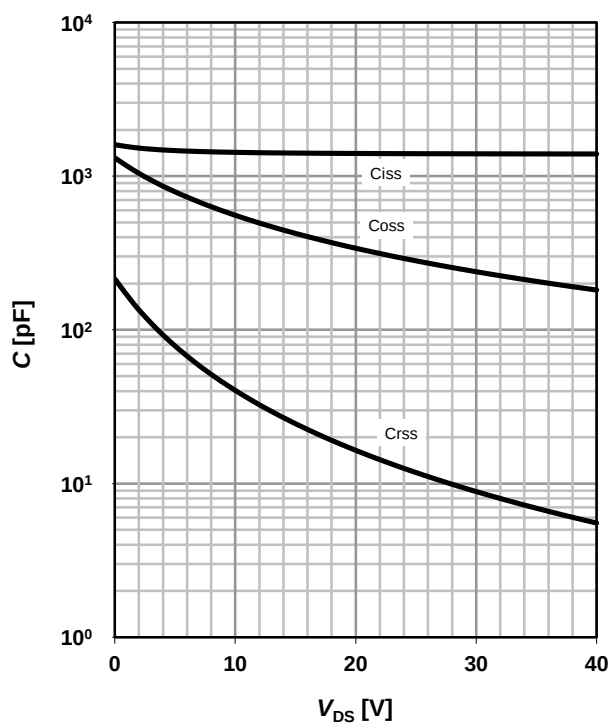
10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 14 \mu\text{A}$$



11 Typ. capacitances

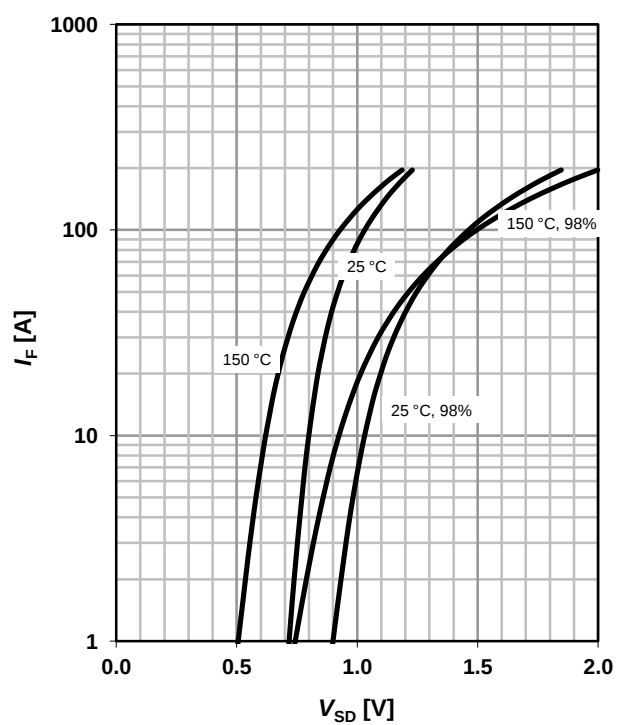
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

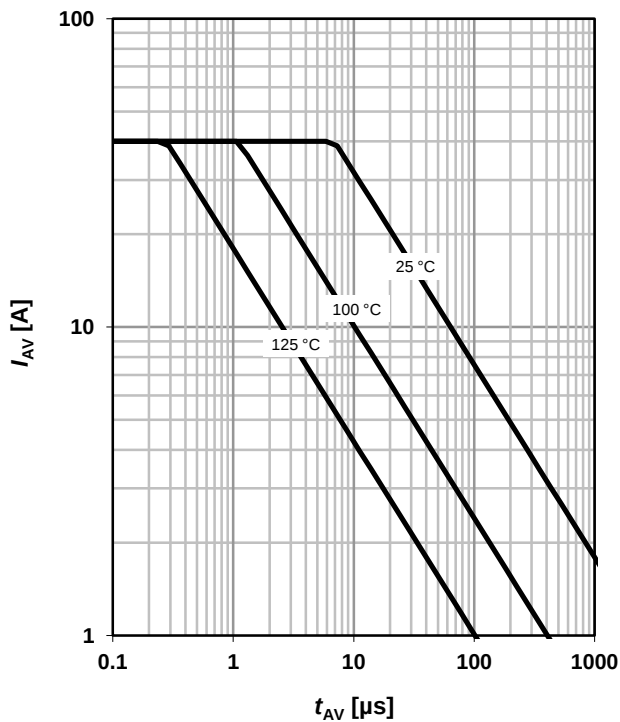
parameter: T_j



13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

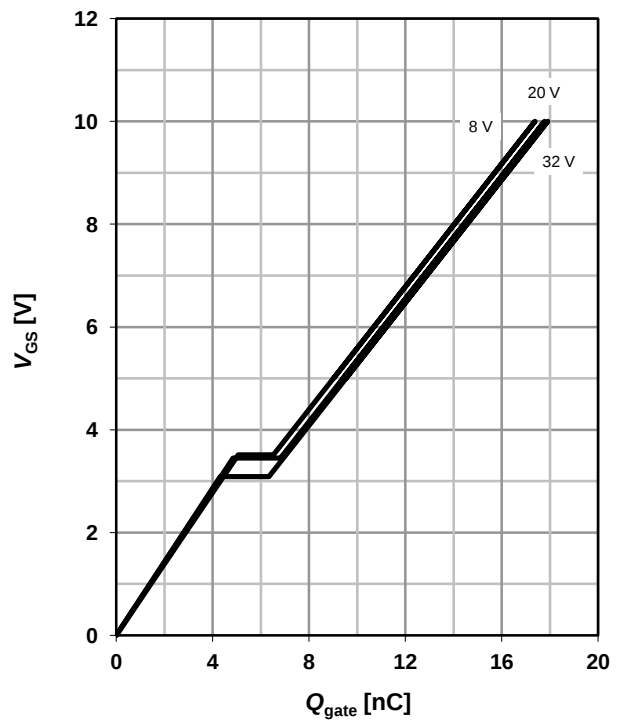
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

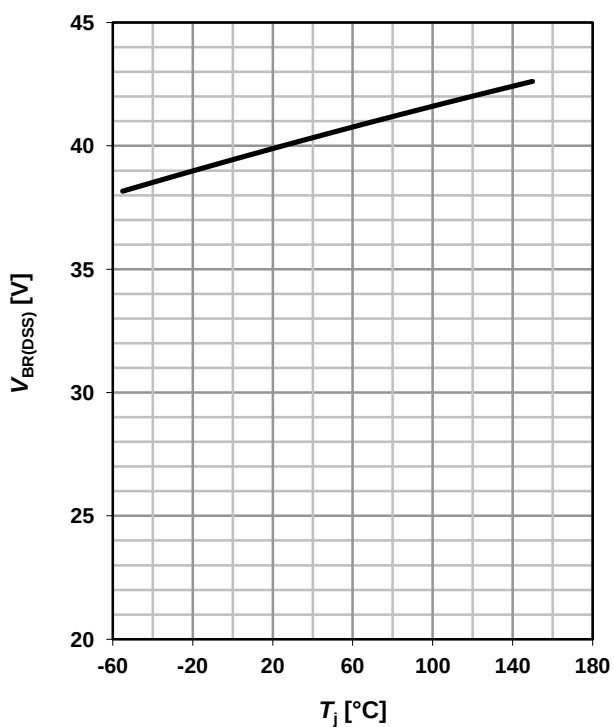
$$V_{GS}=f(Q_{\text{gate}}); I_D=30\ \text{A pulsed}$$

parameter: V_{DD}



15 Drain-source breakdown voltage

$$V_{BR(DSS)}=f(T_j); I_D=1\ \text{mA}$$



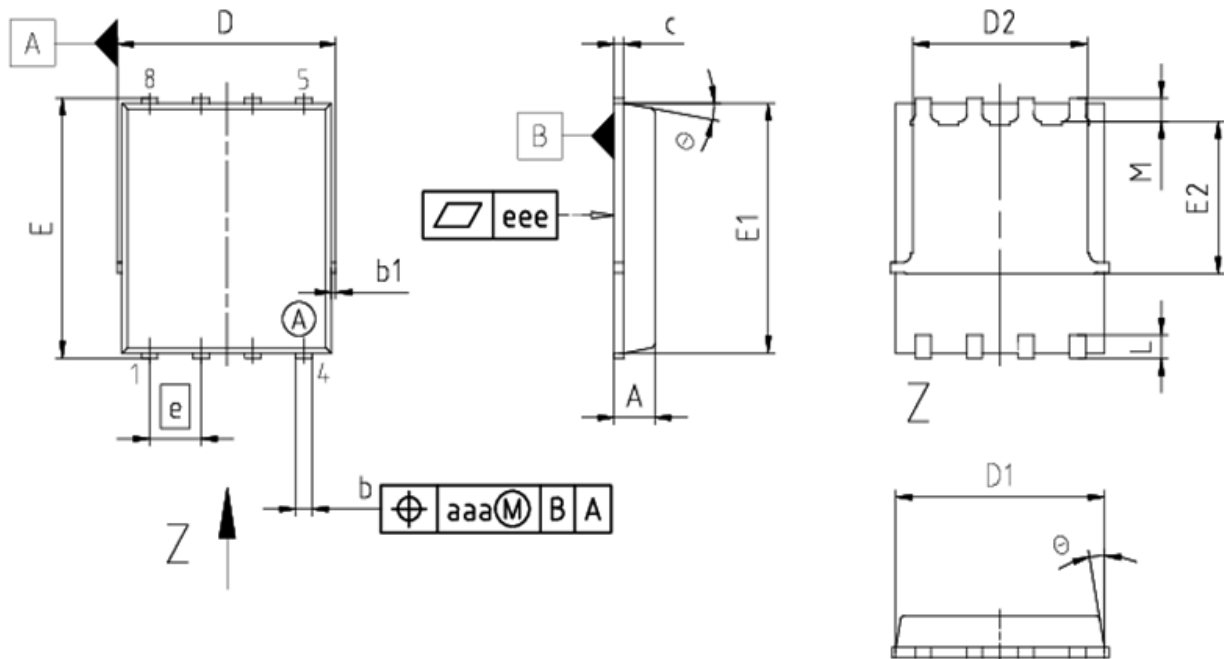
16 Gate charge waveforms



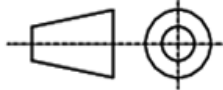
Package Outline

PG-TDSON-8

PG-TDSON-8: Outline



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
θ	8.5°	12°
aaa	0.25	
eee	0.08	

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EUROPEAN PROJECTION 
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Footprint

PG-TDSON-8: Tape



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