

# Broadband 2-Stage LNA

## 1 - 6 GHz



MAAL-011188

Rev. V2

### Features

- Broadband 2-Stage LNA
- Gain:
  - 35.2 dB @ 2.50 GHz
  - 35.1 dB @ 3.75 GHz
  - 35.2 dB @ 4.70 GHz
- Noise Figure:
  - 0.79 dB @ 2.50 GHz
  - 0.86 dB @ 3.75 GHz
  - 0.92 dB @ 4.70 GHz
- Single 5 V Supply
- Enable Pin with 1.8 V logic
- Low DC Current: 80 mA
- Lead-Free 3 mm 16 Lead QFN Package
- RoHS\* Compliant

### Applications

- 5G Massive MIMO
- Wireless Infrastructure
- General purpose wireless
- TDD or FDD systems

### Description

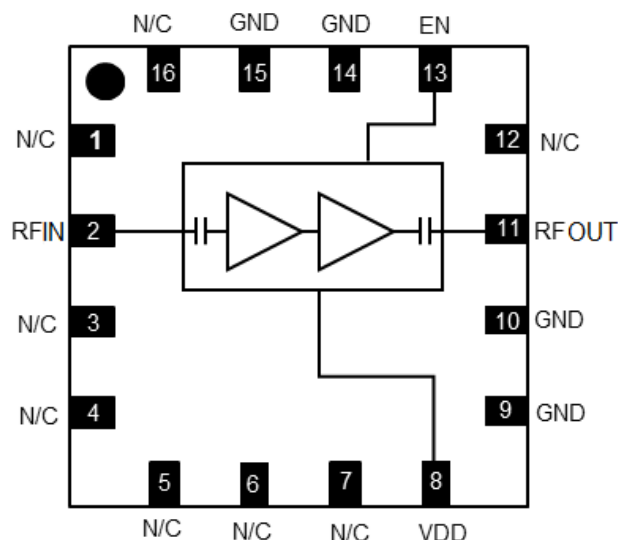
The MAAL-011188 is a compact surface mount, highly integrated 2-stage low noise amplifier (LNA). This LNA is designed for operation from 1 to 6 GHz and is housed in a lead-free 3 mm 16-lead QFN plastic package.

The MAAL-011188 features low noise figure, high gain and low power consumption. The LNA requires a single 5 V supply and the Enable pin is 1.8 V CMOS compatible. All the bias circuitry and matching components are internal to the device.

### Ordering Information

Part Number	Package
MAAL-011188-TR1000	1000 part reel
MAAL-011188-001SMB	Sample Board

### Functional Schematic



### Pin Configuration<sup>1</sup>

Pin #	Pin Name	Description
1,3,4,5,6,7,12,16	N/C	No Connect
9,10,14,15	GND	Ground
2	RFIN	RF Input
8	VDD	Supply Voltage
11	RFOUT	RF Output
13	EN	LNA Enable
17	Paddle <sup>2</sup>	Ground

1. MACOM recommends connecting GND and N/C pins to ground.
2. The exposed pad centered on the package bottom must be connected to PCB ground with low electrical and thermal resistances.

\* Restrictions on Hazardous Substances, compliant to current RoHS EU directive

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### AC Electrical Specifications (LNA ON Mode): $P_{IN} = -30$ dBm, $T_C = +25^\circ\text{C}$ , $V_{DD} = 5$ V, $Z_0 = 50 \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	2.50 GHz 3.75 GHz 4.70 GHz	dB	32 32 —	35.2 35.1 35.2	—
Input IP3	$P_{IN}/\text{tone} = -30$ dBm, Tone Delta = 2 MHz, 2.50 GHz 3.75 GHz 4.70 GHz	dBm	—	-5.2 -3.7 -4.8	—
Input P1dB	2.50 GHz 3.75 GHz 4.70 GHz	dBm	—	-17.4 -17.6 -18.8	—
Noise Figure	2.50 GHz 3.75 GHz 4.70 GHz	dB	—	0.79 0.86 0.92	—
RF <sub>IN</sub> Port Return Loss	RF <sub>IN</sub> Port, 2.50 GHz RF <sub>IN</sub> Port, 3.75 GHz RF <sub>IN</sub> Port, 4.70 GHz	dB	—	24 21 18	—
RF <sub>OUT</sub> Port Return Loss	RF <sub>OUT</sub> Port, 2.50 GHz RF <sub>OUT</sub> Port, 3.75 GHz RF <sub>OUT</sub> Port, 4.70 GHz	dB	—	15 20 16	—
Reverse Isolation	2.50 GHz 3.75 GHz 4.70 GHz	dB	—	55 56 55	—

### Transient Electrical Specifications:

Freq. = 2.5 GHz,  $P_{IN} = -30$  dBm,  $T_C = 25^\circ\text{C}$ ,  $V_{DD} = 5$  V,  $Z_0 = 50 \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
EN Gain Settling Time	RF <sub>IN</sub> to RF <sub>OUT</sub> gain settling time within 0.3 dB of final value after EN command	$\mu\text{s}$	—	0.3	—
Power on Gain Settling Time	RF <sub>IN</sub> to RF <sub>OUT</sub> gain settling time within 0.5 dB of final value after DC power on	ms	—	1	—

### DC Electrical Specifications: $T_C = 25^\circ\text{C}$ , $V_{DD} = 5$ V, $Z_0 = 50 \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Supply Voltage	—	V	4.75	5	5.25
Amplifier Bias Current	LNA ON Mode Disable Mode	mA	—	80 2.3	—
EN Control Voltage	LNA ON Mode, Logic High Disable Mode, Logic Low	V	—	1.8 0	—
EN Logic Input Current	LNA ON Mode, Logic High Disable Mode, Logic Low	$\mu\text{A}$	—	40 +/-0.03	—

### Control Truth Table

EN Control	
LNA ON Mode	Logic High
Disable Mode	Logic Low or Open

### Absolute Maximum Ratings<sup>3,4</sup>

Parameter	Absolute Maximum
RF <sub>IN</sub> Input Power <sup>5</sup> Freq. = 3.75 GHz: LNA ON Mode	23 dBm LTE (8 dB PAR), 26 dBm CW
DC Voltages: V <sub>DD</sub> & RF <sub>IN</sub> EN & RF <sub>OUT</sub>	-0.5 to +5.5 V -0.5 to +2.75 V
Junction Temperature: LNA ON Mode <sup>6,8</sup>	+150°C
Operating Temperature <sup>7</sup>	-40°C to +105°C
Storage Temperature	-55°C to +150°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Single event, up to 10 seconds duration.
6. Operating at nominal conditions with T<sub>J</sub> ≤ +150°C (LNA ON Mode) will ensure MTTF >> 1 x 10<sup>6</sup> hours.
7. Operating/Case temperature (T<sub>C</sub>) is the temperature of the exposed paddle.
8. Junction Temperature (T<sub>J</sub>) = T<sub>C</sub> + Θ<sub>JC</sub> \* P<sub>DISS</sub> where P<sub>DISS</sub> is the total DC & RF dissipated power.
  - LNA ON Mode: Typical thermal resistance (Θ<sub>JC</sub>) = 33.4°C/W.

### Handling Procedures

Please observe the following precautions to avoid damage:

### Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1 A and CDM Class C3 devices.

### Power Supplies

De-coupling capacitors should be placed at the VDD supply pin to minimize noise and fast transients. Supply voltage change or transients should have a slew rate smaller than 1 V / 10 μs. In addition, all control pins should remain at 0 V (+/- 0.3 V) and no RF power should be applied while the supply voltage ramps or while it returns to zero.

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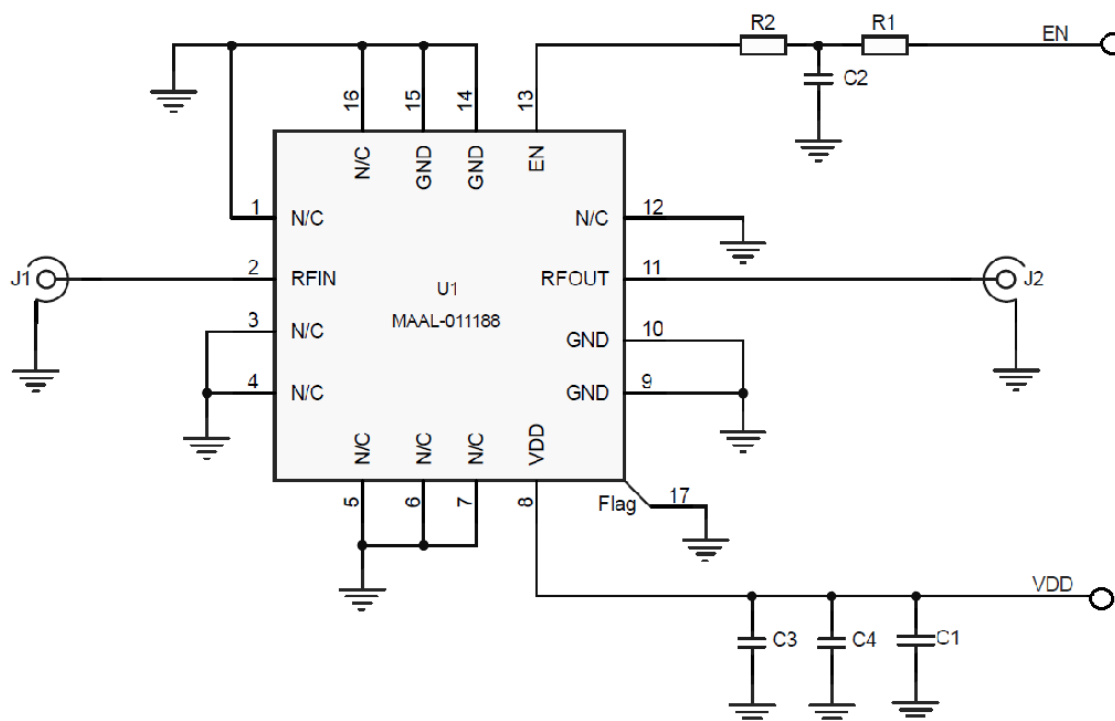
## 1 - 6 GHz



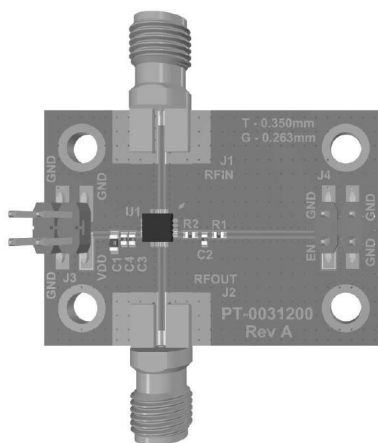
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### Sample Board Schematic



### Sample Board PCB Layout



### Parts List

Part	Value	Case style
C1	10 $\mu$ F	0603
C2	5 pF	0402
C3	470 pF	0402
C4	10 nF	0402
R1	1 k $\Omega$	0402
R2	100 $\Omega$	0402

- Material: Rogers 4003C
- Dielectric thickness: 0.203 mm
- Track/Gap: 0.350/0.263 mm
- Finished copper thickness: 44  $\mu$ m +/- 10  $\mu$ m
- Finish both sides: 0.075  $\mu$ m gold over 4.5 $\mu$ m nickel
- Further layout information available on request

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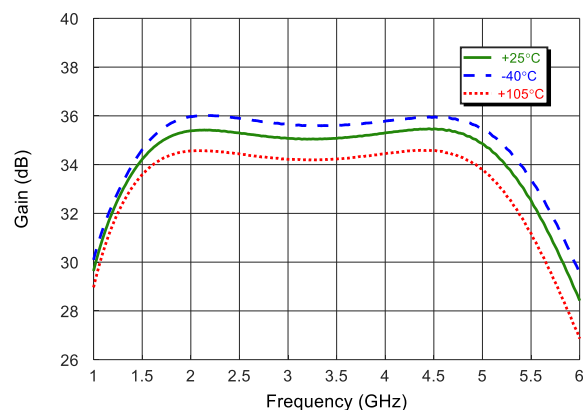
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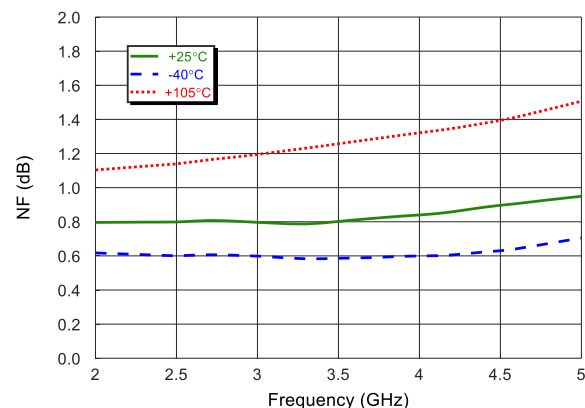
### Typical Performance Curves:

$P_{IN} = -30$  dBm,  $V_{DD} = 5$  V,  $T_C = +25^\circ\text{C}$ ,  $Z_0 = 50 \Omega$  (unless otherwise indicated)

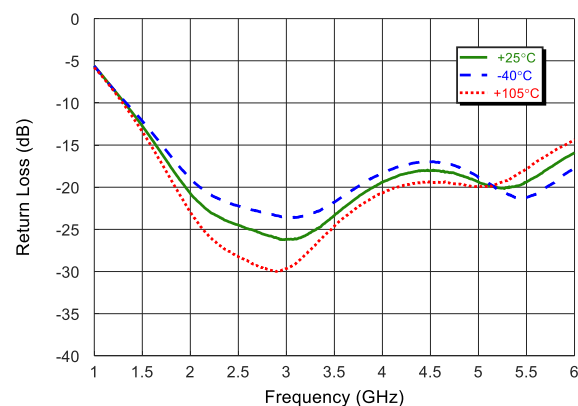
**Gain<sup>9</sup>**



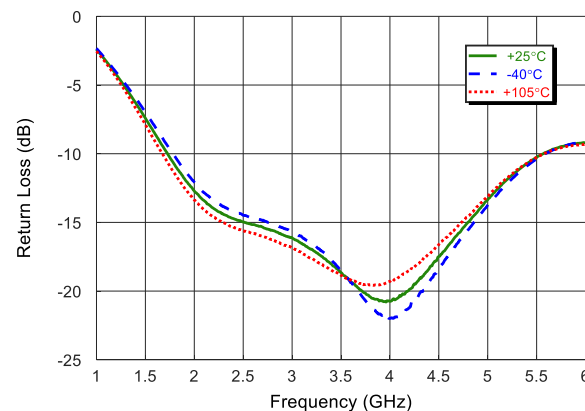
**Noise Figure<sup>9</sup>**



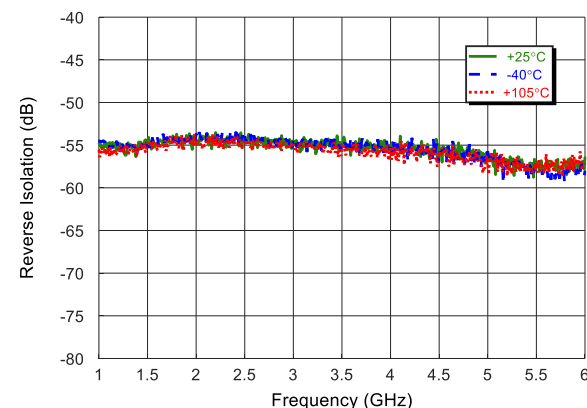
**Input Return Loss**



**Output Return Loss**



**Port Reverse Isolation - RX Mode**



9. For gain, noise figure and isolation plots, RF trace and connector losses are de-embedded.

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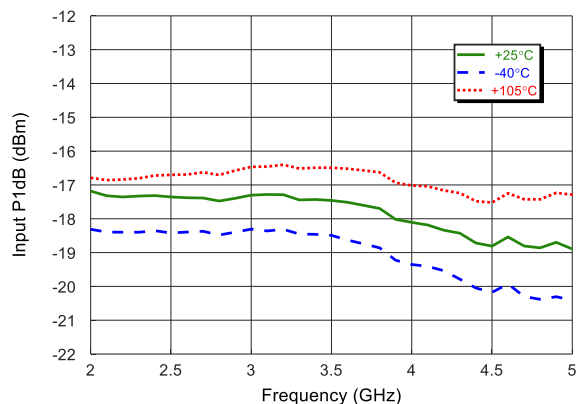
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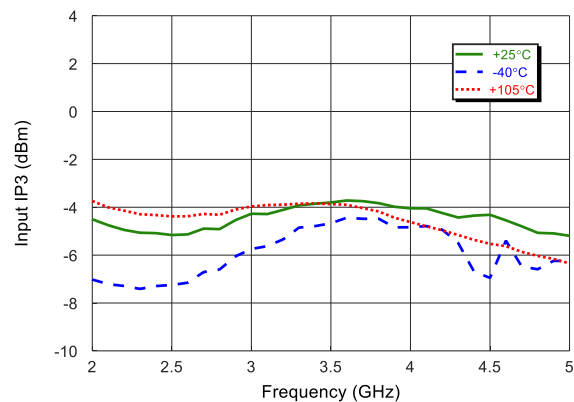
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Input P1dB



Input IP3



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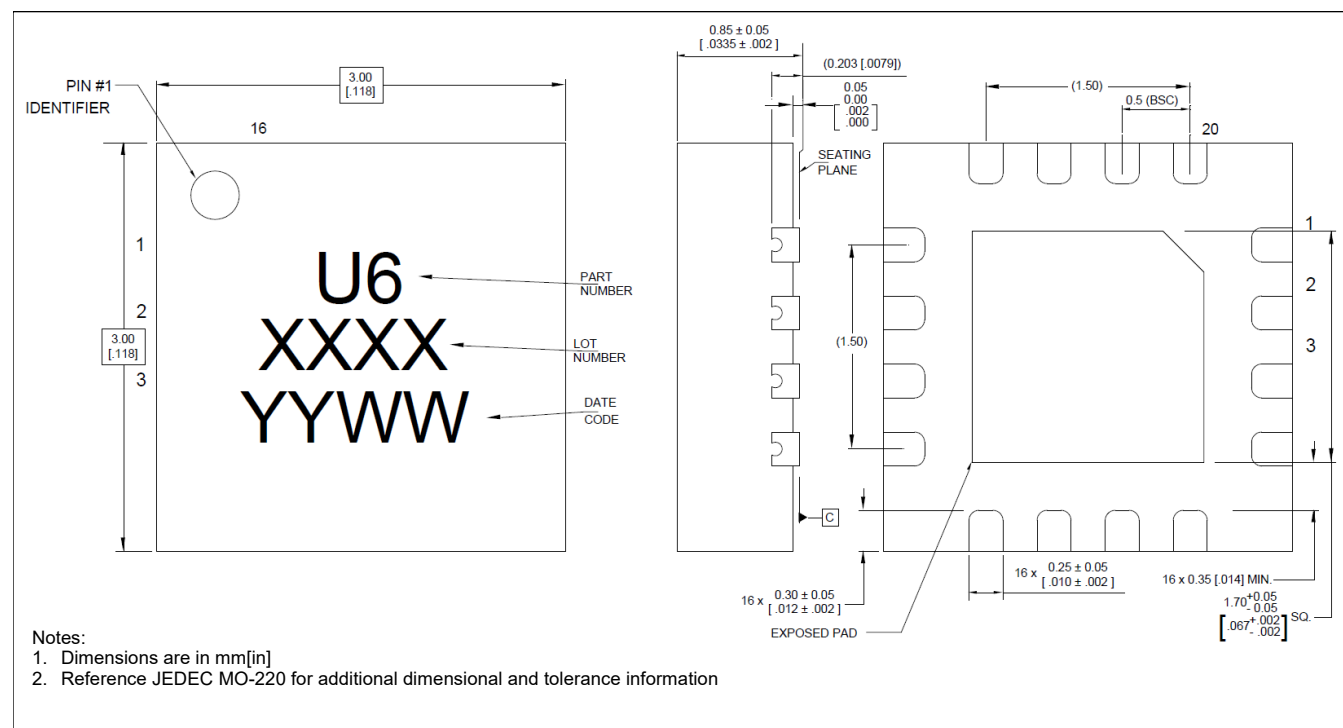
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### Lead-Free 3 mm 16-Lead QFN<sup>†</sup>



<sup>†</sup> Reference Application Note S2083 for lead-free solder reflow recommendations.  
Meets JEDEC moisture sensitivity level 1 requirements in accordance to JEDEC J-STD-020D.  
Plating is NiPdAu over Copper

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