

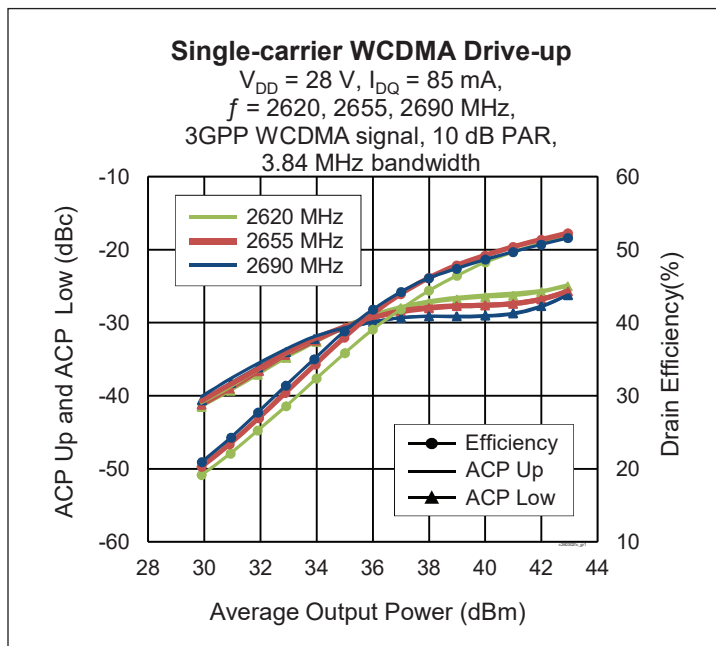
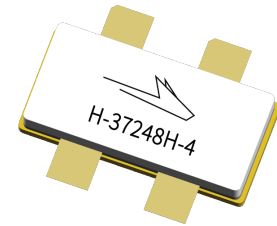
PTAC260302FC

Thermally-Enhanced High Power RF LDMOS FET 30 W, 28 V, 2620 – 2690 MHz

Description

The PTAC260302FC is a 30-watt LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 2620 to 2690 MHz frequency band. This device integrates a 10-W (main) and a 20-W (peak) transistor, making it ideal for asymmetric Doherty amplifier designs. Features include input matching, high gain and thermally-enhanced package with earless flange. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PTAC260302FC
Package H-37248H-4



Features

- Asymmetric design
- Broadband internal matching
- Typical CW performance, 2690 MHz, 28 V (Doherty configuration, combined output)
 - Output power @ $P_{3dB} = 30\text{ W}$
 - Efficiency = 54%
 - Gain = 13 dB
- Typical single-carrier WCDMA performance, 2690 MHz, 28 V, 10 dB PAR
 - Output power = 37.5 dBm avg
 - Gain = 15.5 dB
 - Efficiency = 45%
- Capable of handling 10:1 VSWR @ 32 V, 30 W (CW) output power
- Integrated ESD protection
- Human Body Model Class 1B (per ANSI/ESDA/ JEDEC JS-001)
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in Wolfspeed Doherty test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ} = 85\text{ mA}$, $V_{GS1} = 1.1\text{ V}$, $P_{OUT} = 5.6\text{ W avg}$, $f = 2690\text{ MHz}$,
 3GPP WCDMA signal, 3.84 MHz channel bandwidth, 10 dB peak/average @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	G_{ps}	14.5	15.5	—	dB
Drain Efficiency	η_D	42	45	—	%
Adjacent Channel Power Ratio	ACPR	—	-27	-25	dBc

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10	μA
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1	μA
On-State Resistance	(main) $V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.8	—	Ω
	(peak) $V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.6	—	Ω
Operating Gate Voltage	(main) $V_{DS} = 28\text{ V}$, $I_{DQ} = 0.085\text{ A}$	V_{GS}	2	2.7	3.5	V
	(peak) $V_{DS} = 28\text{ V}$, $I_{DQ} = 0\text{ A}$	V_{GS}	0.4	1.1	1.8	V

Maximum Ratings

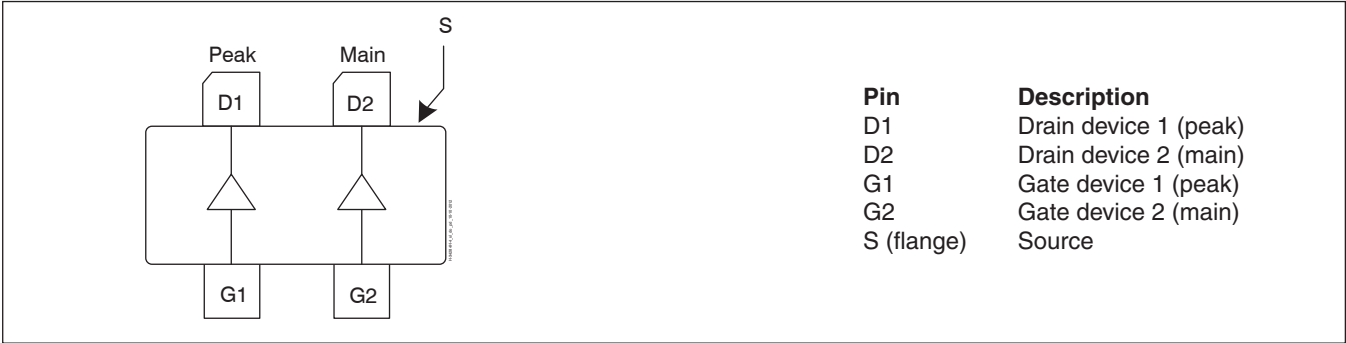
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	−6 to +10	V
Junction Temperature	T_J	225	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	−65 to +150	$^{\circ}\text{C}$
Thermal Resistance	(main) $(T_{CASE} 70^{\circ}\text{C}, 30\text{ W CW})$	R_{qJC}	1.5 $^{\circ}\text{C/W}$
	(peak) $(T_{CASE} 70^{\circ}\text{C}, 30\text{ W CW})$	R_{qJC}	1.7 $^{\circ}\text{C/W}$

Ordering Information

Type and Version	Order Code	Package and Description	Shipping
PTAC260302FC V1 R0	PTAC260302FC-V1-R0	H-37248H-4, Ceramic open-cavity, earless	Tape & Reel, 50 pcs
PTAC260302FC V1 R250	PTAC260302FC-V1-R250	H-37248H-4, Ceramic open-cavity, earless	Tape & Reel, 250 pcs

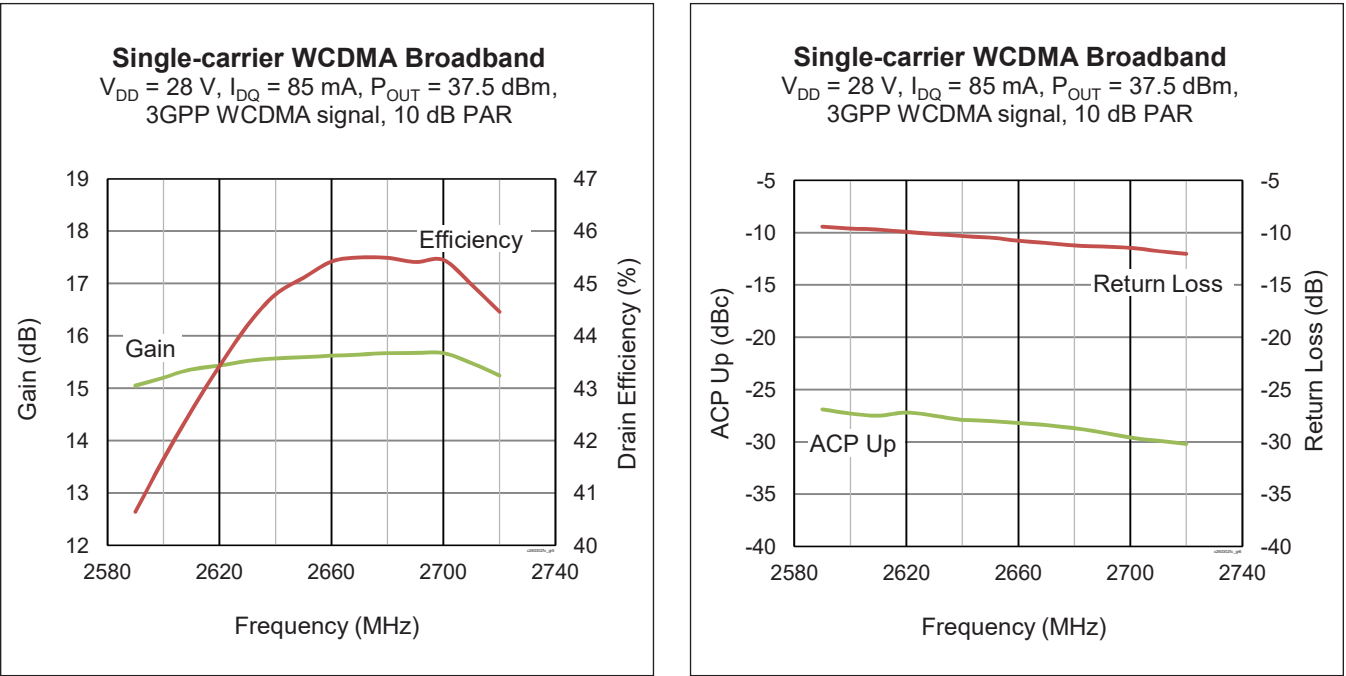


Pinout Diagram (top view)

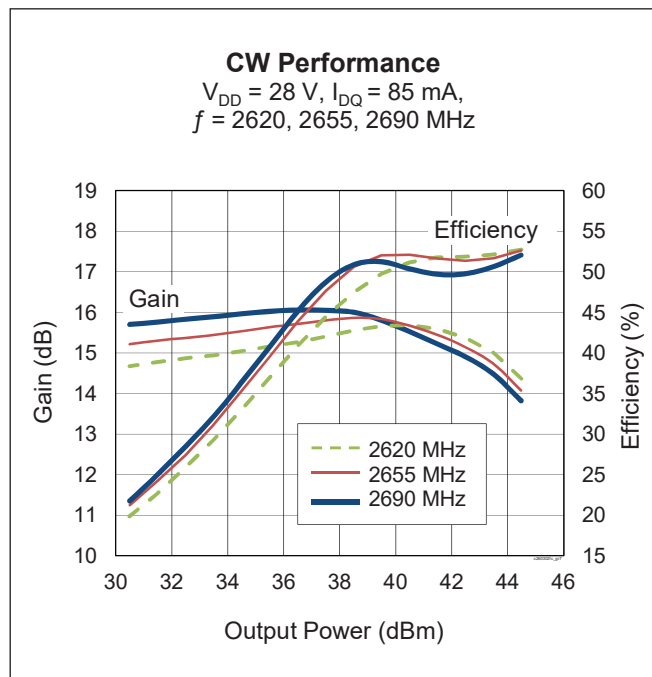
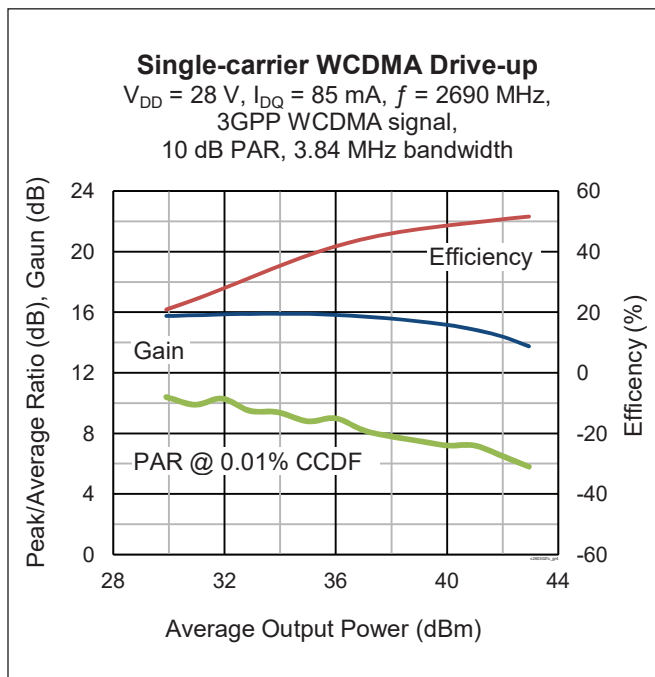
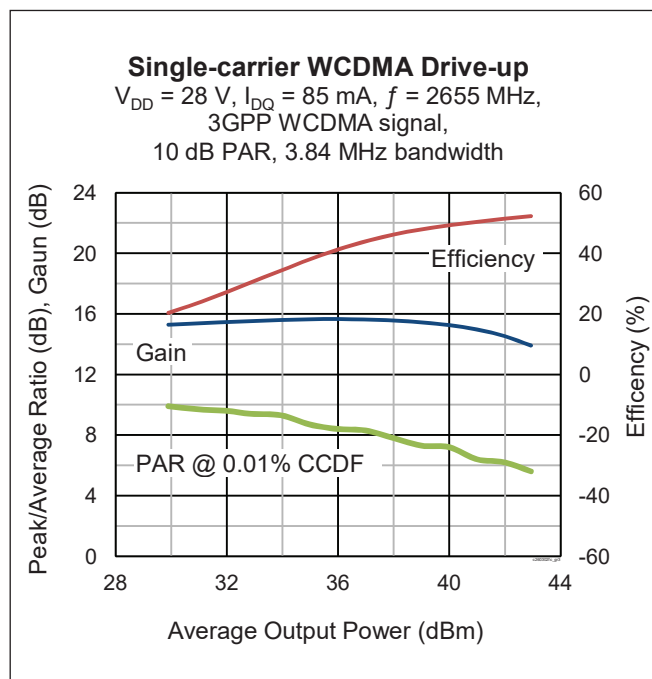
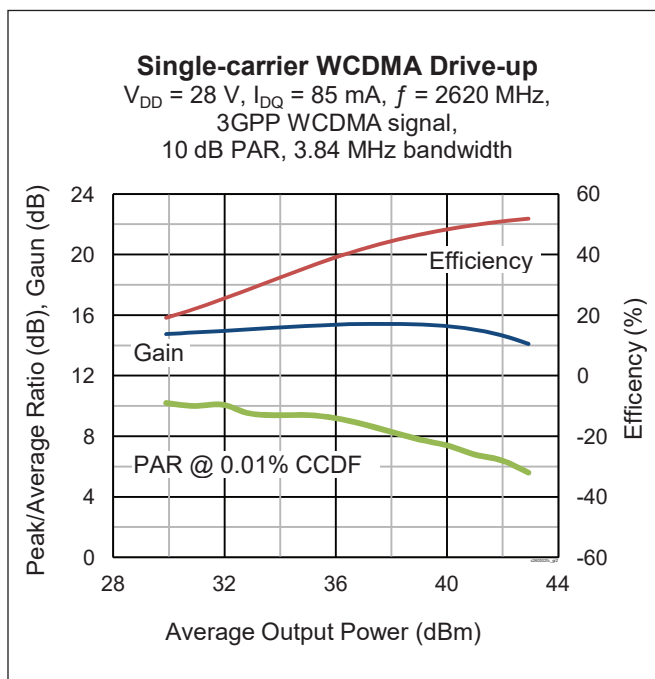


Lead connections for PTAC260302FC

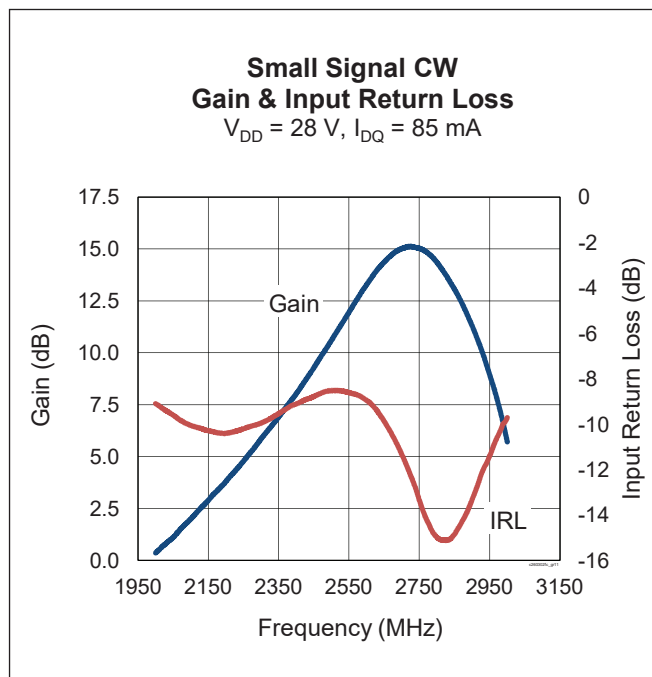
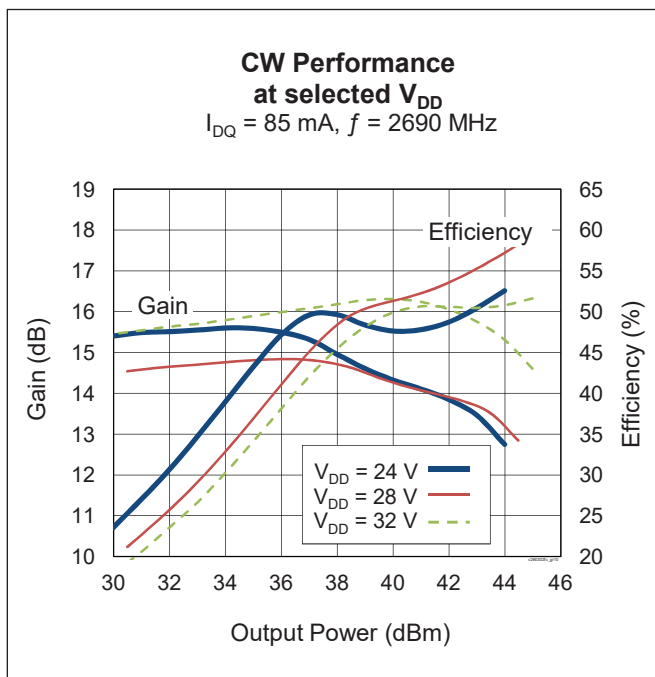
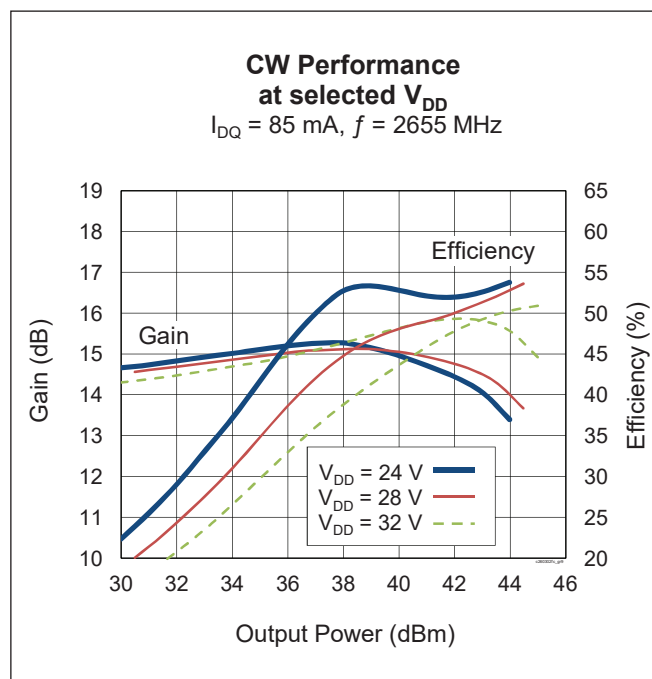
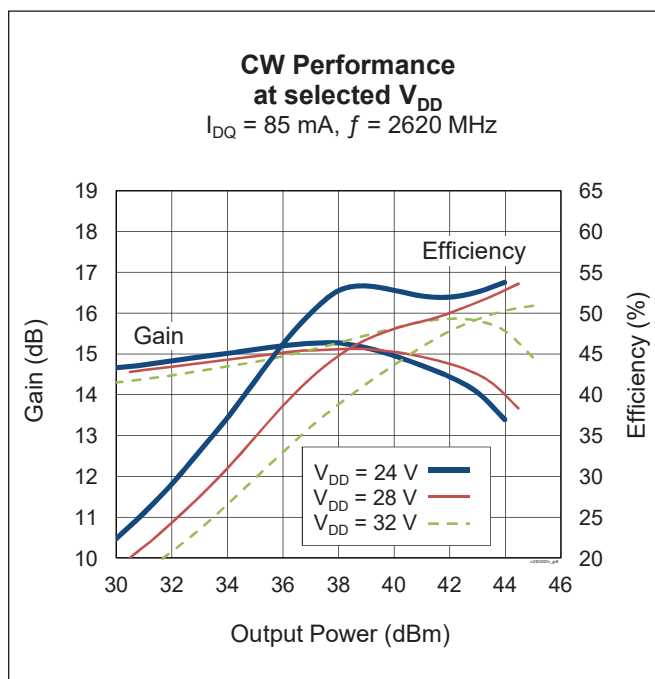
Typical Performance (data taken in a production test fixture)



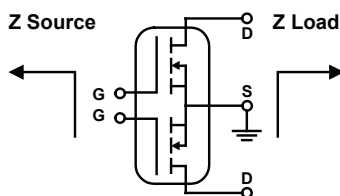
Typical Performance (cont.)



Typical Performance (cont.)



Load Pull Performance



Main Side – Pulsed CW signal: 16 μ sec, 10% duty cycle; 28 V, 85 mA

Class AB		P _{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Z _s Ω	Z _L Ω	Gain [dB]	P _{OUT} [dBm]	P _{OUT} [W]	PAE %	Z _L Ω	Gain [dB]	P _{OUT} [dBm]	P _{OUT} [W]	PAE %
2620	26 – j22	10.9 – j9.7	19.7	42.36	17.2	61.0	5.9 – j7.0	21.6	40.70	11.7	66.4
2655	33 – j32	12.7 – j9.6	20.0	42.45	17.6	59.8	7.1 – j8.1	21.4	41.36	13.7	65.9
2690	55 – j34	15.2 – j11.4	19.3	42.86	19.3	55.1	6.8 – j9.0	21.2	41.33	13.6	64.4

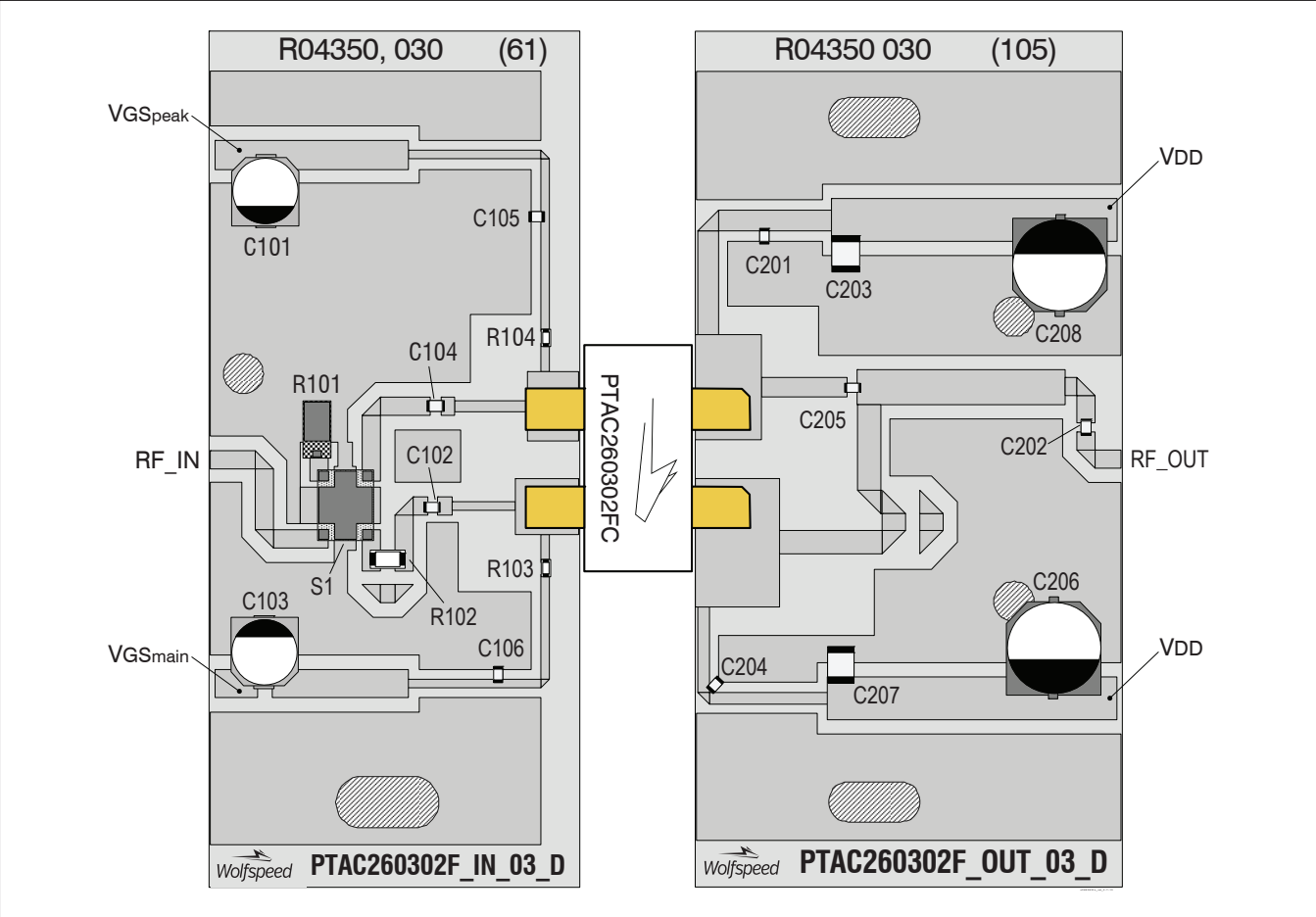
Peak Side – Pulsed CW signal: 16 μ sec, 10% duty cycle; 28 V, 115 mA

Class AB		P _{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Z _s Ω	Z _L Ω	Gain [dB]	P _{OUT} [dBm]	P _{OUT} [W]	PAE %	Z _L Ω	Gain [dB]	P _{OUT} [dBm]	P _{OUT} [W]	PAE %
2620	36 – j41	11.5 – j14.9	19.6	43.11	20.5	58.8	6.4 – j13.4	20.9	41.92	15.6	63.9
2655	42 – j31	11.9 – j12.7	20	43.09	20.4	61.1	7.0 – j13.9	20.8	42.07	16.1	63.2
2690	55 – j33	12.9 – j15.0	19.5	42.87	19.4	57.2	7.8 – j15.1	20.5	42.16	16.4	61.8

Reference Circuit

DUT	PTAC260302FC
Test Fixture Part No.	LTA/PTAC260302FC
PCB	Rogers 4350, 0.762 mm [.030"] thick, 2 oz. copper, $\epsilon_r = 3.66$
Find Gerber files for this test fixture on the Wolfspeed Web site at (http://www.wolfspeed.com/RF)	

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)

Component Information

Component	Description	Suggested Manufacturer	P/N
Input			
C101, C103	Capacitor, 10 μ F, 50 V	Panasonic Electronic Components	EEV-HD1H100P
C102, C104, C105, C106	Chip capacitor, 18 pF	ATC	ATC100A180JW150XB
R101	Resistor, 50 Ohm	Anaren	C16A50Z4
R102	Resistor, 20 Ohm	Panasonic Electronic Components	ERJ-8GEYJ200V
R103, R104	Resistor, 10 Ohm	Panasonic Electronic Components	ERJ-3GEYJ100V
S1	Hybrid coupler	Anaren	X3C25P1_05S
Output			
C201, C202	Chip capacitor, 18 pF	ATC	ATC100A180JW150XB
C203, C207	Capacitor, 10 μ F	Taiyo Yuden	UMK325C7106MM-T
C204, C205	Chip capacitor, 18 pF	ATC	ATC100A180JW150XB
C206, C208	Capacitor, 220 μ F, 35 V	Panasonic Electronic Components	EEE-FP1V221AP

Package Outline Specifications

Package H-37248H-4

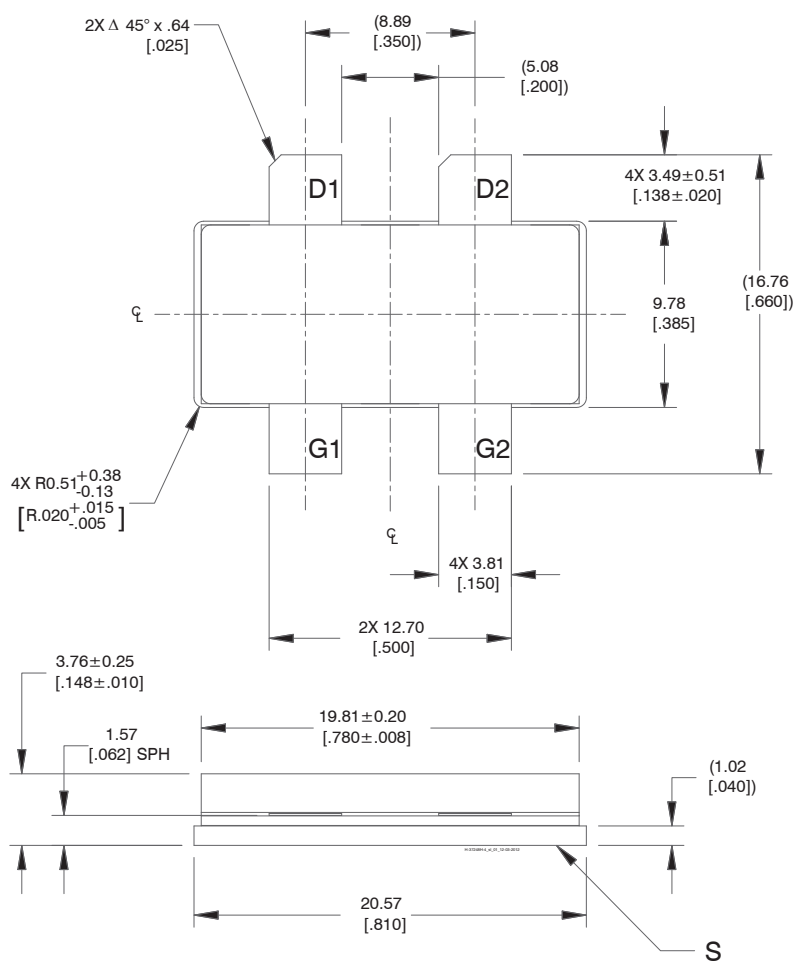


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source.
5. Lead thickness: $0.10 + 0.051/-0.025$ mm [.004 +0.002/-0.001 inch].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2012-03-05	Advance	All	New product, proposed only.
02	2012-11-28	Advance	1,3 2	Updated package and Package Outline. Updated Pinout Diagram.
03	2014-02-12	Production	All 3 – 7	Product released to production. All information updated. Performance graphs, load pull and circuit information added.
04	2016-06-21	Production	1 2	Updated ESD rating Maximum junction temperature raised to 225°C, updated ordering info.
05	2018-07-02	Production	All	Converted to Wolfspeed Data Sheet.

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Notes

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