MOSFET – Dual, N-Channel, Small Signal, Gate ESD Protection, 2x2 WDFN

30 V, 245 mA

Features

- Optimized Layout for Excellent High Speed Signal Integrity
- Low Gate Charge for Fast Switching
- Small 2 x 2 mm Footprint
- ESD Protected Gate
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	30	V
Gate-to-Source Voltage	Gate-to-Source Voltage		±10	V
Continuous Drain Current (Note 1)	Steady State = 25°C	I _D	245	mA
Power Dissipation (Note 1)	Steady State = 25°C	P _D	755	mW
Pulsed Drain Current	t _P ≤ 10 μs	I _{DM}	1.2	Α
Operating Junction and Storage Temperature		T _J , T _{STG}	-55 to 150	°C
Continuous Source Current (Body Diode)		I _{SD}	245	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	166	°C/W

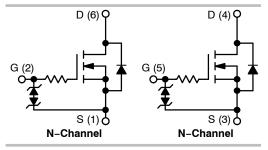
^{1.} Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



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V _{(BR)DSS}	R _{DS(on)} Typ @ V _{GS}	I _D MAX (Note 1)
20.1/	1.4 Ω @ 4.5 V	0.45 1
30 V	2.3 Ω @ 2.5 V	245 mA



MARKING DIAGRAM



WDFN6 CASE 506AN

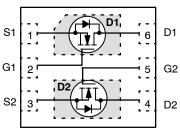


JG = Specific Device Code

M = Date Code

= Pb-Free Package(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping [†]
NVLJD4007NZTAG	WDFN6 (Pb-Free)	3000/Tape & Reel
NVLJD4007NZTBG	WDFN6 (Pb-Free)	3000/Tape & Reel

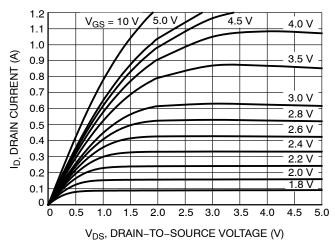
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
OFF CHARACTERISTICS	<u>.</u>					
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 100 \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	Reference to 25°C, $I_D = 100 \mu A$		27		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 30 V			1.0	μА
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 20 V, T = 85 °C			1.0	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 10 \text{ V}$			±25	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$			±1.0	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$ T = 85 °C			±1.0	μΑ
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	V _{GS(TH)}	$V_{DS} = V_{GS}, I_D = 100 \mu A$	0.5	1.0	1.5	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J	Reference to 25°C, I _D = 100 μA		-2.5		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 125 mA		1.4	7.0	
		V _{GS} = 2.5 V, I _D = 125 mA		2.3	7.5	5 Ω
Forward Transconductance	9FS	$V_{DS} = 3 \text{ V, } I_{D} = 125 \text{ mA}$		80		mS
CAPACITANCES & GATE CHARGE						
Input Capacitance	C _{ISS}			12.2	20	
Output Capacitance	C _{OSS}	$V_{DS} = 5.0 \text{ V, f} = 1 \text{ MHz,} $ $V_{GS} = 0 \text{ V}$		10	15	pF
Reverse Transfer Capacitance	C _{RSS}	143 51		3.3	6.0	
Total Gate Charge	Qg			0.75		
Gate-to-Source Charge	Q _{gs}	V _{DS} = 24 V, I _D = 100 mA,		0.20		nC
Gate-to-Drain Charge	Q_{gd}	$V_{DS} = 24 \text{ V}, I_{D} = 100 \text{ mA}, $ $V_{GS} = 4.5 \text{ V}$		0.20		7
Plateau Voltage	V _{GP}	1 – – – – – – – – – – – – – – – – – – –		1.57		V
SWITCHING CHARACTERISTICS (Note 3)	-					
Turn-On Delay Time	t _{d(ON)}			9		ns
Rise Time	t _r	V _{GS} = 4.5 V, V _{DS} = 24 V,		41		ns
Turn-Off Delay Time	t _{d(OFF)}	I_D = 125 mA, R_G = 10 Ω		96		
Fall Time	t _f			72		
DRAIN-SOURCE DIODE CHARACTERISTIC	S					
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 125 mA		0.79	0.9	V

Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

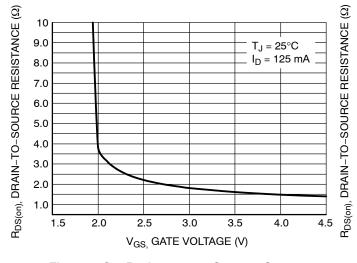
TYPICAL PERFORMANCE CURVES



1.2 $V_{DS} = 5 V$ 1.1 $T_J = 25^{\circ}C$ 1.0 D, DRAIN CURRENT (A) 0.9 0.8 0.7 $T_J = 150^{\circ}C$ 0.6 $T_J = -55^{\circ}C$ 0.5 0.4 0.3 0.2 0.1 0.5 2.0 2.5 1.0 1.5 3.0 3.5 V_{GS}, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



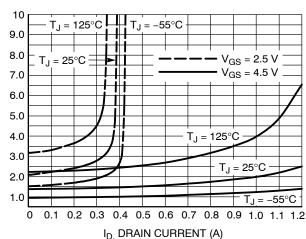
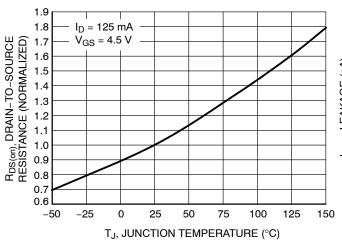


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



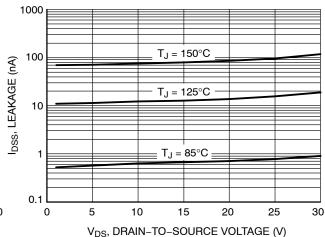
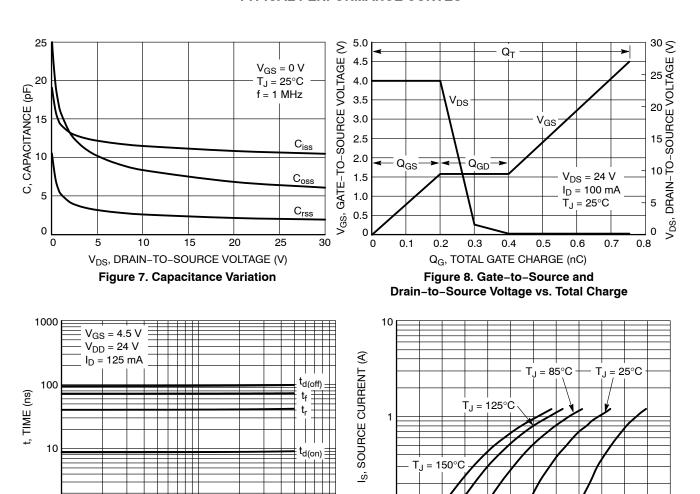


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES



0.1

0.5

0.6

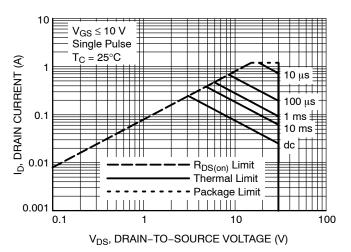
 $\label{eq:RG} \textbf{R}_{\textbf{G}}, \, \textbf{GATE RESISTANCE} \; (\Omega)$ Figure 9. Resistive Switching Time Variation vs. Gate Resistance

10

 $\label{eq:VSD} V_{SD}, \text{SOURCE-TO-DRAIN VOLTAGE (V)} \\ \textbf{Figure 10. Diode Forward Voltage vs. Current}$

-55°C

1.1



100

Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES

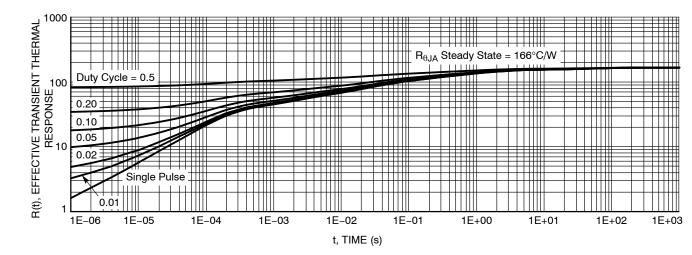
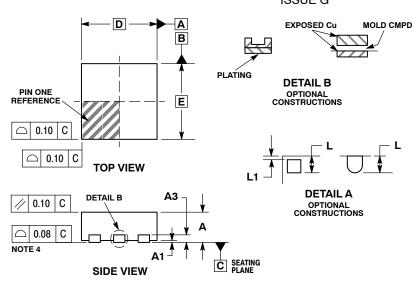


Figure 12. Thermal Impedance (Junction-to-Ambient)

PACKAGE DIMENSIONS

WDFN6 2x2, 0.65P CASE 506AN **ISSUE G**



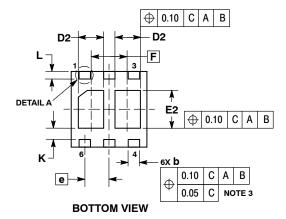
NOTES:

- DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION 6 APPLIES TO PLATED
 TERMINAL AND IS MEASURED BETWEEN
 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
 COPLANARITY APPLIES TO THE EXPOSED
- PAD AS WELL AS THE TERMINALS.

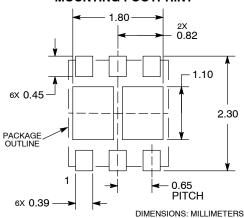
ABAO WELLAO ITIL TEIN			
	MILLIMETERS		
DIM	MIN	MAX	
Α	0.70	0.80	
A1	0.00	0.05	
A3	0.20 REF		
b	0.25	0.35	
D	2.00 BSC		
D2	0.57	0.77	
Е	2.00 BSC		
E2	0.90	1.10	
е	0.65 BSC		
F	0.95 BSC		
K	0.25 REF		
L	0.20	0.30	
L1		0.10	

STYLE 3: PIN 1

- SOURCE 1
- GATE 1 2.
- 3. SOURCE 2 DRAIN 2
- GATE 2 5.



SOLDERMASK DEFINED **MOUNTING FOOTPRINT**



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