

N-channel 20 V, 0.025 Ω typ., 5 A STripFET™ V Power MOSFET in a SOT23-6L package

Datasheet — production data

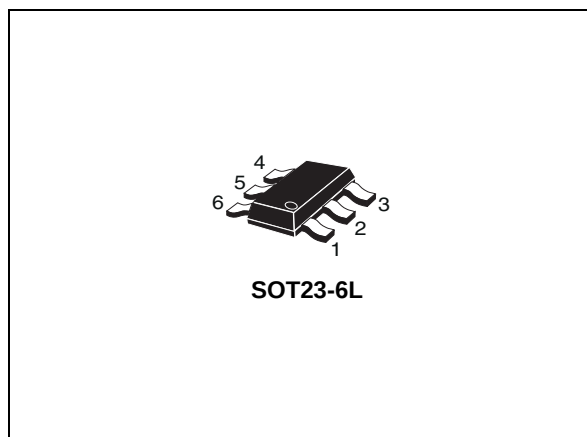
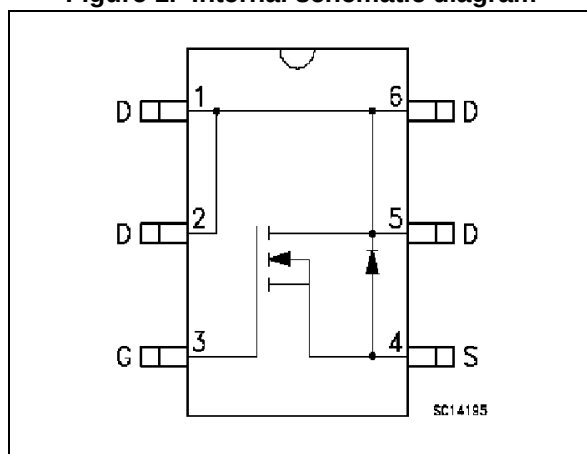


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STT5N2VH5	20 V	0.04 Ω ($V_{GS}=2.5$ V)	5 A	1.6 W

- Very low profile package
- Conduction losses reduced
- Switching losses reduced
- 2.5 V gate drive
- Very low threshold device

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to a FOM that is among the best in its class.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STT5N2VH5	STD1	SOT23-6L	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate-source voltage	± 8	V
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	5	A
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	3.1	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	20	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	1.6	W
T_{stg}	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
T_j	Max. operating junction temperature		$^{\circ}\text{C}$

1. This value is rated according to $R_{thj-pcb}$

2. Pulse width is limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	78	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz Cu, $t < 10\text{ sec.}$

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	20			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 20\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$			10	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 8\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	0.7			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 4.5\text{ V}$, $I_D = 2\text{ A}$		0.025	0.03	Ω
		$V_{GS} = 2.5\text{ V}$, $I_D = 2\text{ A}$		0.031	0.04	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 16\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	367	-	pF
C_{oss}	Output capacitance		-	92	-	pF
C_{rss}	Reverse transfer capacitance		-	16	-	pF
Q_g	Total gate charge	$V_{DD} = 16\text{ V}$, $I_D = 2\text{ A}$, $V_{GS} = 4.5\text{ V}$ (see Figure 14)	-	4.6	-	nC
Q_{gs}	Gate-source charge		-	0.9	-	nC
Q_{gd}	Gate-drain charge		-	1	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Voltage delay time	$V_{DD} = 16\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 4.5\text{ V}$ (see Figure 15 and Figure 18)	-	4.8	-	ns
$t_r(v)$	Voltage rise time		-	14.4	-	ns
$t_d(off)$	Current fall time		-	17	-	ns
t_f	Crossing time		-	4	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2\text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 16\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 18)	-	10		ns
Q_{rr}	Reverse recovery charge		-	24		nC
I_{RRM}	Reverse recovery current		-	4.8		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

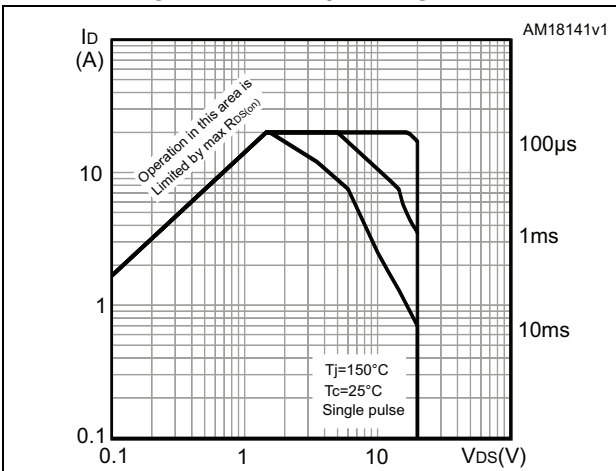


Figure 3. Thermal impedance

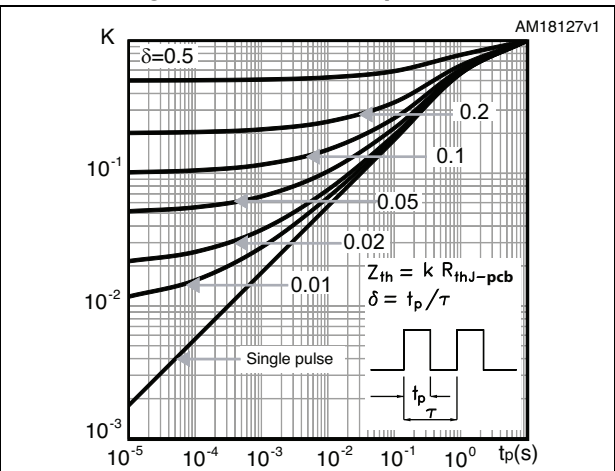


Figure 4. Output characteristics

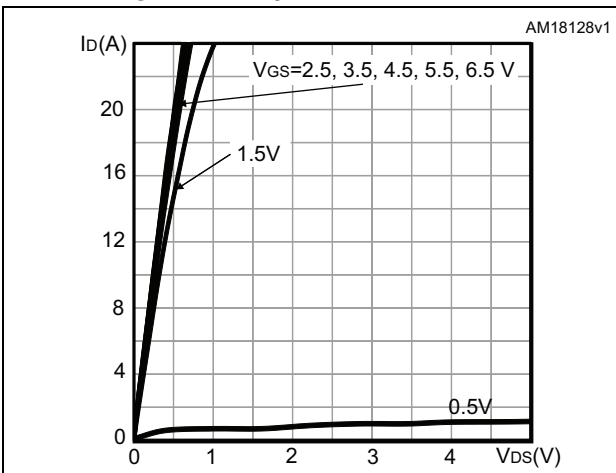


Figure 5. Transfer characteristics

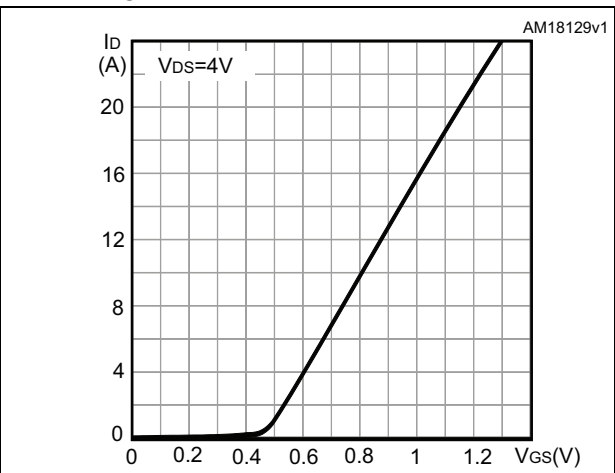


Figure 6. Gate charge vs gate-source voltage

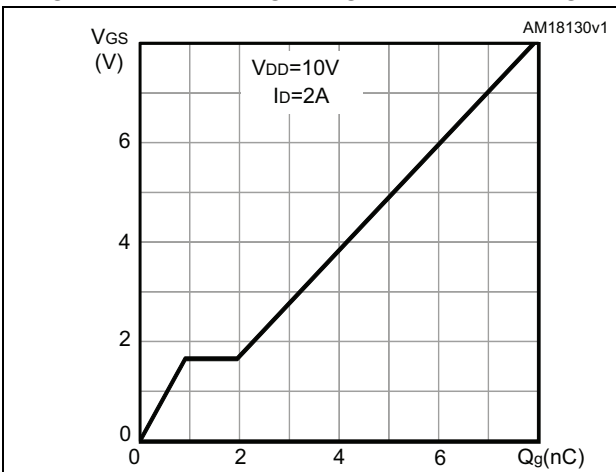


Figure 7. Static drain-source on-resistance

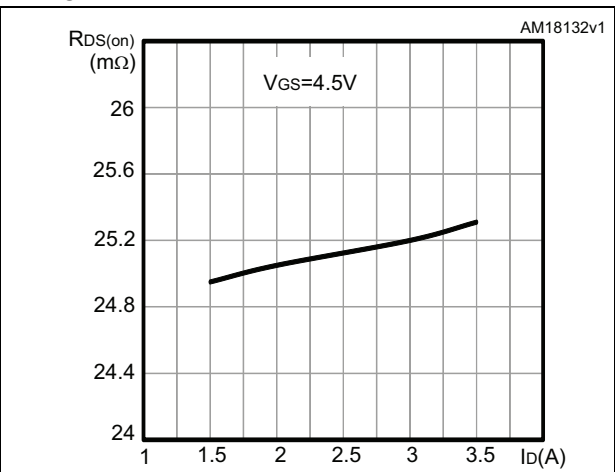


Figure 8. Capacitance variations

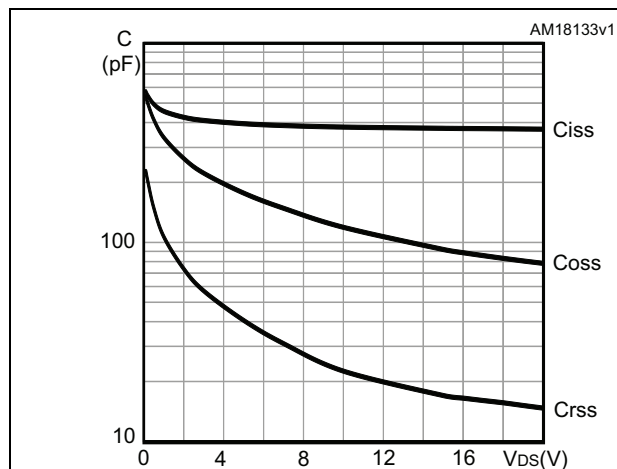


Figure 9. Normalized gate threshold voltage vs temperature

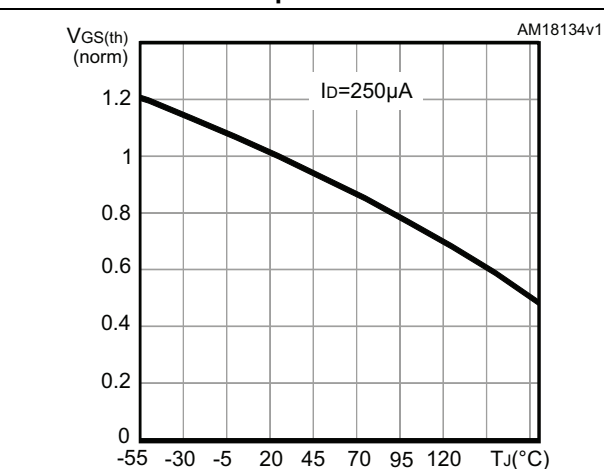


Figure 10. Normalized on-resistance vs temperature

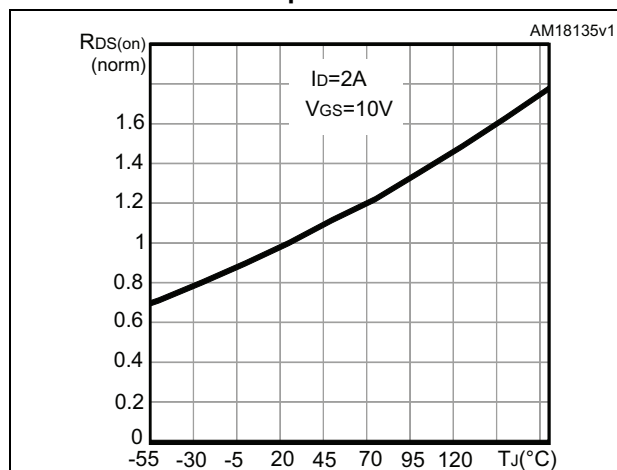
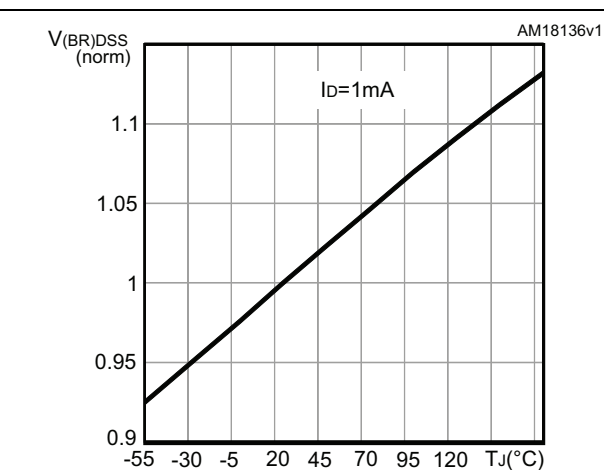
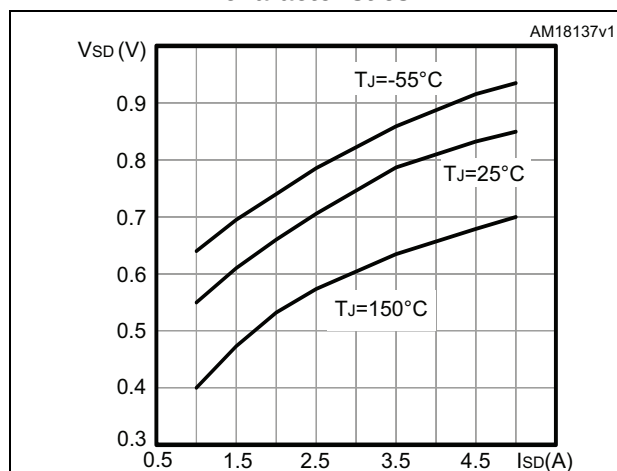
Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

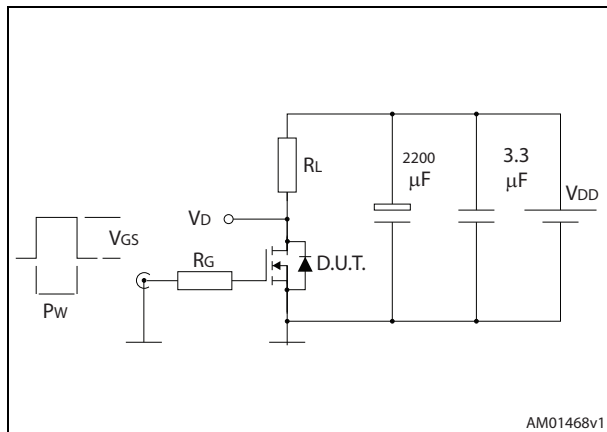


Figure 14. Gate charge test circuit



Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped inductive load test circuit



Figure 17. Unclamped inductive waveform



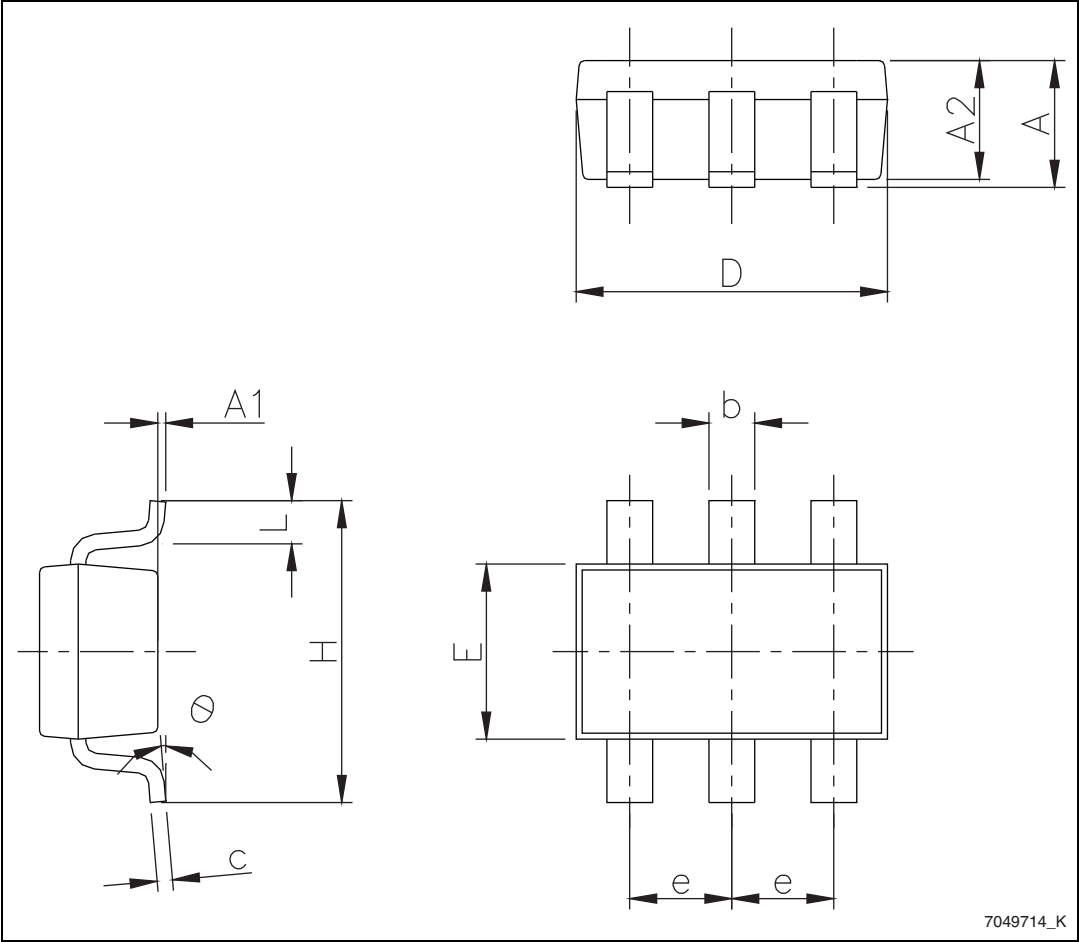
Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. SOT23-6L package drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-Mar-2014	1	First release. Part number previously included in datasheet DocID023799

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