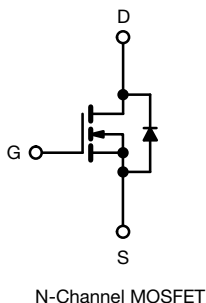
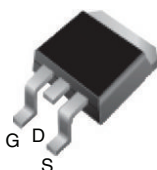


## Power MOSFET

**D<sup>2</sup>PAK (TO-263)**


### FEATURES

- Low gate charge  $Q_g$  results in simple drive requirement
- Improved gate, avalanche and dynamic  $dV/dt$  ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS\***  
Available  
**HALOGEN**  
**FREE**  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

### APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

### APPLICABLE OFF LINE SMPS TOPOLOGIES

- Active clamped forward
- Main switch

### PRODUCT SUMMARY

$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.75
$Q_g$ max. (nC)	49	
$Q_{gs}$ (nC)	13	
$Q_{gd}$ (nC)	20	
Configuration	Single	

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHFS9N60A-GE3	SiHFS9N60ATTR-GE3 <sup>a</sup>	SiHFS9N60ATRL-GE3 <sup>a</sup>
Lead (Pb)-free	IRFS9N60APbF	IRFS9N60ATTRPbF <sup>a</sup>	IRFS9N60ATRLPbF <sup>a</sup>

### Note

a. See device orientation

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	600	V
Gate-Source Voltage			V <sub>GS</sub>	± 30	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	9.2	A
		T <sub>C</sub> = 100 °C		5.8	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	37	
Linear Derating Factor				1.3	W/°C
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	290	mJ
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	9.2	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	17	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	170	W
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering Recommendations (Peak temperature) <sup>d</sup>	for 10 s			300	


### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 6.8\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 9.2\text{ A}$  (see fig. 12)
- $I_{SD} \leq 9.2\text{ A}$ ,  $dI/dt \leq 50\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.75	

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

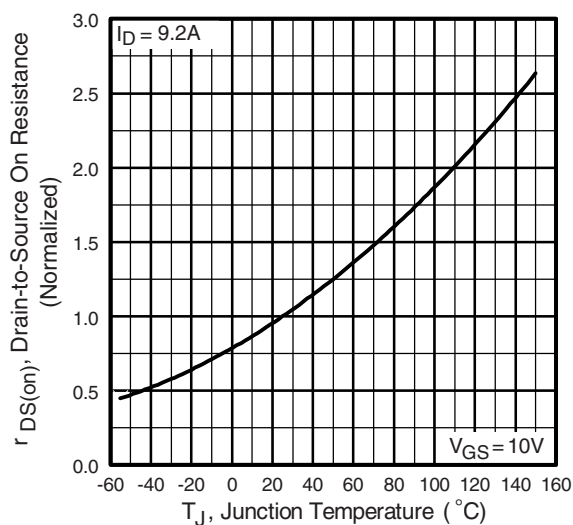
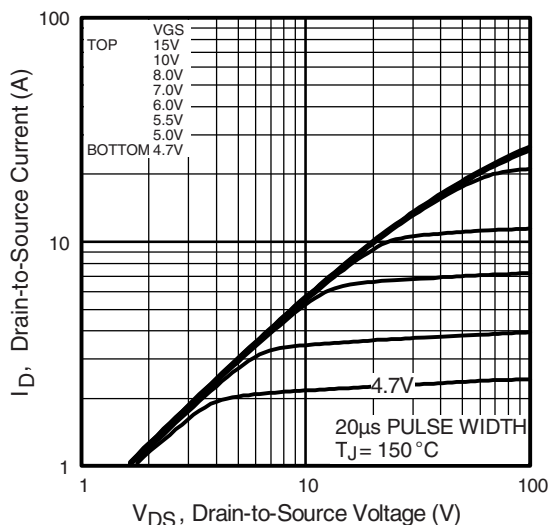
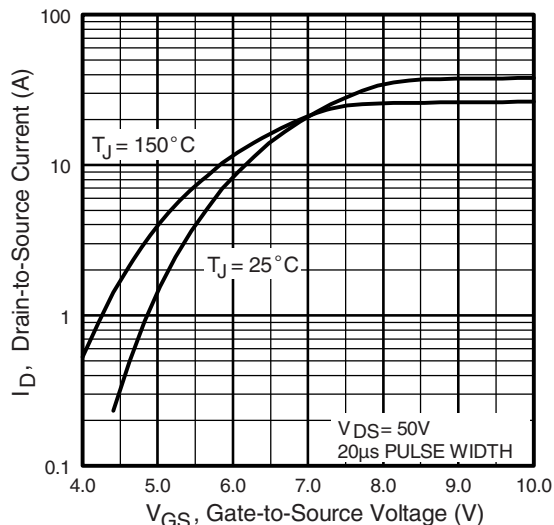
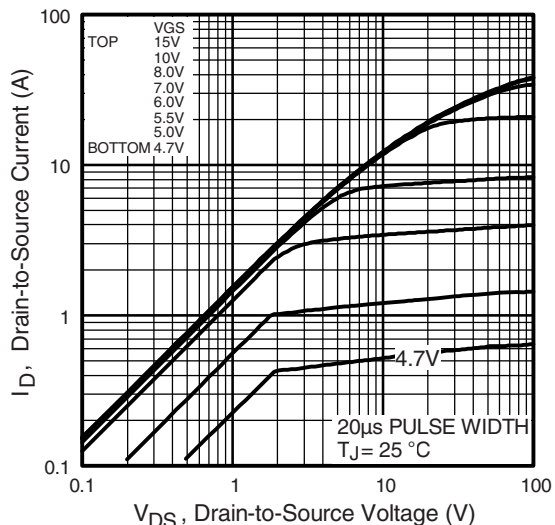
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$ , $I_D = 1\text{ mA}$	-	0.66	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}^b$	-	-	0.75	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 25\text{ V}, I_D = 3.1\text{ A}$	5.5	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$ , see fig. 5	-	1400	-	pF
Output Capacitance	$C_{oss}$		-	180	-	
Reverse Transfer Capacitance	$C_{rss}$		-	7.1	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$ $V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$ $V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$ $V_{DS} = 0\text{ V to } 480\text{ V}^c$	-	1957	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		-	49	-	nC
Total Gate Charge	$Q_g$		-	-	49	
Gate-Source Charge	$Q_{gs}$	$V_{GS} = 10\text{ V}$ $I_D = 9.2\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	13	
Gate-Drain Charge	$Q_{gd}$		-	-	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 9.2\text{ A}$ $R_g = 9.1\text{ }\Omega, R_D = 35.5\text{ }\Omega,$ see fig. 10 <sup>b</sup>	-	13	-	ns
Rise Time	$t_r$		-	25	-	
Turn-Off Delay Time	$t_{d(off)}$		-	30	-	
Fall Time	$t_f$		-	22	-	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}$ , open drain	0.5	-	3.2	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	9.2	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	37	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^{\circ}\text{C}, I_S = 9.2\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^{\circ}\text{C}, I_F = 9.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	530	800	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	3.0	4.4	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

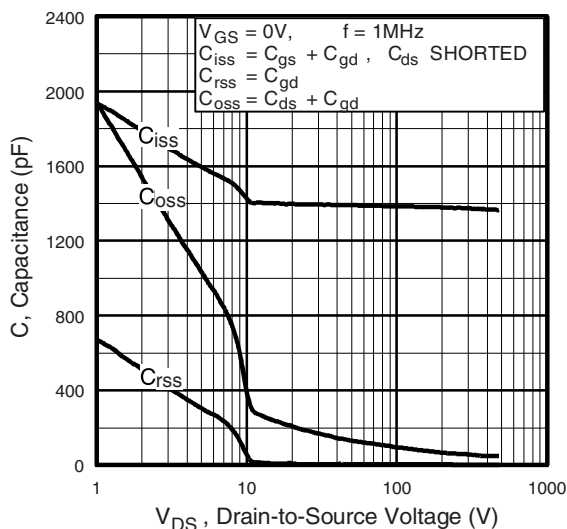
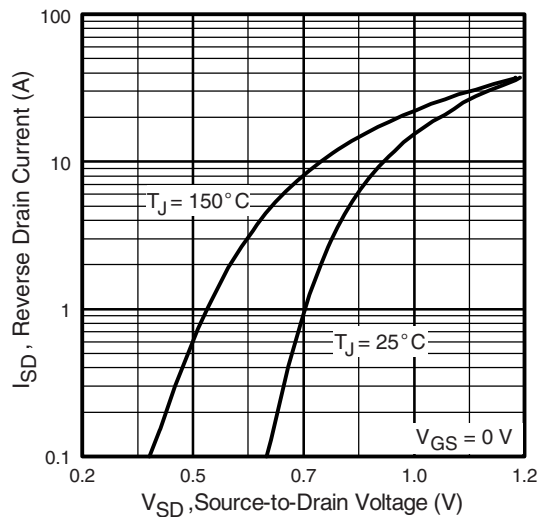
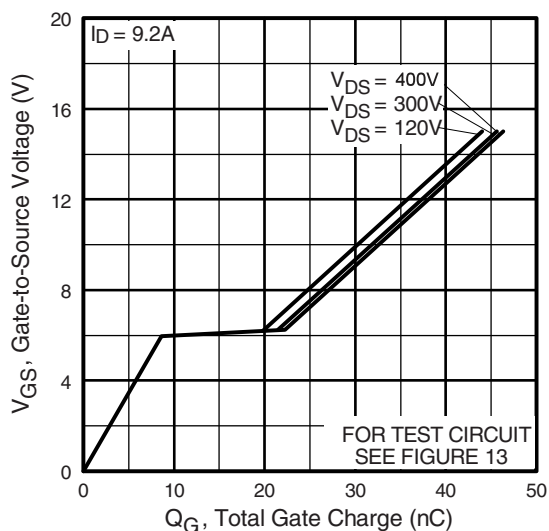
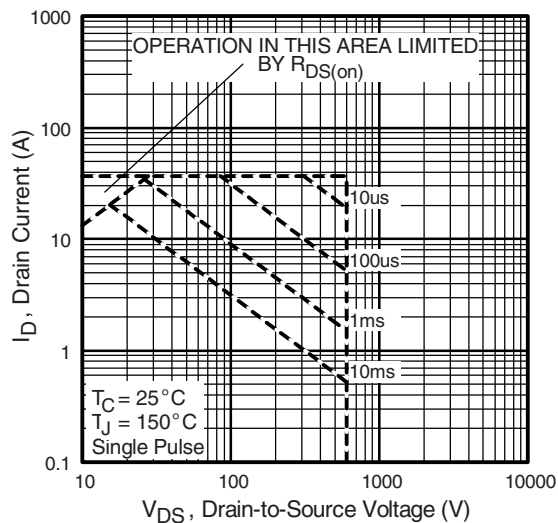
**Notes**

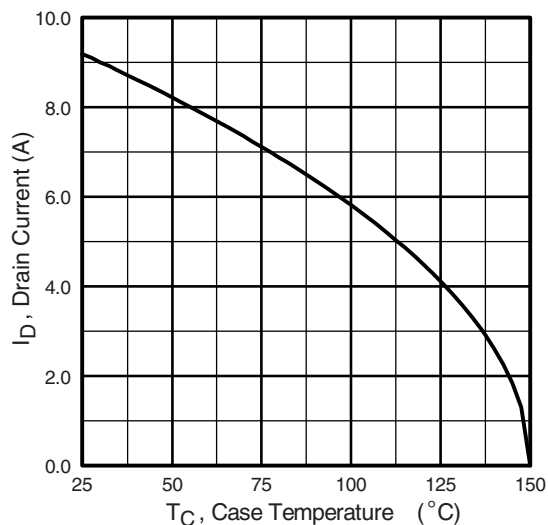
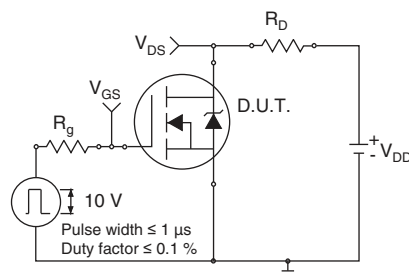
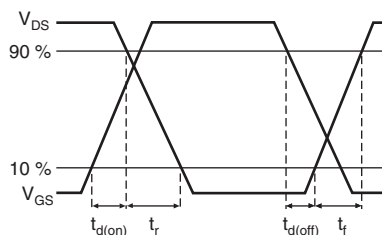
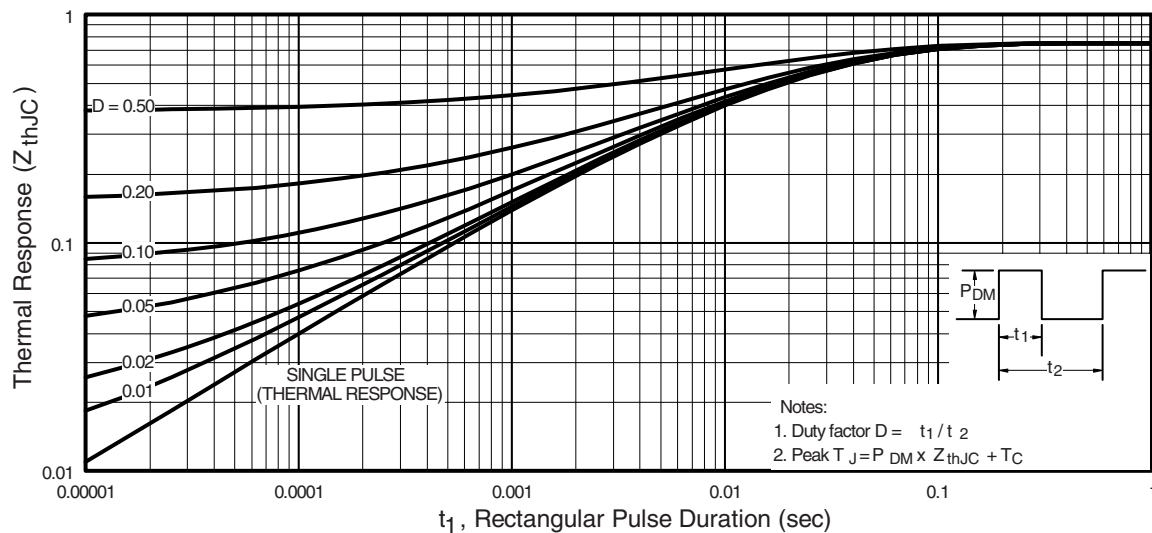
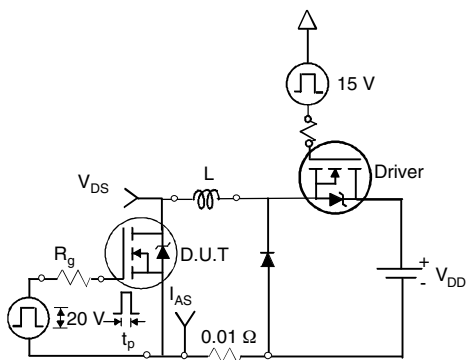
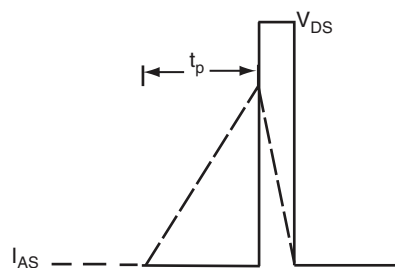
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$   
c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$

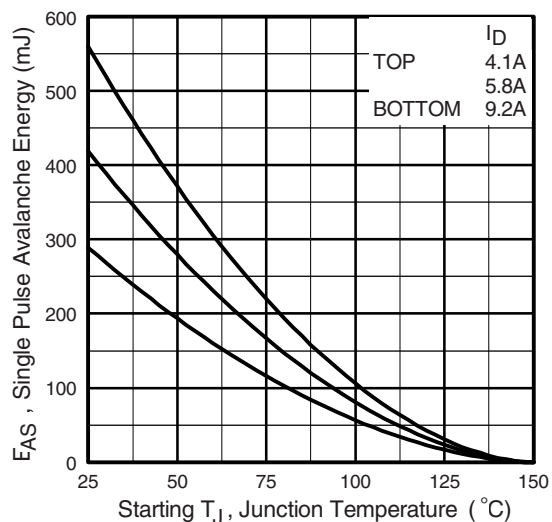


**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

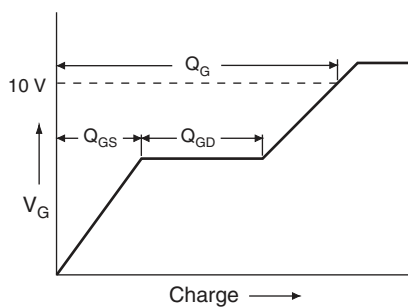



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 1 - Maximum Safe Operating Area**

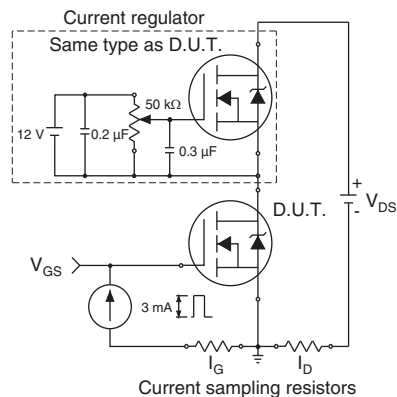

**Fig. 8 - Maximum Drain Current vs. Case Temperature**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**



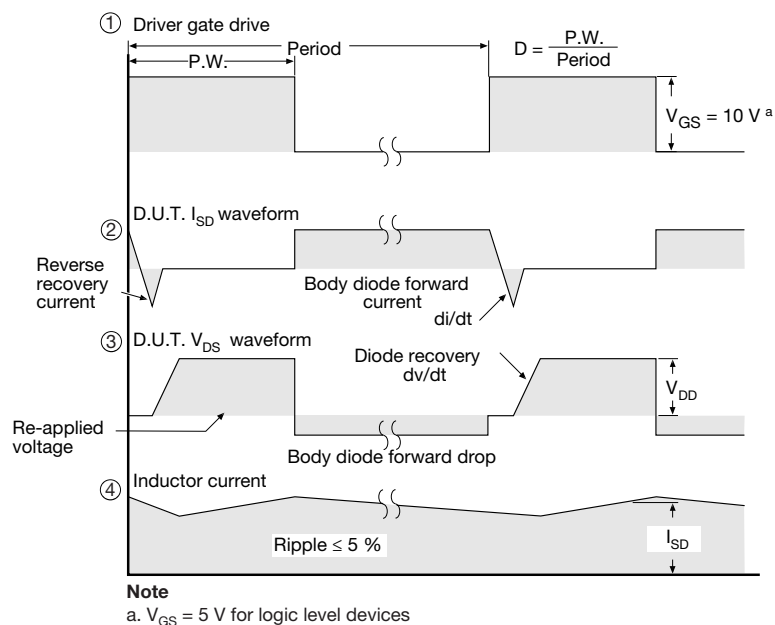
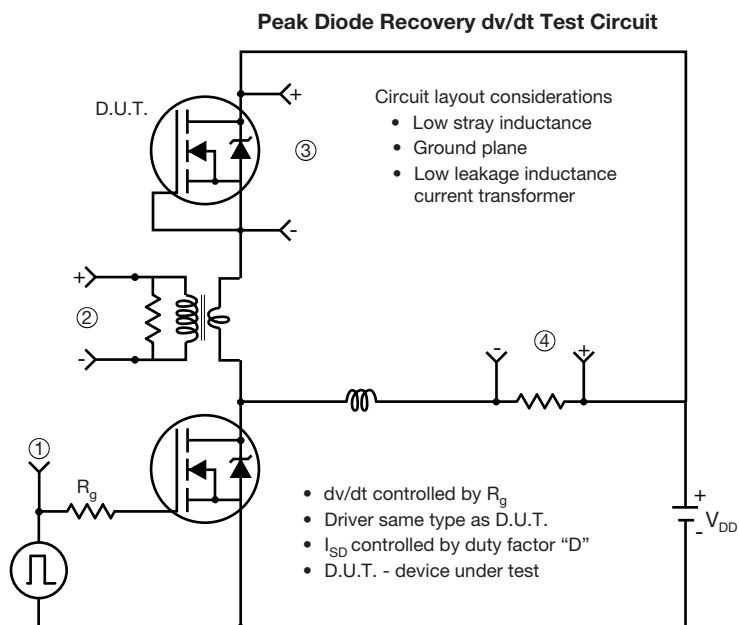
**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**



**Fig. 13a - Basic Gate Charge Waveform**



**Fig. 13b - Gate Charge Test Circuit**



**Fig. 14 - For N-Channel**

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	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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