

2 OUTPUT PCIE GEN1/2 SYNTHESIZER

IDT5V41285

Recommended Applications

2 output synthesizer for PCIe Gen1/2 and Ethernet

General Description

The IDT5V41285 is a PCIe Gen2 compliant clock generator. The device has 2 differential HCSL outputs. The output frequency is selectable via select pins.

Output Features

- 2 - Non-spread 0.7V current mode differential HCSL output pairs

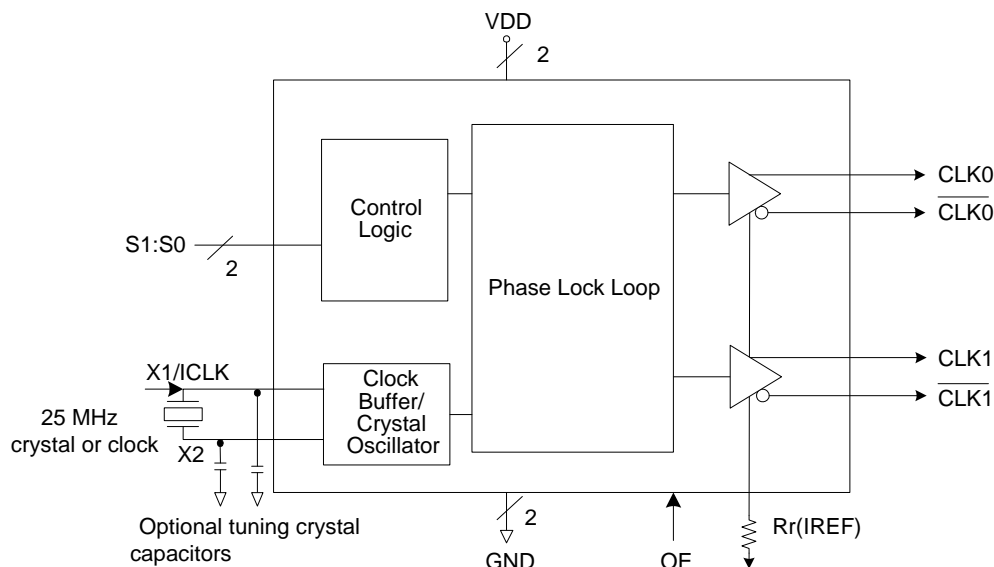
Features/Benefits

- 16-pin TSSOP and VFQFPN packages; small board footprint
- Outputs can be terminated to LVDS; can drive a wider variety of devices
- OE control pin; greater system power management
- Industrial temperature range available; supports demanding embedded applications
- **For PCIe Gen3 applications, see the IDT5V41315**

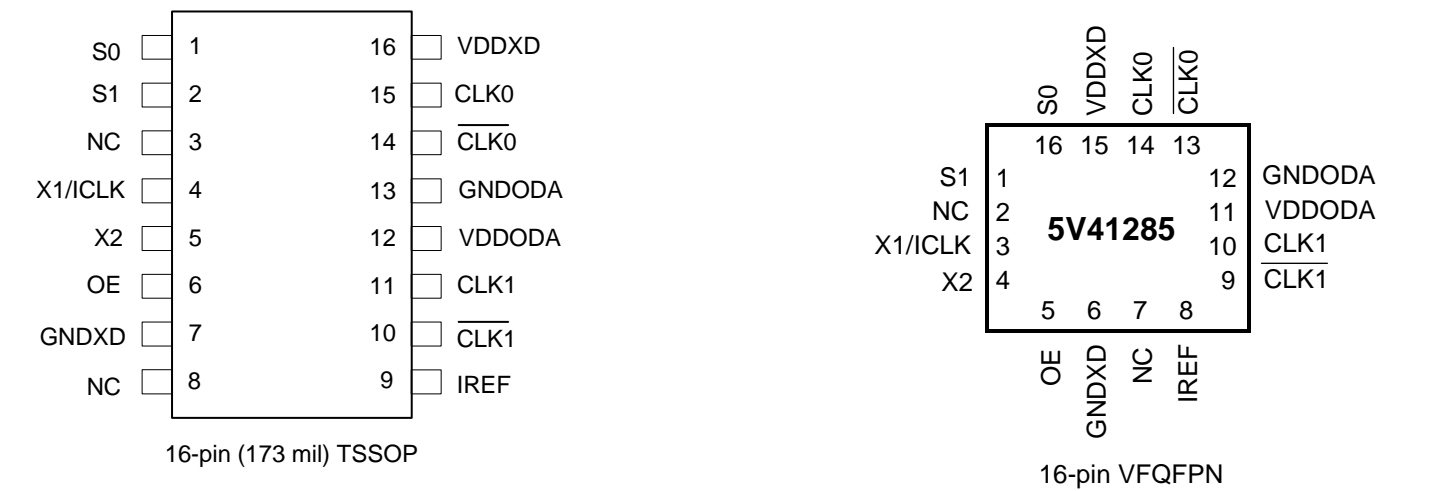
Key Specifications

- Cycle-to-cycle jitter: 80ps
- Output-to-output skew <50 ps
- PCIe Gen2 phase jitter <3.0ps RMS
- Low phase noise: 12kHz to 20MHz <6ps

Block Diagram



Pin Assignment



Output Select Table 1 (MHz)

| S1 | S0 | CLK(1:0), CLK(1:0) |
|----|----|--------------------|
| 0 | 0 | 25M |
| 0 | 1 | 100M |
| 1 | 0 | 125M |
| 1 | 1 | 200M |

Pin Descriptions

| VFQFP Pin Number | TSSOP Pin Number | Pin Name | Pin Type | Pin Description |
|------------------------|------------------------|-------------|-------------|---|
| 16 | 1 | S0 | Input | Select pin 0. See Output Select Table 1. Internal pull-up resistor. |
| 1 | 2 | S1 | Input | Select pin 1. See Output Select Table 1. Internal pull-up resistor. |
| 2 | 3 | NC | – | No connect. |
| 3 | 4 | X1/ICLK | Input | Crystal or clock input. Connect to a 25 MHz crystal or single ended clock. |
| 4 | 5 | X2 | Output | Crystal connection. Leave unconnected for clock input. |
| 5 | 6 | OE | Input | Output enable. Tri-states outputs and device is not shut down. Internal pull-up resistor. |
| 6 | 7 | GNDXD | Power | Connect to ground. |
| 7 | 8 | NC | – | No connect. |
| 8 | 9 | IREF | Output | Precision resistor attached to this pin is connected to the internal current reference. |
| 9 | 10 | CLK1 | Output | HCSL complementary clock output 1. |
| 10 | 11 | CLK1 | Output | HCSL true clock output 1. |
| 11 | 12 | VDDODA | Power | Connect to voltage supply +3.3 V for output driver and analog circuits |
| 12 | 13 | GNDODA | Power | Connect to ground. |
| 13 | 14 | CLK0 | Output | HCSL complementary clock output 0. |
| 14 | 15 | CLK0 | Output | HCSL true clock output 0. |
| 15 | 16 | VDDXD | Power | Connect to voltage supply +3.3 V for crystal oscillator and digital circuit. |

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 μF should be connected between each VDD pin and the ground plane, as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into ICS pin.

Crystal

A 25 MHz fundamental mode parallel resonant crystal should be used. This crystal must have less than 300 ppm of error across temperature in order for the IDT5V41285 to meet PCI Express specifications.

Crystal Capacitors

Crystal capacitors are connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

C_L = Crystal's load capacitance in pF

Crystal Capacitors (pF) = $(C_L - 8) * 2$

For example, for a crystal with a 16 pF load cap, each external crystal cap would be 16 pF. $(16-8)*2=16$.

Current Source (Iref) Reference Resistor - R_R

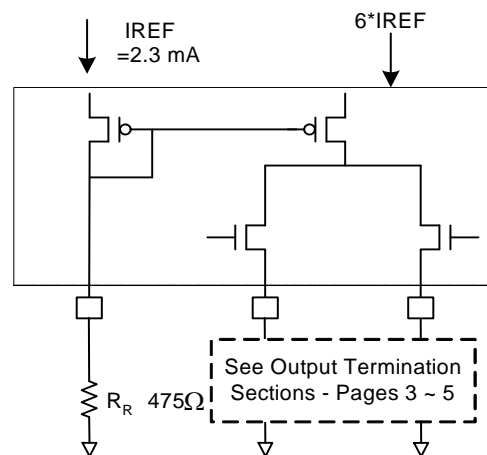
If board target trace impedance (Z) is 50 Ω , then $R_R = 475\Omega$ (1%), providing IREF of 2.32 mA. The output current (I_{OH}) is equal to 6*IREF.

Output Termination

The PCI-Express differential clock outputs of the IDT5V41285 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The IDT5V41285 can also be configured for LVDS compatible voltage levels. See the **LVDS Compatible Layout Guidelines** section.

Output Structures



General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01 μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.
2. No vias should be used between decoupling capacitor and VDD pin.
3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.
4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the IDT5V41285. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Layout Guidelines

| SRC Reference Clock | | | |
|---|--|--------------------|------|
| Common Recommendations for Differential Routing | | Dimension or Value | Unit |
| L1 length, route as non-coupled 50ohm trace | | 0.5 max | inch |
| L2 length, route as non-coupled 50ohm trace | | 0.2 max | inch |
| L3 length, route as non-coupled 50ohm trace | | 0.2 max | inch |
| Rs | | 33 | ohm |
| Rt | | 49.9 | ohm |

| Down Device Differential Routing | | | |
|--|--|---------------------|------|
| L4 length, route as coupled microstrip 100ohm differential trace | | 2 min to 16 max | inch |
| L4 length, route as coupled stripline 100ohm differential trace | | 1.8 min to 14.4 max | inch |

| Differential Routing to PCI Express Connector | | | |
|--|--|-----------------------|------|
| L4 length, route as coupled microstrip 100ohm differential trace | | 0.25 to 14 max | inch |
| L4 length, route as coupled stripline 100ohm differential trace | | 0.225 min to 12.6 max | inch |

Figure 1: Down Device Routing

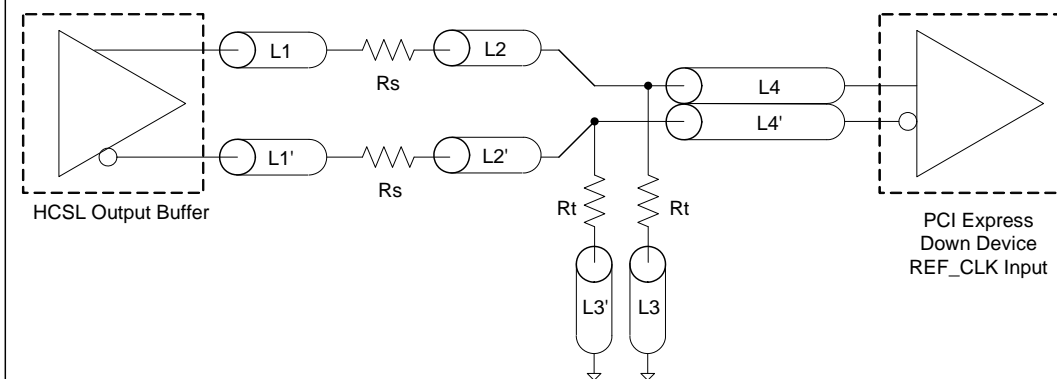
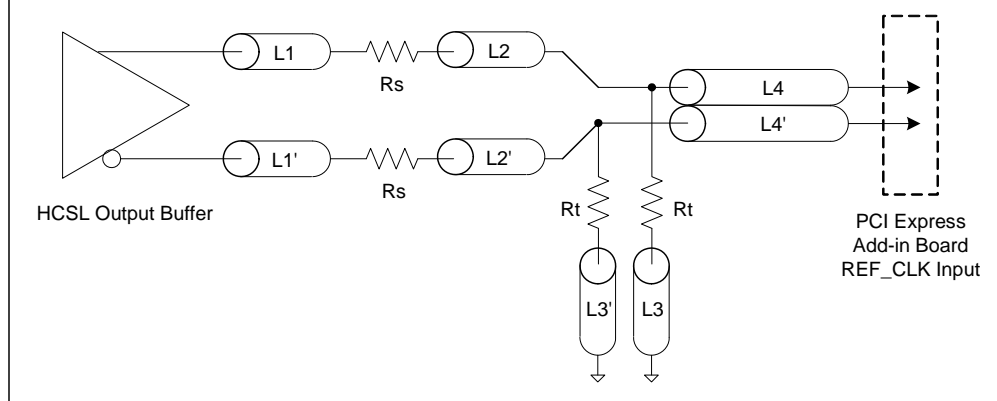


Figure 2: PCI Express Connector Routing

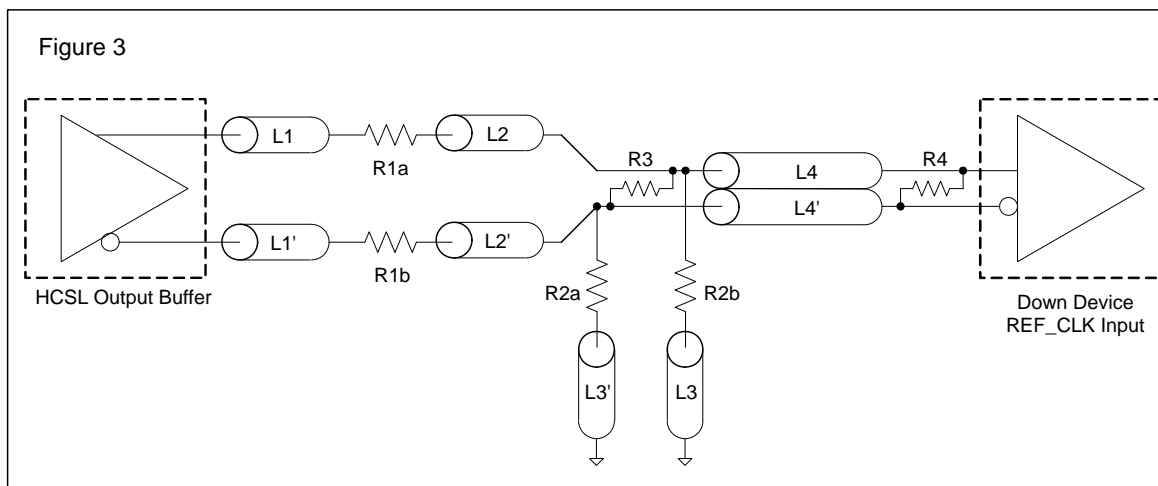


Alternative Termination for LVDS and other Common Differential Signals (figure 3)

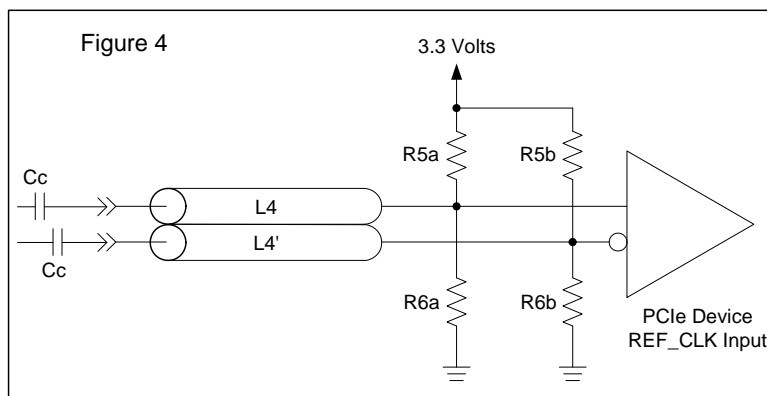
| V _{diff} | V _{p-p} | V _{cm} | R1 | R2 | R3 | R4 | Note |
|-------------------|------------------|-----------------|----|------|------|-----|--------------------------------|
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

R1a = R1b = R1

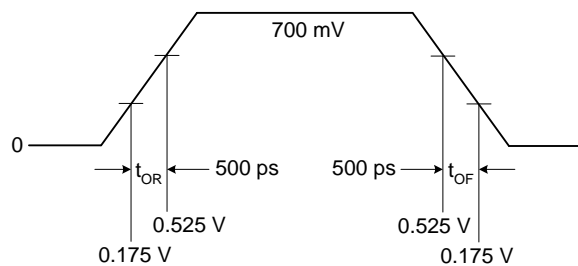
R2a = R2b = R2

**Cable Connected AC Coupled Application (figure 4)**

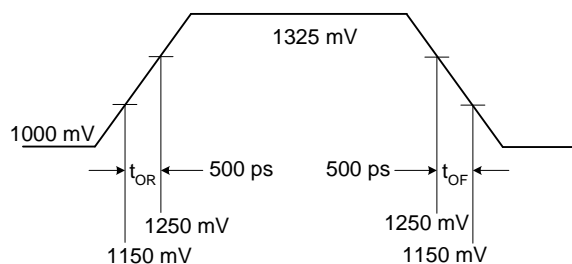
| Component | Value | Note |
|-----------------|-------------|------|
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| V _{cm} | 0.350 volts | |



Typical PCI-Express (HCSL) Waveform



Typical LVDS Waveform



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V41285. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDDXD, VDDODA | 4.6 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (commercial) | 0 to +70°C |
| Ambient Operating Temperature (industrial) | -40 to +85°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |
| ESD Protection (Input) | 2000 V min. (HBM) |

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------------|-------------------|--|---------|------|----------|-------|
| Supply Voltage | V | | 3.135 | 3.3 | 3.465 | V |
| Input High Voltage ¹ | V _{IH} | S0, S1, OE, ICLK | 2.2 | | VDD +0.3 | V |
| Input Low Voltage ¹ | V _{IL} | S0, S1, OE, ICLK | VSS-0.3 | | 0.8 | V |
| Input Leakage Current ² | I _{IL} | 0 < V _{in} < VDD | -5 | | 5 | μA |
| Operating Supply Current @ 100 MHz | I _{DD} | R _S =33Ω, R _P =50Ω, C _L =2 pF | | 63 | 85 | mA |
| | I _{DDOE} | OE =Low | | 42 | 50 | mA |
| Input Capacitance | C _{IN} | Input pin capacitance | | | 7 | pF |
| Output Capacitance | C _{OUT} | Output pin capacitance | | | 6 | pF |
| X1, X2 Capacitance | C _{INX} | | | | 5 | pF |
| Pin Inductance | L _{PIN} | | | | 5 | nH |
| Output Impedance | Z _O | CLK outputs | 3.0 | | | kΩ |
| Pull-up Resistor | R _{PU} | S0, S1, OE | | 100 | | kΩ |

1. Single edge is monotonic when transitioning through region.
2. Inputs with pull-ups/-downs are not included.

AC Electrical Characteristics - CLK0/CLK1, CLK0/CLK1

Unless stated otherwise, VDD=3.3 V \pm 5%, Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---------------------|--------------------------|------|------|------|-------|
| Input Frequency | | | | 25 | | MHz |
| Output Frequency | | HCSL termination | 25 | | 200 | MHz |
| | | LVDS termination | 25 | | 100 | MHz |
| Output High Voltage ^{1,2} | V _{OH} | HCSL | | | 850 | mV |
| Output Low Voltage ^{1,2} | V _{OL} | HCSL | -150 | | | mV |
| Crossing Point Voltage ^{1,2} | | Absolute | 250 | | 550 | mV |
| Crossing Point Voltage ^{1,2,4} | | Variation over all edges | | | 140 | mV |
| Jitter, Cycle-to-Cycle ^{1,3} | | | | | 80 | ps |
| Frequency Synthesis Error | | All outputs | | 0 | | ppm |
| Rise Time ^{1,2} | t _{OR} | From 0.175 V to 0.525 V | 175 | | 700 | ps |
| Fall Time ^{1,2} | t _{OF} | From 0.525 V to 0.175 V | 175 | | 700 | ps |
| Rise/Fall Time Variation ^{1,2} | | | | | 125 | ps |
| Output to Output Skew | | | | | 50 | ps |
| Duty Cycle ^{1,3} | | | 45 | | 55 | % |
| Output Enable Time ⁵ | | All outputs | | 50 | 100 | ns |
| Output Disable Time ⁵ | | All outputs | | 50 | 100 | ns |
| Stabilization Time | t _{STABLE} | From power-up VDD=3.3 V | | | 1.8 | ms |

Note 1: Test setup is R_S=33Ω, R_P=50Ω with C_L=2 pF, R_r = 475Ω (1%).

Note 2: Measurement taken from a single-ended waveform.

Note 3: Measurement taken from a differential waveform.

Note 4: Measured at the crossing point where instantaneous voltages of both CLK and $\overline{\text{CLK}}$ are equal.

Note 5: CLK pins are tri-stated when OE is low asserted. CLK is driven differential when OE is high.

Electrical Characteristics - Differential Phase Jitter

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---------------|-------------------------|---|-----|-----|-----|----------|-------|
| Jitter, Phase | t _{jphasePLL} | PCIe Gen1 | | 32 | 86 | ps (p-p) | 1,2 |
| | t _{jphaseLO} | PCIe Gen2, 10 kHz < f < 1.5 MHz | | 0.8 | 3 | ps (RMS) | 1,2 |
| | t _{jphaseHIGH} | PCIe Gen2, 1.5 MHz < f < Nyquist (50 MHz) | | 2.3 | 3.1 | ps (RMS) | 1,2 |

Note 1. Guaranteed by design and characterization, not 100% tested in production.

Note 2. See <http://www.pcisig.com> for complete specs.

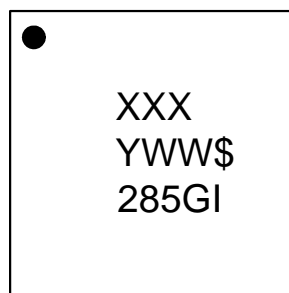
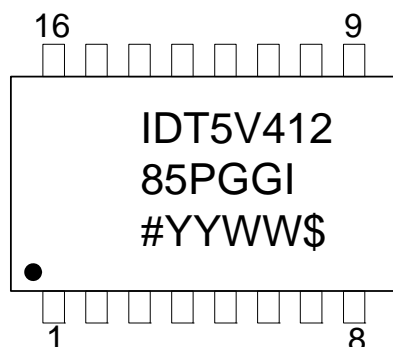
Thermal Characteristics (16-TSSOP)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 78 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 70 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 68 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 37 | | °C/W |

Thermal Characteristics (16-VFQFPN)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 63.2 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 55.9 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 51.4 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 65.8 | | °C/W |

Marking Diagrams

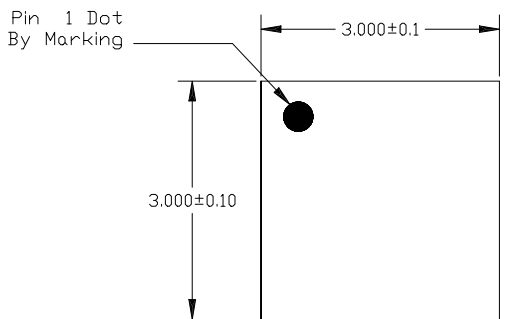


Notes:

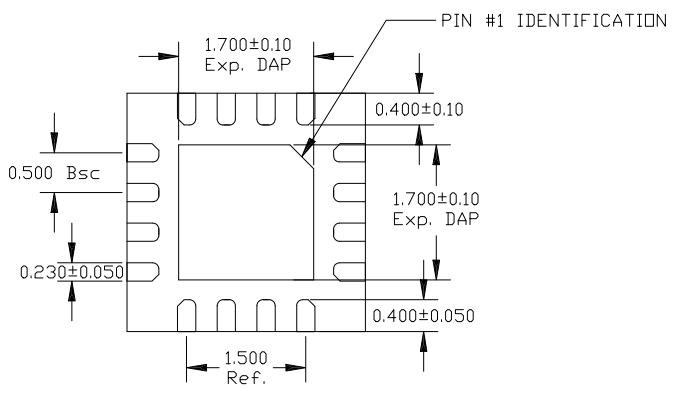
1. Line 1 and 2: IDT part number.
2. Line 3: # – Die revision; YYWW – Date code; \$–Assembly location.
3. “G” after the two-letter package code designates RoHS compliant package.
4. “I” at the end of part number indicates industrial temperature range.
5. Bottom marking: country of origin if not USA (TSSOP only).

Package Outline and Dimensions (3 x 3mm 16-VFQFPN)

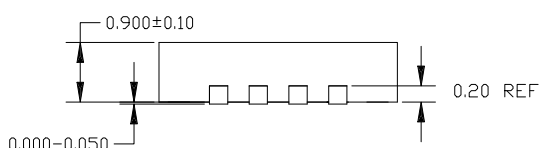
| REVISIONS | | | |
|-----------|----------------------------|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/15/08 | RC |
| 01 | COMBINE POD & LAND PATTERN | 9/17/13 | KS |



TOP VIEW




BOTTOM VIEW



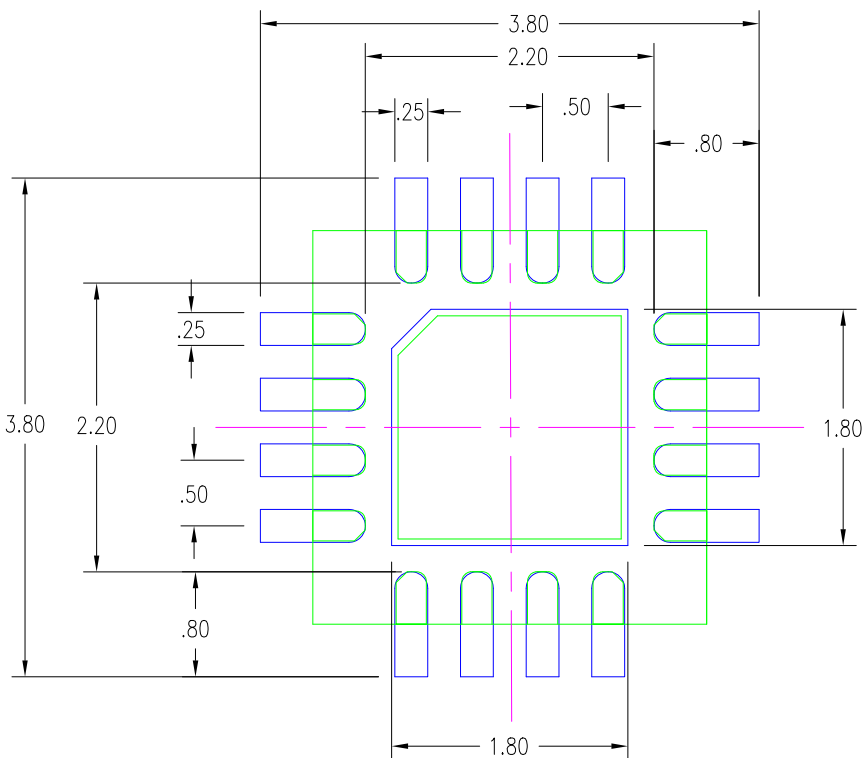
TOP VIEW

16LD QFN 3X3 (0.5MM PITCH)

| | | | |
|--------------------------------|----------|---|-----|
| TOLERANCES UNLESS SPECIFIED | |  6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com | |
| DECIMAL | ANGULAR | | |
| XX± | ± | TITLE NL/NLG16 PACKAGE OUTLINE 3.0 x 3.0 mm BODY 0.5 mm PITCH QFN | |
| XXX± | | | |
| XXXX± | | | |
| APPROVALS | DATE | SIZE | REV |
| DRAWN <i>RLC</i> | 10/15/08 | C | 01 |
| CHECKED | | DRAWING No. PSC-4169 | |
| | | DO NOT SCALE DRAWING | |
| | | SHEET 1 OF 2 | |


Package Outline and Dimensions (3 x 3mm 16-VFQFPN), cont.

| REVISIONS | | | |
|-----------|----------------------------|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/15/08 | RC |
| 01 | COMBINE POD & LAND PATTERN | 9/17/13 | KS |

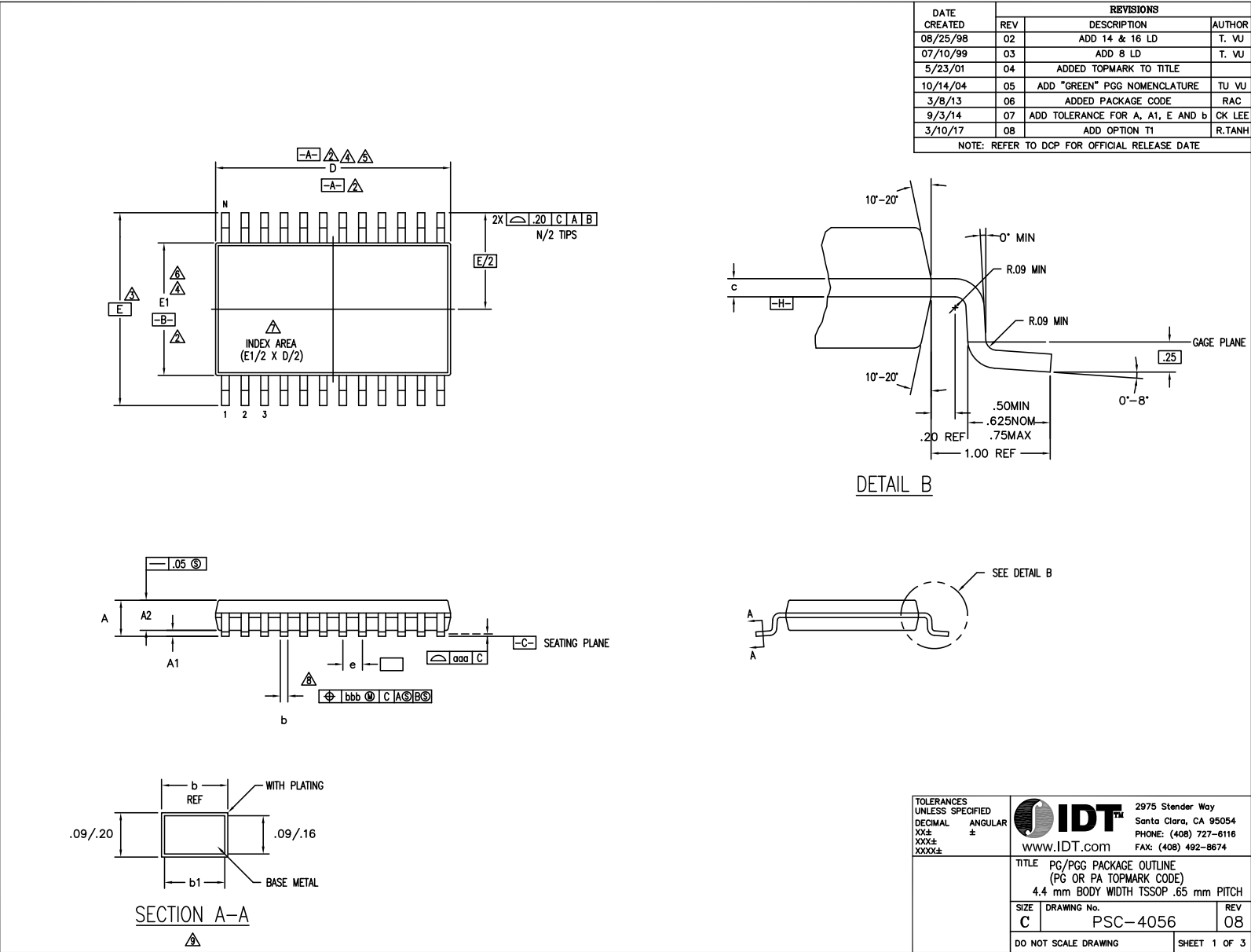


NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | | | | |
|---|----------|--|--------------|---|--|
| TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX± | |  IDT www.IDT.com | | 6024 Silver Creek Valley Road San Jose, CA 95138 ☎ PHONE: (408) 284-8200 FAX: (408) 284-8591 | |
| APPROVALS | DATE | TITLE | | | |
| DRAWN <i>RAC</i> | 10/15/08 | NL/NLG16 PACKAGE OUTLINE | | | |
| CHECKED | | 3.0 x 3.0 mm BODY | | | |
| | | 0.5 mm PITCH QFN | | | |
| | | SIZE | DRAWING No. | REV | |
| | | C | PSC-4169 | 01 | |
| DO NOT SCALE DRAWING | | | SHEET 2 OF 2 | | |

Package Outline and Dimensions (4.4 mm body, 16-TSSOP)



Package Outline and Dimensions (4.4 mm body, 16-TSSOP), cont.

| DATE CREATED | REVISIONS | | |
|-----------------|-----------|----------------------------------|--------|
| | REV | DESCRIPTION | AUTHOR |
| 08/25/98 | 02 | ADD 14 & 16 LD | T. VU |
| 07/10/99 | 03 | ADD 8 LD | T. VU |
| 5/23/01 | 04 | ADDED TOPMARK TO TITLE | |
| 10/14/04 | 05 | ADD "GREEN" PGG NOMENCLATURE | TU VU |
| 3/8/13 | 06 | ADDED PACKAGE CODE | RAC |
| 9/3/14 | 07 | ADD TOLERANCE FOR A, A1, E AND b | CK LEE |
| 3/10/17 | 08 | ADD OPTION T1 | R.TANH |

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE

| SYMBOL | PG/PGG8 | | | | NOTE | PG/PGG14 | | | | NOTE | PG/PGG16 | | | | NOTE | PG/PGG20 | | | | NOTE | PG/PGG24 | | | | NOTE | PG/PGG28 | | | | NOTE |
|--------|-----------------|------|------|-----|---------|-----------------|------|-----|---------|------|-----------------|-----|---------|------|------|-----------------|---------|------|------|------|-----------------|------|------|-----|------|-----------------|------|-----|--|------|
| | JEDEC VARIATION | | | | | JEDEC VARIATION | | | | | JEDEC VARIATION | | | | | JEDEC VARIATION | | | | | JEDEC VARIATION | | | | | JEDEC VARIATION | | | | |
| | AA | | | | | AB-1 | | | | | AB | | | | | AC | | | | | AD | | | | | AE | | | | |
| | MIN | NOM | MAX | | | MIN | NOM | MAX | | | MIN | NOM | MAX | | | MIN | NOM | MAX | | | MIN | NOM | MAX | | | MIN | NOM | MAX | | |
| A | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | | |
| A1 | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | | | |
| A2 | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | | |
| D | 2.90 | 3.00 | 3.10 | 4,5 | 4.90 | 5.00 | 5.10 | 4,5 | 4.90 | 5.00 | 5.10 | 4,5 | 6.40 | 6.50 | 6.60 | 4,5 | 7.70 | 7.80 | 7.90 | 4,5 | 9.60 | 9.70 | 9.80 | 4,5 | 9.60 | 9.70 | 9.80 | 4,5 | | |
| E | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | | |
| E1 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | | |
| e | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | | | | | | | |
| b | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | | | |
| b1 | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | | | |
| aaa | — | — | .10 | | — | — | .10 | | — | — | .10 | | — | — | .10 | | — | — | .10 | | — | — | .10 | | — | — | .10 | | | |
| bbb | — | — | .10 | | — | — | .10 | | — | — | .10 | | — | — | .10 | | — | — | .10 | | — | — | .10 | | — | — | .10 | | | |
| N | 8 | | | | 14 | | | | 16 | | | | 20 | | | | 24 | | | | 28 | | | | | | | | | |

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- DATUMS $\boxed{-A-}$ AND $\boxed{-B-}$ TO BE DETERMINED AT DATUM PLANE $\boxed{-H-}$
- DIMENSION E TO BE DETERMINED AT SEATING PLANE $\boxed{-C-}$
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE $\boxed{-H-}$
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AA, AB-1, AB, AC, AD & AE

| | | OPTION T1 | | | |
|--------|-----------------|-----------|------|--|------|
| SYMBOL | PGG14T1 | | | | NOTE |
| | JEDEC VARIATION | | | | |
| | AB-1 | | | | |
| | MIN | NOM | MAX | | |
| A | .90 | 1.10 | 1.20 | | |
| A1 | .05 | .10 | .15 | | |
| A2 | .80 | 1.00 | 1.05 | | |
| D | 4.90 | 5.00 | 5.10 | | 4,5 |
| E | 6.20 | 6.40 | 6.60 | | 3 |
| E1 | 4.30 | 4.40 | 4.50 | | 4,6 |
| e | .65 BSC | | | | |
| b | .19 | .25 | .30 | | |
| b1 | .19 | .22 | .25 | | |
| c | .09 | — | .20 | | |
| aaa | — | — | .10 | | |
| bbb | — | — | .10 | | |
| N | 14 | | | | |

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TITLE PGG/PGG PACKAGE OUTLINE
(PG OR PA TOPMARK CODE)
4.4 mm BODY WIDTH TSSOP .65 mm PITCH

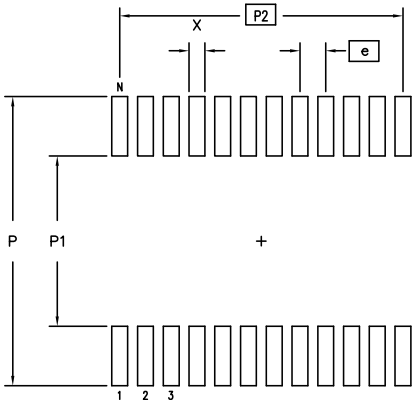
SIZE C DRAWING No. PSC-4056 REV 08

DO NOT SCALE DRAWING SHEET 2 OF 3


Package Outline and Dimensions (4.4 mm body, 16-TSSOP), cont.

| DATE CREATED | REVISIONS | | |
|--|-----------|----------------------------------|--------|
| | REV | DESCRIPTION | AUTHOR |
| 08/25/98 | 02 | ADD 14 & 16 LD | T. VU |
| 07/10/99 | 03 | ADD 8 LD | T. VU |
| 5/23/01 | 04 | ADDED TOPMARK TO TITLE | |
| 10/14/04 | 05 | ADD "GREEN" PGG NOMENCLATURE | TU VU |
| 3/8/13 | 06 | ADDED PACKAGE CODE | RAC |
| 9/3/14 | 07 | ADD TOLERANCE FOR A, A1, E AND b | CK LEE |
| 3/10/17 | 08 | ADD OPTION T1 | R.TANH |
| NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE | | | |

LAND PATTERN DIMENSIONS



| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
|----|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|
| P | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 |
| P1 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 |
| P2 | 1.95 BSC | | 3.90 BSC | | 4.55 BSC | | 5.85 BSC | | 7.15 BSC | | 8.45 BSC | |
| X | .30 | .50 | .30 | .50 | .30 | .50 | .30 | .50 | .30 | .50 | .30 | .50 |
| e | .65 BSC | | .65 BSC | | .65 BSC | | .65 BSC | | .65 BSC | | .65 BSC | |
| N | 8 | | 14 | | 16 | | 20 | | 24 | | 28 | |

| | | | | | |
|--------------------------------|-------------------------|---|---|--|--|
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| XX± | ± | | | | |
| XXX± | | | | | |
| XXXX± | | TITLE PG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH | | | |
| SIZE C | DRAWING No. PSC-4056 | | REV 08 | | |
| DO NOT SCALE DRAWING | | | SHEET 3 OF 3 | | |

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|---------------|---------------|
| 5V41285PGGI | See Page 10 | Tubes | 16-pin TSSOP | -40 to +85° C |
| 5V41285PGGI8 | | Tape and Reel | 16-pin TSSOP | -40 to +85° C |
| 5V41285NLGI | See Page 10 | Trays | 16-pin VFQFPN | -40 to +85° C |
| 5V41285NLGI8 | | Tape and Reel | 16-pin VFQFPN | -40 to +85° C |

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

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Revision History

| Rev. | Date | Originator | Description of Change |
|------|----------|------------|--|
| A | 04/03/12 | J. Chao | New datasheet; Preliminary initial release. |
| B | 06/05/12 | J. Chao | 1. Removed references to outputs for Ethernet applications in General Description and Features. 2. Updated pins 1 and 2 in pinout and pin description table from S0:S1 to NC. 3. Removed Output Select table. 4. Removed commercial grade ordering info. |
| C | 06/29/12 | J. Chao | 1. Under output features, changed to “2 - 100MHz 0.7V current mode...” 2. Added to the beginning of the CLK1 (pin 10/11) and CLK0 (pin 14/15) descriptions “ 100MHz HCSL...” |
| D | 07/23/12 | J. Chao | 1. Updated Output Features bullet to include “Non-spread” nomenclature. 2. Added “Low Phase Noise:... ” bullet to Features/Benefits. 3. Added “Output Select Table 1”. 4. Updated pin 1 & 2 descriptions to remove NC and replace with S0 and S1 respectively. 5. Updated pin descriptions for pins 1 & 2. |
| E | 07/24/12 | J. Chao | 1. Removed 100MHz selection on the pins 10/11 and 14/15 descriptions, and from the Output Features section. 2. Changed Cycle-to-cycle Jitter max. spec from 100ps to 80ps. |
| F | 10/24/12 | J. Chao | Added note to page 1 Features/Benefits section stating “For PCIe Gen3 applications, see the 5V41315” |
| G | 06/10/14 | J. Chao | 1. Added 16VFQFPN package, tables and all references. 2. Moved to Final. |
| H | 05/08/17 | C.P. | Updated package outline drawings and legal disclaimer. |

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