RAA223182

1000V Off-line Flyback Regulator

The RAA223182 is an off-line Flyback regulator with a 1000V integrated MOSFET, designed for high input voltage applications such as 3-phase electric meter power supplies and other generally isolated power supplies. The RAA223182 can deliver up to 11W from the universal 3-phase input voltage.

The RAA223182 operates in DCM with constant switching frequency at full load. The system is inherently stable with an easy feedback loop design while switching at constant frequency without interfering with the communication of the smart meter. At light load, the RAA223182 enters burst mode operation to reduce the IC power consumption while keeping the burst frequency below 3kHz to avoid interference to the PLC frequency band.

The RAA223182 features a unique short-time heavy load operation mode, which boosts output power for a programmed time. This feature allows the smart meter's AC/DC power supply to be designed at a regular power level without being over-designed for 2x power in the transmission mode, greatly reducing system cost.

The RAA223182 also has a fault-tolerant input overvoltage protection feature. The CDRV pin allows customers to use an external FET to disconnect the input bulk capacitors from the DC bus to protect them from a sustained overvoltage while simultaneously stopping the main switching (Figure 30). When this is not needed, the CDRV pin can simply be floated (Figure 1). The IC simply stops the PWM switching in the event of an input overvoltage. See Table 1 for other RAA22318x products with different overvoltage protection features.

In addition, the RAA223182 adopts the valley switching technique to reduce switching losses and EMI noises. It also features VinUV, input brownout, VccUV, VccOV, output overload, output short-circuit, primary winding short, and over-temperature protections. These features are integrated into an SO13 package.

Features

- Flyback regulator with 1000V 9Ω MOSFET
- Frequency doubling for heavy load operation (21W and above), for a programmable duration (maximum time depends on thermal capability)
- Fault-tolerant input overvoltage protection
- Valley switching to reduce switching losses
- Programmable constant frequency PWM operation
- Burst mode operation at light load
- Protection features: short-circuit protection (SCP), overload protection (OLP), input undervoltage lockout (VinUV), input OVP, VCC overvoltage protection (VccOV), VCC undervoltage lockout (VccUV) and over-temperature protection (OTP).

Applications

- Smart Meter
- Large appliances
- Industry control

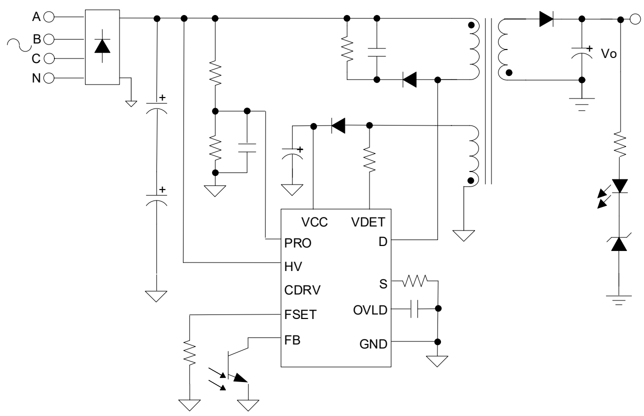


Figure 1. Typical 3-Phase RAA223182 Flyback Circuit

Contents

1. Overview

1.1 Block Diagram

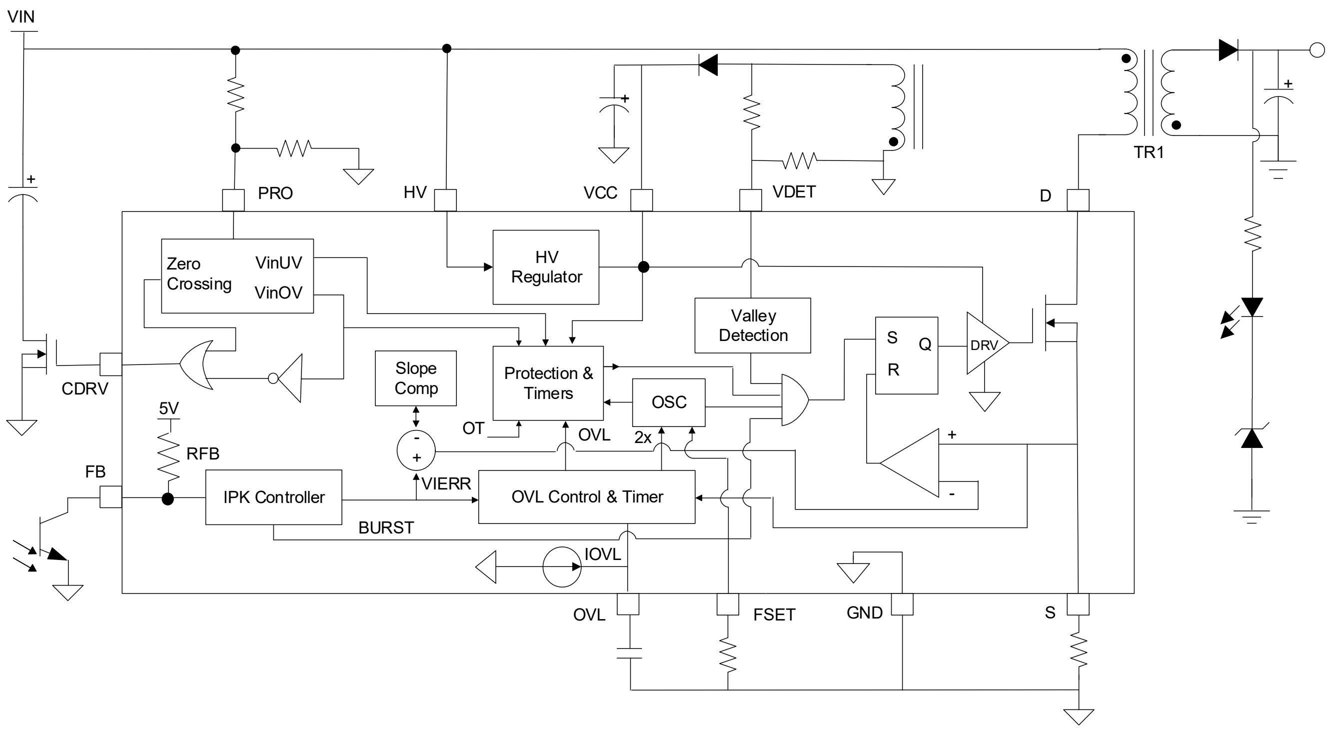


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments

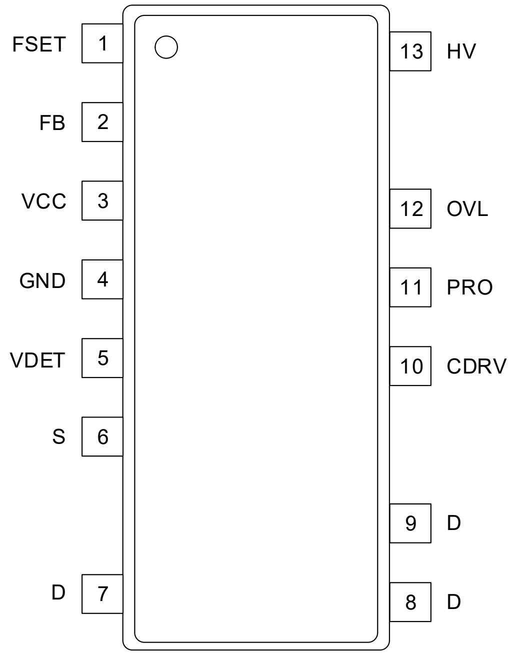


Figure 3. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	FSET	Oscillator frequency set
2	FB	Feedback
3	VCC	IC supply voltage
4	GND	Signal ground
5	VDET	Valley detection
6	S	Source of power FET
7, 8, 9	D	Drain of power FET
10	CDRV	Gate of input cap disconnection MOSFET
11	PRO	Bus overvoltage sense
12	OVL	Short-time heavy-load programming
13	HV	High voltage startup

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC	-0.3	+30	V
VFB	-0.3	+5	V
VDET	-0.3	+5	V
CDRV	-0.3	+30	V
PRO	-0.3	+5	V
HV	-0.3	+700	V
D (to S)	-0.3	+1000	V
Continuous Power Dissipation (T_A = +25°C)	-	1	W
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-60	+150	°C
Human Body Model (Tested per JS-001-2017)	-	1.2	kV
Charged Device Model (Tested per JS-002-2018)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	13 Ld SOIC	θ_{JA}[1]	Junction to ambient	27.4	°C/W
		θ_{JC}[2]	Junction to case	31	°C/W

1. θ_{JA} is measured on a FR4 2oz PCB with copper size of 165mm^2 on pin 7, 8, and 9 at 26°C ambient.
2. For θ_{JC}, the case temperature location is taken at the package top center.

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
V_{CC}	10	24	V
Ambient Temperature	-40	+125	°C

3.4 Electrical Specifications

Typical operating conditions at 25°C, V_{DRAIN} = 375V, V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Startup and Power FET						
Internal V_{CC} Startup Current	I_{VCC_START}	V_{CC} = 8, V_{DRAIN} = 100V	-	4.0	8	mA
Drain Leakage Current	I_{D_LEAK}	V_{CC} = 0, V_D = 375V, V_{FB} = 0V	-	0.1	3.5	µA
HV Bias	I_{HV_BIAS}	V_{CC} = 12, V_{DRAIN} = 375V	-	1.0	5	µA
Power FET Breakdown Voltage	$V_{(BR)DSS}$	-	1000	-	-	V
Power FET On-Resistance	$r_{DS(ON)}$	T_J = 25°C, V_{CC} = 12V, I_{DS} = 300mA	-	9	11	Ω
		T_J = 125°C	-	18	22	Ω
Power FET Output Capacitance	C_{oss}	V_{DS} = 25V, V_{GS} = 0V	-	24.7	-	pF
V_{CC} Supply						
V_{CC} Start (Rising)/HV Regulator Off	V_{CC_START}	V_{HV} = 100V	11	12	13	V
V_{CC} (Falling) /HV Regulator On	V_{CC_HVON}	V_{HV} = 100V	8	9	10	V
HV Regulator On/Off Hysteresis	V_{VCC_HYS}		2	3	4	V
V_{CC} Undervoltage Threshold (Falling)	V_{CC_UVLO}	IC stop switching	4.8	5.5	6	V
V_{CC} OVP Threshold	V_{CC_OVC}	-	21.4	24	26.3	V
V_{CC} OV Latch-Off Threshold	V_{CC_OVL}	-	23	26	29.5	V
V_{CC} Quiescent Current	I_{VCC_Q}	V_{FB} =0V, no switching	-	480	685	µA
V_{CC} Current During Switching	I_{VCC}	V_{FB} > 0.7V, switching frequency = 50kHz, D = 0.4	-	705	825	µA
Current Sense						
Max Current Sensing Threshold	V_{CS_MAX}	V_{FB}=2.5V,	425	500	550	mV
SCP Threshold	V_{CS_SC}	-	-	1000	-	mV
Minimum Current Sensing Threshold	V_{CS_MIN}	-	155	205	245	mV
Leading Edge Blank Time	t_{LEB}	-	300	350	425	ns
Feedback						
Transconductance	GM	V_{FB} to V_{CS}	-	0.225	-	V/V
FB Pin Pull-Up Resistor	R_{FB}	-	24	35	-	kΩ
FB Threshold Entering Burst Mode	V_{BURL}	-	-	1.5	-	V
FB Threshold Exiting Burst Mode	V_{BURH}	-	-	1.87	-	V
FB Threshold Into 2x Frequency	V_{FB_2XF}	-	2.6	3.2	4	V
FB Threshold Out of 2x Frequency	V_{FB_1XF}	-	1.6	2.6	3.2	V
FB Threshold for Overload Protection	V_{FB_OLP}	-	3.8	4.4	5.1	V
FB Internal Pull-Up Voltage	V_{FB_MAX}	-	4.4	4.8	-	V

Typical operating conditions at 25°C, V_{DRAIN} = 375V, V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise specified. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Programmable Heavy Load						
OVL Pin Source Current	I_{OVL}	-	-	10.5	11.8	µA
OVL Pin Discharge Current	I_{OVL_D}	-	1.8	2	-	µA
OVL Pin Threshold	V_{OVL}	-	3.7	4.2	4.7	V
Input Undervoltage and Overvoltage Protection						
PRO Pin UV Rising Threshold	V_{BUSUV_R}	-	0.35	0.4	0.5	V
PRO Pin UV Falling Threshold	V_{BUSUV_F}	-	0.23	0.3	0.37	V
PRO Pin OV Threshold (Rising)	V_{BUSOV_R}	-	4.3	4.7	5.2	V
PRO Pin OV Threshold (Falling)	V_{BUSOV_F}	-	3.8	4.25	4.7	V
OV Falling Delay	T_{BUSOV_DL}	-	1.3	1.6	-	ms
CDRV Driver Low-Side On-Resistance	R_{DS_L}	-	-	17	32	Ω
CDRV Driver Source Current	I_{DRVS}	-	-	25	-	mA
Frequency						
FSET Pin Reference Voltage	V_{FSET}	-	2.3	2.5	2.7	V
Oscillator frequency	f_{SW}	R_{FSET} = 187k	42.5	50	55	kHz
Dithering		percent frequency	-2.5	-	2.5	%
Double Frequency	f_{SW_2x}		85	90	95	kHz
Valley Detection						
Ringing Frequency	-	Established by design	550	-	1000	kHz
Timing						
Maximum Duty Cycle	D_{MAX}	f_{SW} = 50kHz	42	50	54	%
OVL Blanking	T_{OVL_BLK}	2 Cycles, 50kHz	-	40	-	µs
Startup Timer	T_{ST}	4096 cycles, 50kHz	-	82	-	ms
Hiccup Restart Delay	T_{HICC}	16384 cycles, 50kHz	-	328	-	ms
OLP/OCP Delay Timer	T_{OLP}	2048 cycles, f_{SW} = 100kHz, V_{FB} > 4.5V	-	20.5	-	ms
VinUV Delay Timer	T_{VINUV}	2048 cycles, f_{SW} = 100kHz	-	20.5	-	ms
Thermal						
Over-Temperature Threshold	OTP_{TH}	-	-	150	-	C
Over-Temperature Hysteresis	OTP_{HYS}	-	-	30	-	C

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

4. Typical Characterization Curves

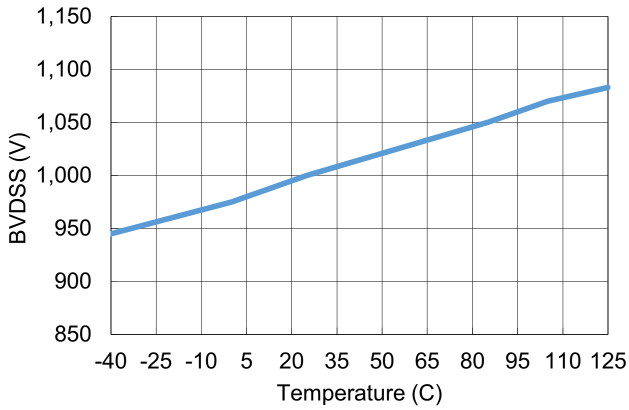


Figure 4. Breakdown Voltage vs Temperature

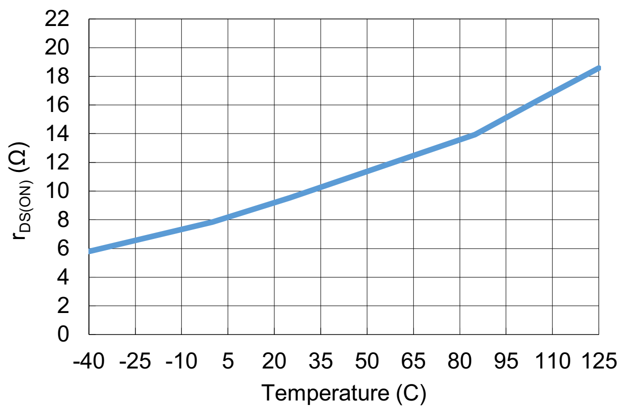


Figure 5. $r_{DS(ON)}$ vs Temperature

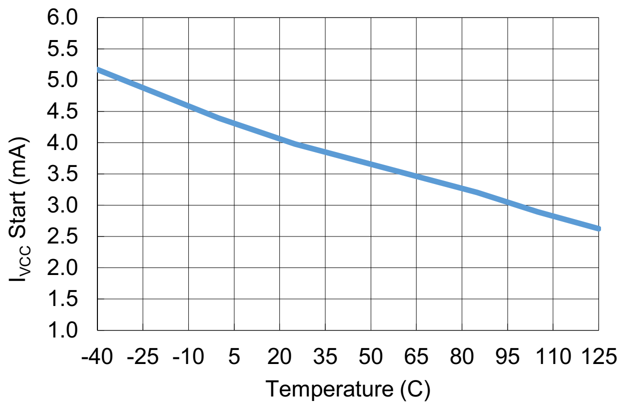


Figure 6. VCC Start Current vs Temperature

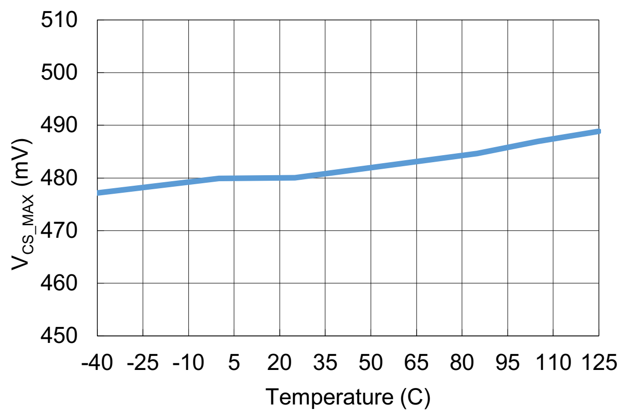


Figure 7. Maximum Current Sensing Threshold vs Temperature

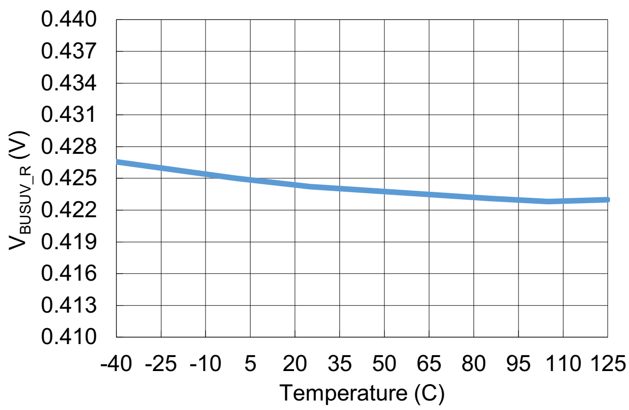


Figure 8. BUS Undervoltage Rising vs Temperature

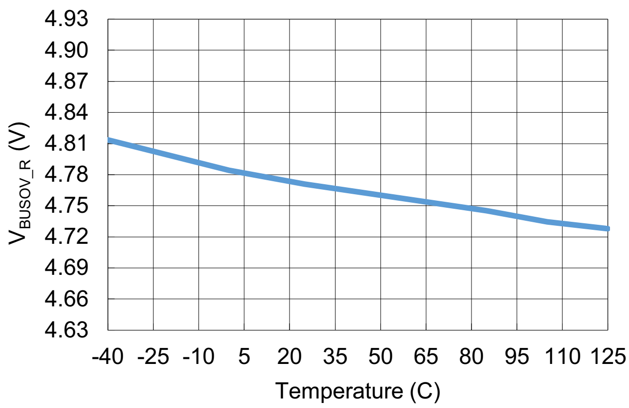


Figure 9. BUS Overvoltage Rising vs Temperature

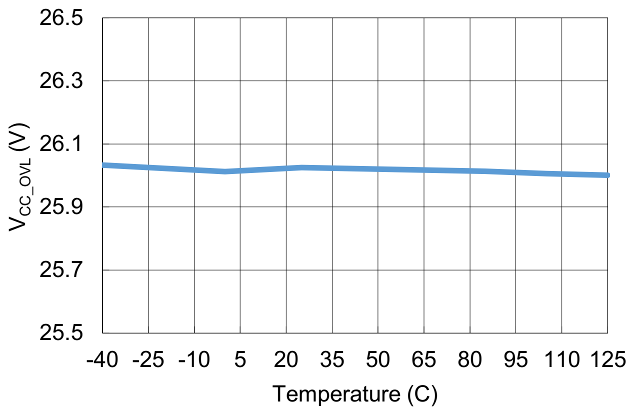


Figure 10. VCC OVP Latch Threshold vs Temperature

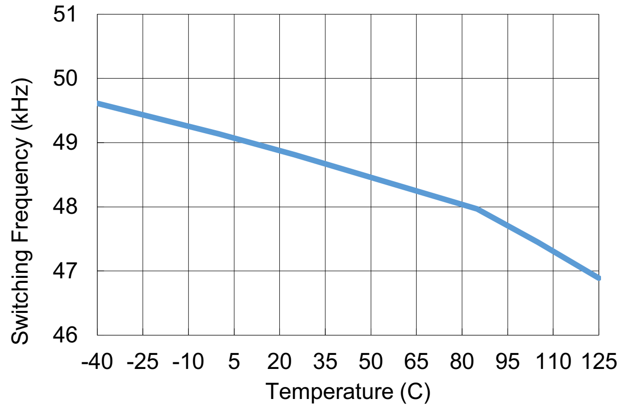


Figure 11. Switching Frequency (R_{FSET} = 200k) vs Temperature

Typical Waveforms (V_{IN} = 230V_{AC}, V_{OUT} = 13V, I_{OUT} = 850mA, Lpri = 1.3mH, C_{OUT} = 1000µF, T_A = 25°C)

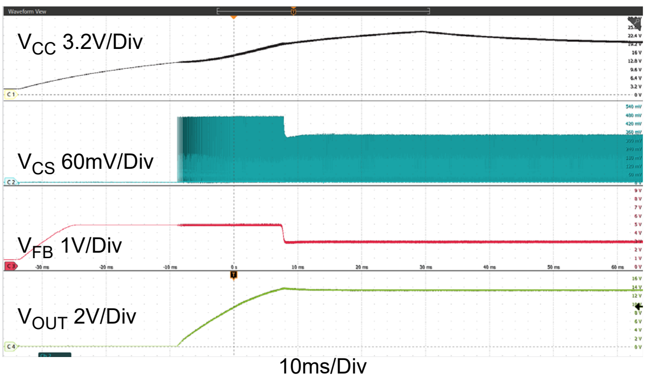


Figure 12. Startup

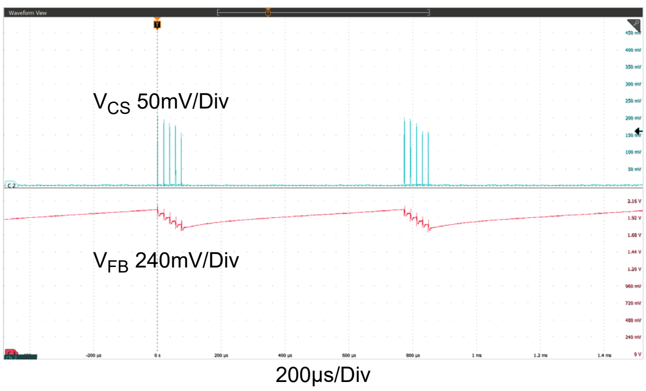


Figure 13. Light Load Operation

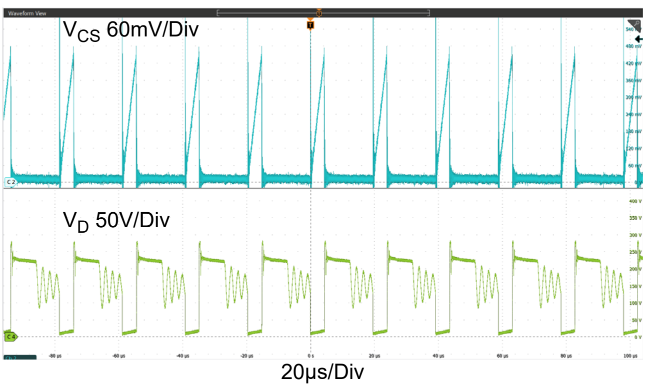


Figure 14. Full Load Operation (V_{IN} = 120V_{AC})

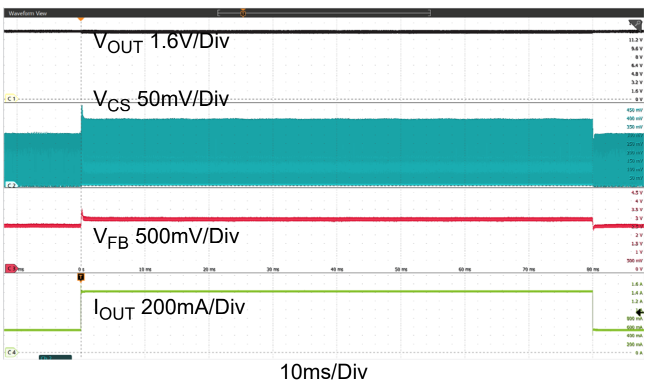


Figure 15. Short-Time Heavy Load Operation

Typical Waveforms (V_{IN} = 230V_{AC}, V_{OUT} = 13V, I_{OUT} = 850mA, Lpri = 1.3mH, C_{OUT} = 1000µF, T_A = 25°C) (Cont.)

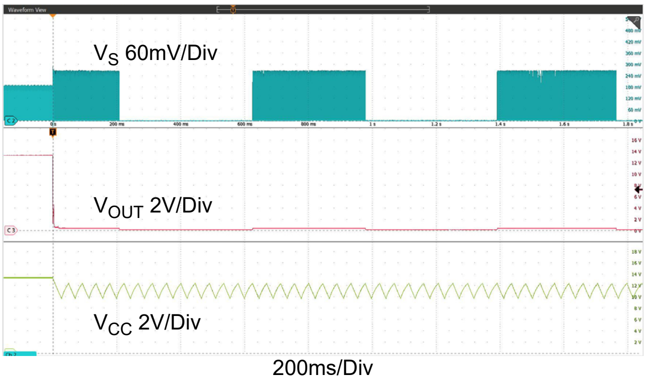


Figure 16. Short-Circuit/Overload Protection

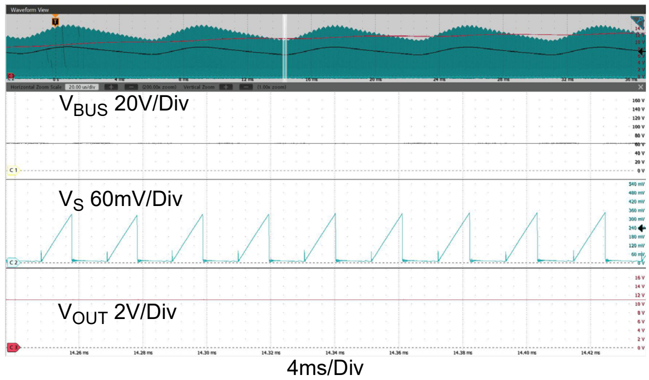


Figure 17. Input Brownout Protection (V_{IN} = 80V_{AC})

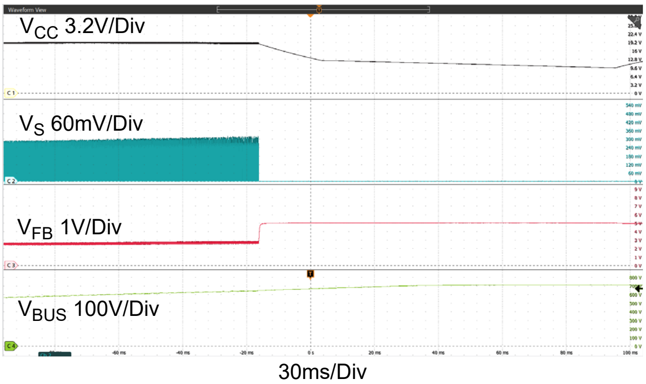


Figure 18. Bus Overvoltage Protection

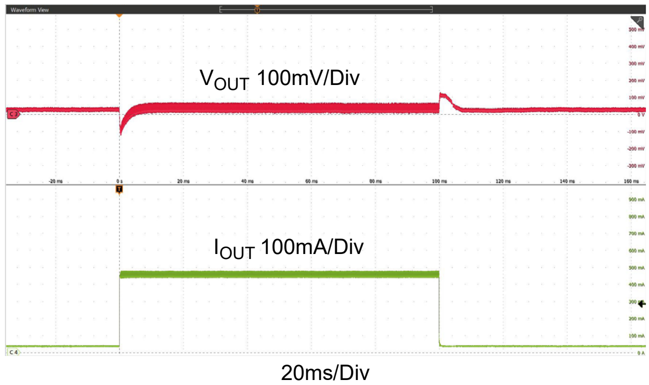


Figure 19. Load Transient (45mA-450mA)

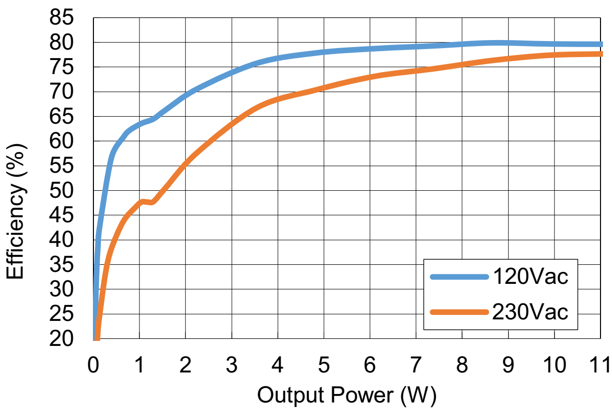


Figure 20. Efficiency (3-Phase)

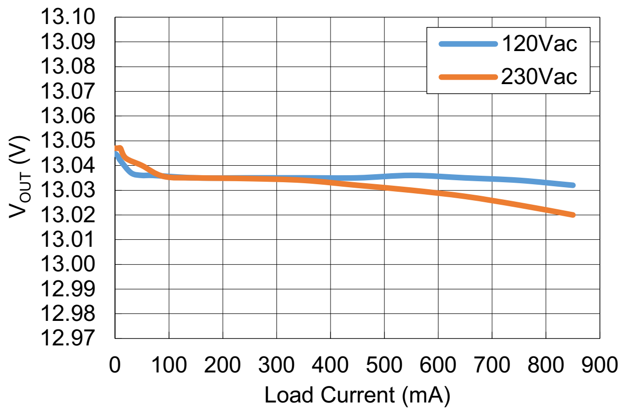


Figure 21. Load Regulation (3-Phase)

5. Detailed Description

The RAA223182 adopts constant frequency switching with secondary side regulation, as Figure 22 shows. When the power is less than the maximum output power (set by RS, primary transformer inductance, and the FSET resistor), it operates in DCM at the chosen switching frequency. When the power exceeds the maximum output power, it operates in CCM at the doubled frequency for a programmed time. The output voltage keeps regulated during the double-frequency operation until overload protection is reached. The IC uses valley detection to reduce switching losses and ensure DCM operation.

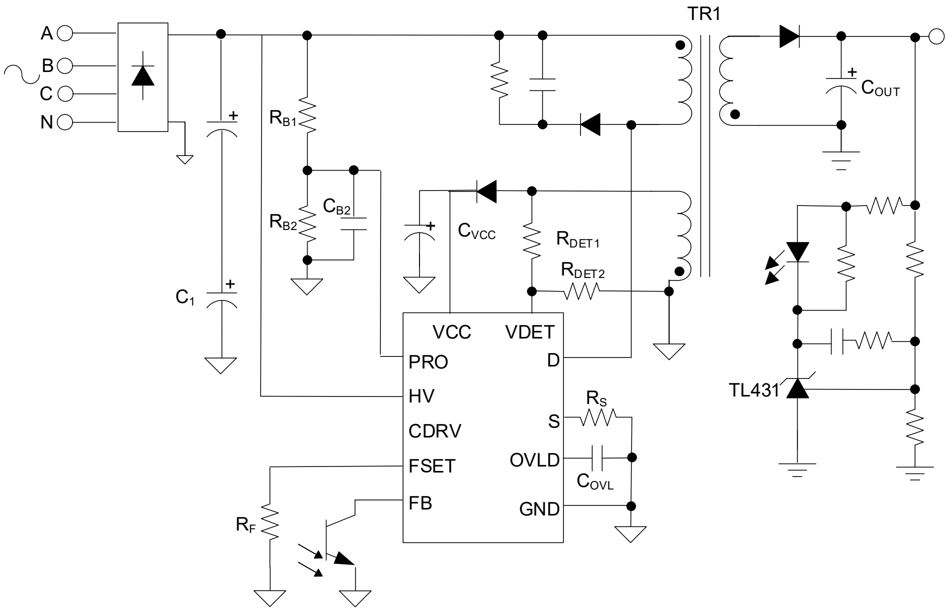


Figure 22. RAA223182 Flyback Application Circuit

5.1 Constant frequency PWM mode

The IC regulates the output voltage with an error amplifier (TL431) through the optocoupler and peak current control at full load. The feedback pin is the error output optocoupled from the secondary side. Its voltage level controls the peak current in every switching cycle. The turn-on point is set by the internal fixed frequency oscillator and valley detection circuit, which senses the voltage on the auxiliary winding. If the valley is undetected, it waits for the nearest valley to turn on the FET. The valley detection is illustrated in Figure 23. Because the ringing frequency usually ranges from 500kHz to 1MHz, the possible half-ringing cycle delay only causes ~5% frequency variation.

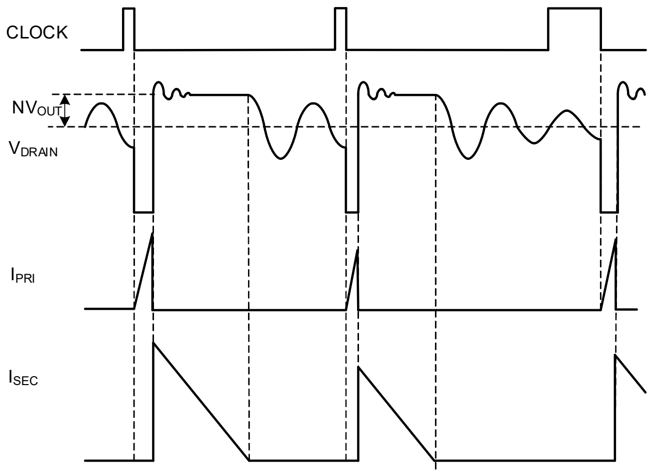


Figure 23. Valley Switching

5.2 Burst Mode

At the light load, the regulator transitions into burst mode operation to save power consumption while keeping the switching frequency constant without interfering with the communication. The burst frequency is designed to be less than 3kHz, to avoid the minimum frequency of the narrow-band PLC communication. During light load, the FB voltage is reduced, and when it drops below V_{BURL}, the part enters burst mode operation. The IC stops switching. When FB voltage rises to V_{BURH}, the IC resumes switching until FB voltage falls back to V_{BURL}. In Burst mode, the peak current is less than 200mA, effectively avoiding audible noises. Burst Mode is illustrated in Figure 24.

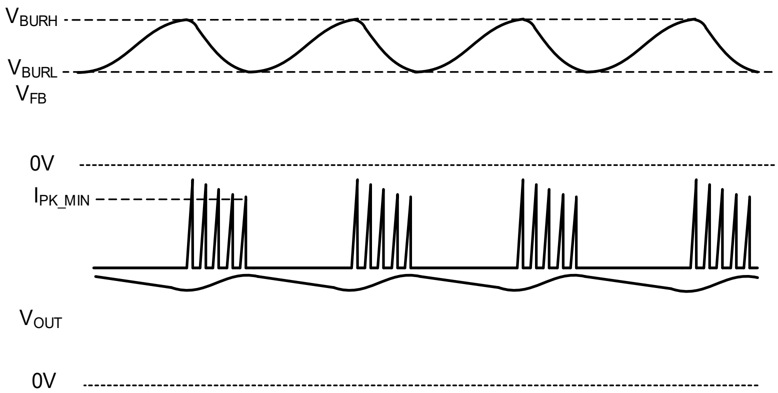


Figure 24. Burst Mode Operation at Light Load

5.3 Short-Time Heavy Load Operation (OVL)

The IC allows a short-time heavy load operation over a programmable time (depending on the thermal capability of the design). When V_{FB}> V_{FB_100k}, the oscillator frequency is doubled, valley detection is disabled, and the part operates in CCM. At the same time, a programmable timer starts - an internal 10µA current charges the external cap on pin OVL. When the OVL pin reaches 4.2V, the heavy load operation stops, and the IC waits for five times the programmed heavy load operation time before the heavy load operation is allowed again. When V_{FB}<V_{FB_50k}, the part exits heavy load operation before the heavy load timer expires. If the load is too heavy, FB continues rising to V_{FB_OLP}, the heavy load operation stops, and the overload protection is triggered. The operation is shown in Figure 25.

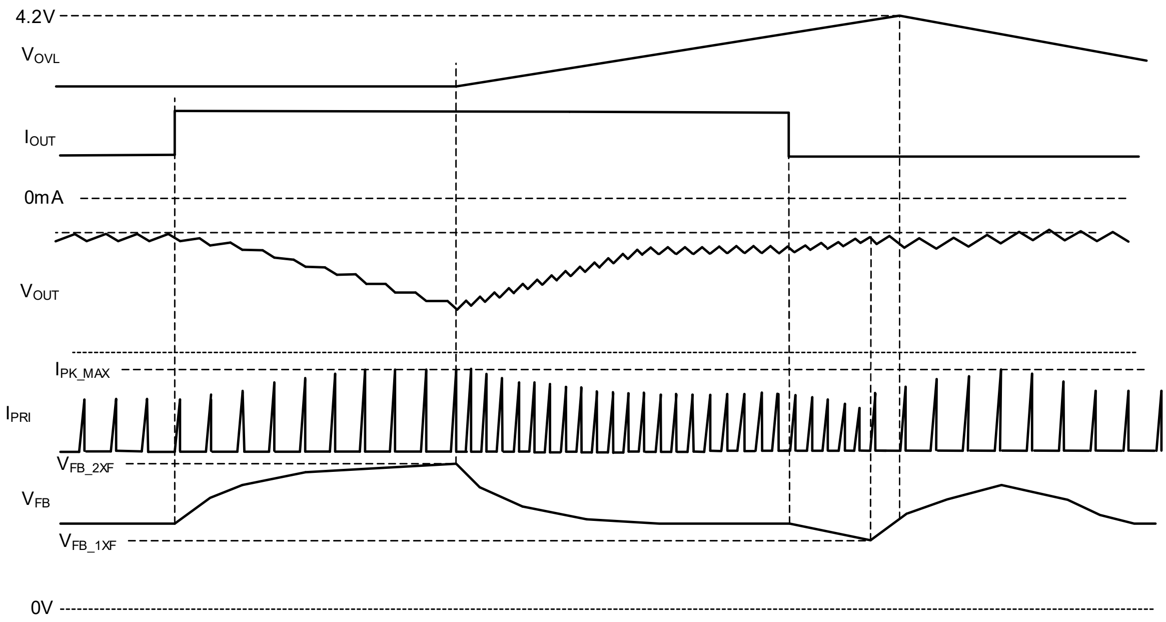


Figure 25. Short-Time Heavy Load Operation

5.4 Input Overvoltage Protection

When CDRV is not used (floated), the IC detects the input overvoltage by the PRO pin through a resistor divider connected to the rectified DC BUS. When the PRO pin voltage is higher than a certain level, IC stops the PWM switching, protecting the internal power FET from the potential overvoltage damage, as illustrated in Figure 26.

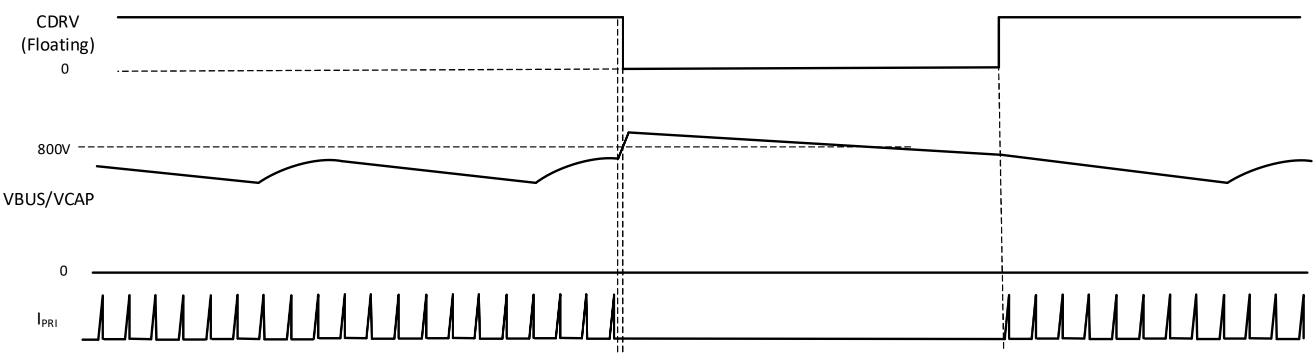


Figure 26. Input Overvoltage Protection

5.5 The Optional Cap Saver

The IC also has an optional cap-saver feature that protects the input bulk cap from potential overvoltage damage. The protection uses the CDRV pin to control an external FET connected to the input bulk cap (Figure 30). If an input overvoltage event occurs, the FET is turned off and disconnects the bulk cap from the rectified DC BUS, therefore protecting the cap from overvoltage damage. At the startup, the FET is initially off. When the rectified voltage is pulled down low enough by the switching current, it's turned on with minimum inrush current. The operation is illustrated in Figure 27.

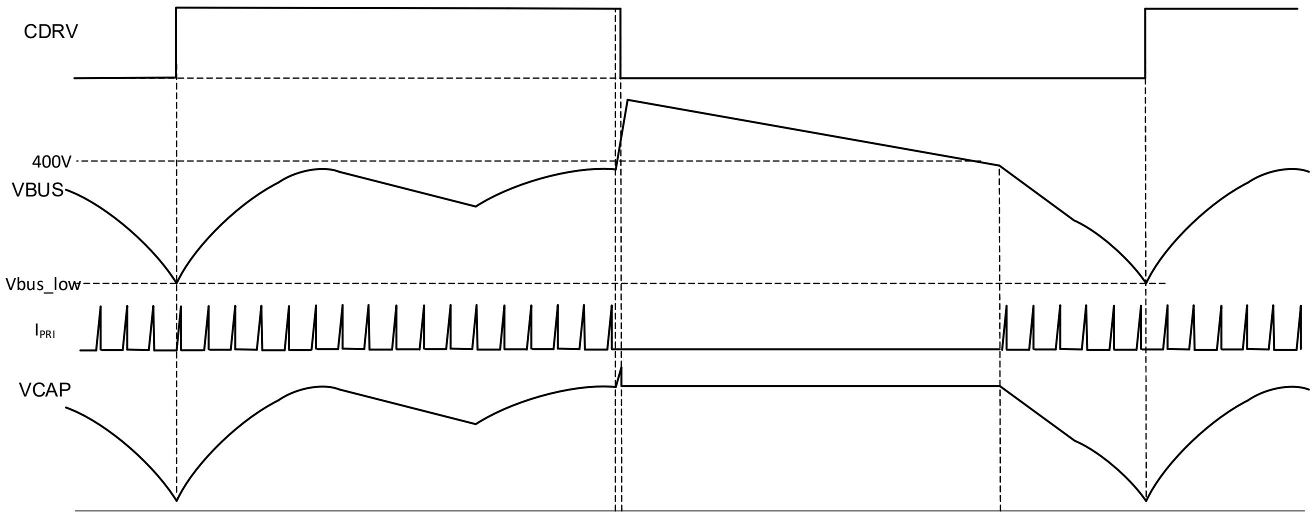


Figure 27. Input Overvoltage Protection with the Cap-Saver FET

5.6 Soft Startup

When the input rectified voltage is higher than a certain level (determined by the PRO pin resistor divider), an internal HV current source (I_{VCC_START}) starts to charge the VCC cap. When the VCC reaches V_{CC_START}, the IC switches, a startup timer begins (~82ms), and the internal HV regulator turns off; the regulator turns on again when VCC drops below V_{CC_HVON}. Before the timer expires, a DCM operation with a constant maximum peak current is enforced to ensure a soft startup. The SCP is disabled during the startup blanking time. When V_{OUT} is fully established, VCC is supplied by the auxiliary winding, and the internal HV current source is mostly off in steady-state operation to save power consumption. The startup process is illustrated in Figure 28 shows.

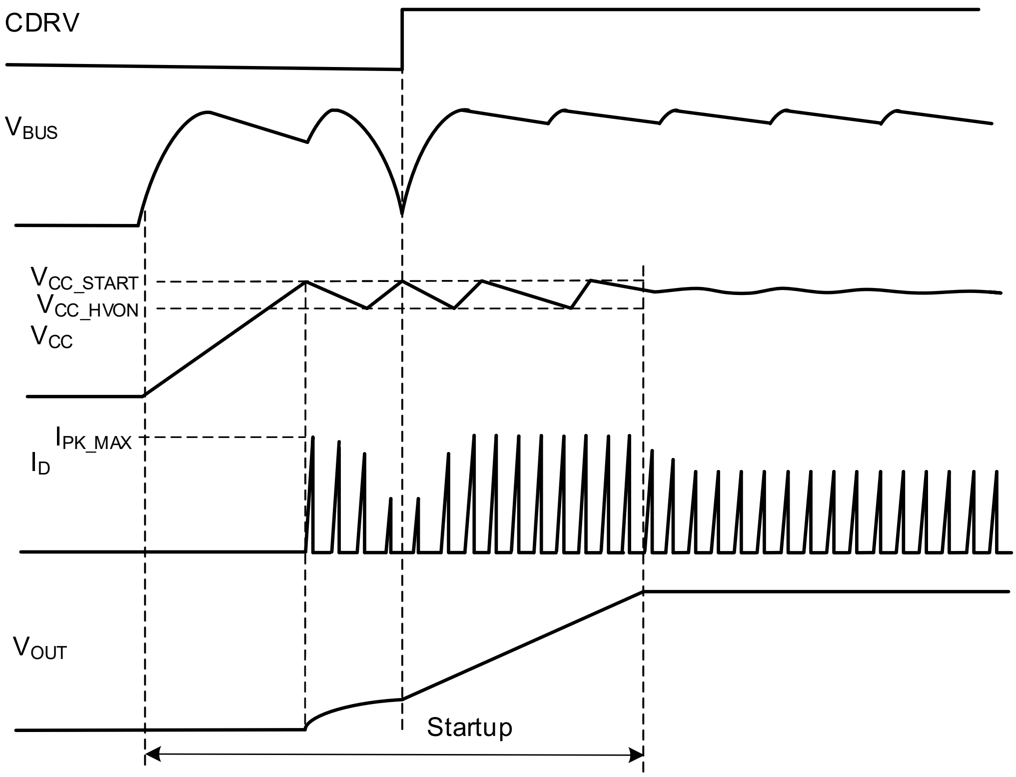


Figure 28. Startup Process

5.7 VCC Overvoltage and Undervoltage Protection

VCC voltage provides internal voltage for IC operation and is used to drive the internal power FET. It should stay within a certain range to ensure effective MOSFET driving. In steady-state operation, VCC is normally supplied by an auxiliary winding of a flyback transformer unless supplied by an external power supply. If VCC receives an excessive supply current, the VCC voltage increases. When the VCC voltage reaches V_{CC_OVC}, an internal shunt regulator is on to sink a current to prevent it from going higher (clamping). If VCC still increases and reaches a higher level at V_{CC_OVL}, the IC is latched off to prevent damage to the gate of the internal MOSFET unless VCC or VIN is recycled. When VCC is less than V_{CC_UVLO}, the IC stops switching until it is charged back to V_{CC_START}.

5.8 Overload and Short-Circuit Protection

When an overload or a short-circuit occurs, V_{FB} rises high. When V_{FB} reaches V_{FB_2XF}, the heavy load operation is enabled with twice the switching frequency. If V_{FB} continues to rise and reaches another threshold V_{FB_OLP}, and the current sense detected above V_{CS_MAX} after a blanking time, a fault delay timer starts. If these thresholds are still reached after the timer expires (~20.5ms), the heavy load operation is disabled, and the IC stops switching for a hiccup time (~328ms). The IC resumes switching after the timer expires. Figure 29 shows the logic sequence.

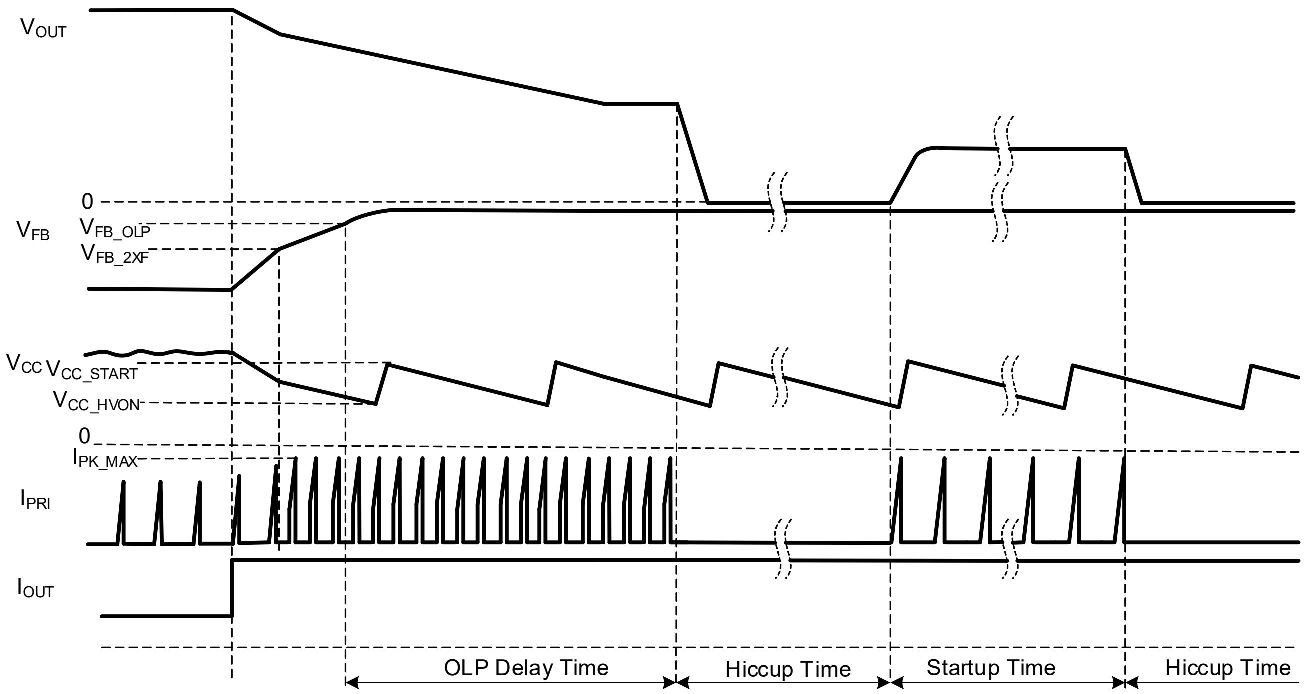


Figure 29. Overload Protection Diagram

6. Application Topologies

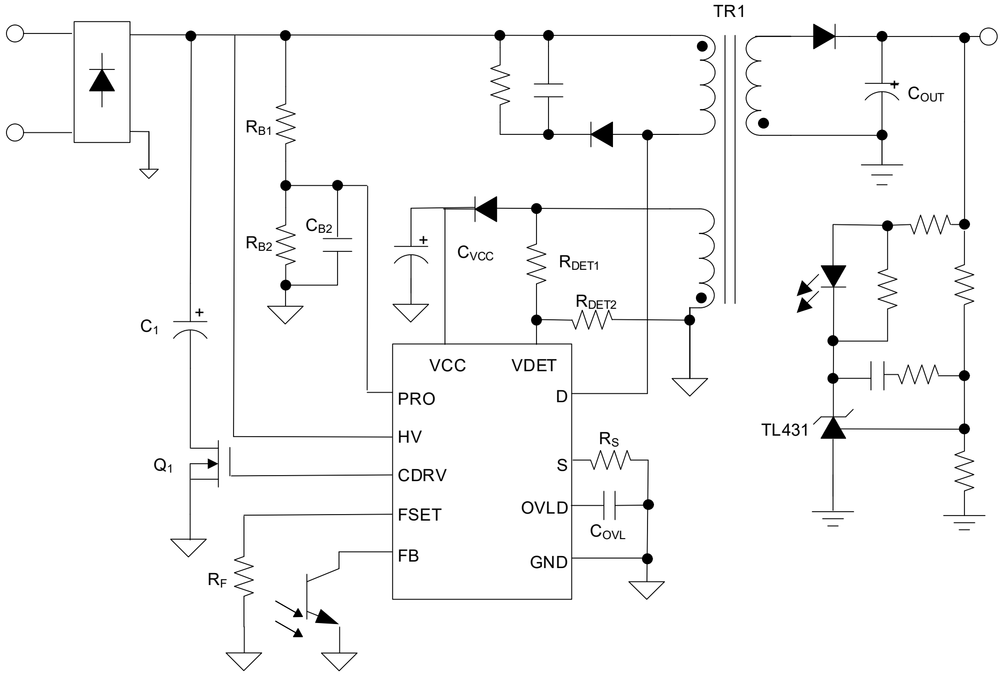


Figure 30. Single-Phase RAA223182 Flyback with Cap-Saver Overvoltage Protection

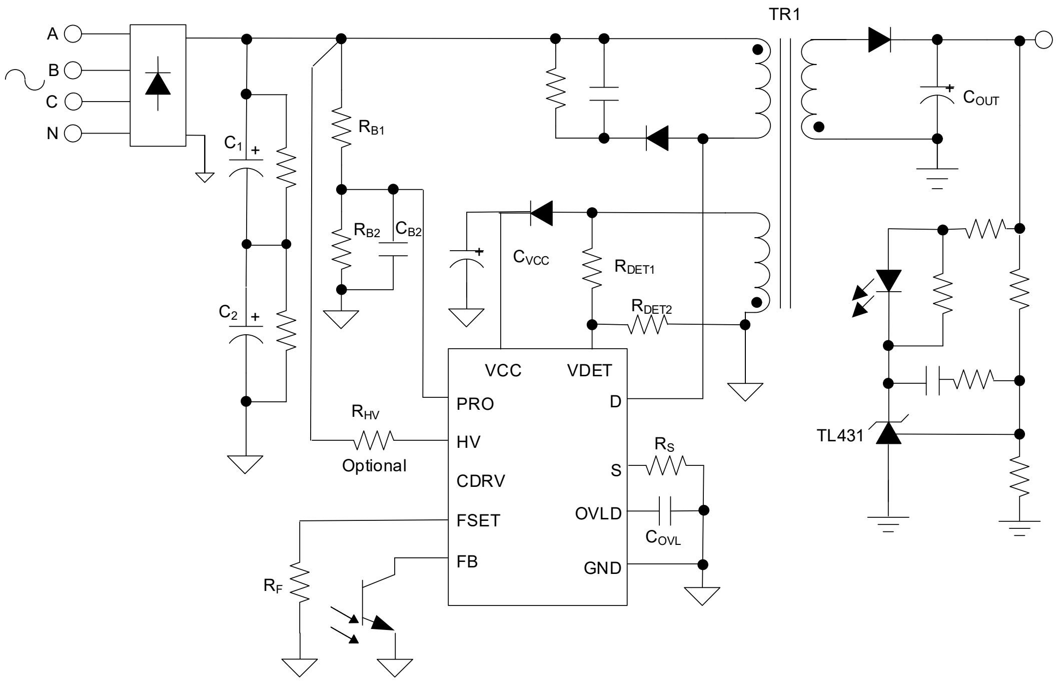


Figure 31. Three-Phase RAA223182 Flyback

7. Design Guidance

7.1 Input Bulk Capacitor

The input bulk capacitor provides a DC voltage with some voltage ripple for a given power. In other words, how low the bus voltage can drop to determines the power Flyback can deliver. Equation 1 calculates the required minimum bus valley voltage for the target output power. To keep the bus valley above this value, the bulk capacitance needs to be big enough to not only support normal output power but also a short-time heavy load up to 2x normal output power. Use Equation 2 to calculate the required capacitance, where I_{PKFL} is the peak current required for your full load operation. D_{MAX} is the maximum duty cycle in DCM operation. η is the assumed full load efficiency at $85V_{AC}$.

(EQ. 1) $$V_{valley} = \frac{2P_{OUT}}{\eta I_{PKFL} D_{MAX}}$$

(EQ. 2) $$C_{in} = \frac{4P_{OUT}\left(0.25 + \frac{1}{2\pi}\operatorname{asin}\frac{\sqrt{2}V_{acmin} - V_{valley}}{\sqrt{2}V_{acmin}}\right)}{\eta(2V^2_{acmin} - V^2_{valley})f_{LINE}}$$

In 3-phase applications, when the regular output power is not more than 15W, the required V_{valley} is always guaranteed by the rectified voltage, even when AC input is at a minimum. Therefore, theologically, a bulk capacitor is not necessary to maintain the power delivery, even though a capacitor is often added to absorb surge energy.

7.2 Transformer Primary Inductance and Turns Ratio

Because the regulator operates in DCM, the primary inductance has to be chosen small enough so that the inductor current always resets within a switching cycle while still big enough to deliver enough power at minimum AC input. Accordingly, use Equation 3 to calculate the required primary inductance, while using Equation 4 to specify its maximum value. In 3-phase applications with regular output power less than 15W, $V_{valley} = 1.5 \times \sqrt{2} \times V_{acmin}$.

(EQ. 3) $$L_P \geq \frac{2P_O}{\eta f_{SW} I^2_{PKFL}}$$

(EQ. 4) $$L_P \leq \frac{D_{MAX} V_{valley}}{f_{SW} I_{PKFL}}$$

The transformer turns ratio needs to be set appropriately so the duty cycle is not too big at the valley of the rectified bus voltage at the minimum AC input, even when it runs into 2x frequency operation. The maximum turns ratio can be calculated using Equation 5. D_{max} is the maximum duty cycle in 2x frequency operation. It can be chosen around 0.7. In 3-phase applications, $V_{valley} = 1.5 \times \sqrt{2} \times V_{acmin}$.

(EQ. 5) $$N \leq \frac{V_{Valley}}{V_o} \bullet \frac{D_{max}}{1 - D_{max}}$$

In the meantime, the turns ratio needs to be big enough so that the maximum peak current can fully reset when D_{MAX} is reached at the valley of the minimum AC input. The minimum turns ratio needs to satisfy Equation 6.

(EQ. 6) $$N \geq \frac{L_P I_{PKFL} f_{SW}}{(1 - D_{MAX})V_O}$$

7.3 Current-Sensing Resistor

The peak current is sensed through R_{SENSE} on the S pin and compared with the internal current command. When the sensed voltage reaches the command, the MOSFET is turned off. With the chosen R_{SENSE}, the max peak current is limited by an internal current sense voltage limit, V_{CS_MAX}. To have a good regulation without hitting the peak current limit, V_{SENSE} should be set around $0.9V_{CS\_MAX}$. Use Equation 7 to calculate R_{SENSE}.

Note: RSENSE needs to be evaluated for proper power capability.

(EQ. 7) $$R_{SENSE} = \frac{0.9V_{CSMAX}}{I_{PKFL}}$$

7.4 FSET Pin Resistor

The FSET pin resistor sets the switching frequency. Use Equation 8 to calculate the resistor value.

(EQ. 8) $$R_{FSET} = \frac{3.72V_{FSET}}{f_{SW}} \times 10^6 (k\Omega)$$

7.5 VDET Pin Resistors

The valley switching is detected at the VDET pin by a resistor divider (R_{DET1} and R_{DET2}). Use Equation 9 to calculate the R_{DET1} value and Equation 10 to calculate the R_{DET2} value. N_{PA} is the turn ratio of the primary winding to auxiliary winding, and V_{ACMAX} is the maximum AC input voltage. N_{SA} is the turn ratio of the output winding to the auxiliary winding. V_{DF} is the forward voltage of the output diode.

(EQ. 9) $$R_{DET1} \geq \frac{\sqrt{2}V_{ACMAX}}{N_{PA}} (k\Omega)$$

(EQ. 10) $$R_{DET2} < \frac{R_{DET1} \times 5}{\frac{V_{DF} + V_{OUT}}{N_{SA}} - 5} (k\Omega)$$

7.6 PRO Pin Resistors

The PRO pin sets the V_{IN} OV threshold and V_{IN} UV threshold. The resistor divider must ensure the V_{IN} OV protection at the correct bus voltage.

(EQ. 11) $$R_{B1} = \frac{V_{BUSOV} - V_{BUSOV\_R}}{V_{BUSOV\_R}} \bullet R_{B2}$$

Where V_{BUSOV} is the maximum bus voltage allowed and is usually chosen slightly above the voltage rating of the input cap, C1, but below 110% of the rated cap voltage. To minimize the power dissipation, R_{B2} is usually chosen between 5k-25kΩ. When R_{B1} and R_{B2} are chosen, the V_{IN} UV threshold is set around $V_{BUSOV}/(V_{BUSOV\_R}/V_{BUSUV\_R})$ and $V_{BUSOV}/(V_{BUSOV\_R}/V_{BUSUV\_F})$ for V_{IN} rising and falling, respectively.

7.7 PRO Pin Capacitor

The cap at the PRO pin, C_{B2}, helps filter out the noise to ensure normal operation of the IC. It also delays the voltage rise on the PRO pin when an input surge occurs so it does not trigger OV protection and keep the bulky capacitor connected to the BUS using the external FET. The capacitance of C_{B2} can be calculated according to the IEC61000-4-5 surge time specs by Equation 12, where $V_{PROMAX} = V_{ACMAX} \times 1.414 \times R_{B1}/(R_{B1}+R_{B2})$.

(EQ. 12)
$$C_{B2} > \frac{30}{\left(\frac{R_{B1} \times R_{B2}}{R_{B1} + R_{B2}}\right) \times \ln\left(1 - \frac{V_{BUSOV\_R} - V_{PROMAX}}{625 \times R_{B2}/(R_{B1}+R_{B2}) - V_{PROMAX}}\right)^{-1}} (\mu F)$$

7.8 MOSFET in Series with C1 (if used)

The MOSFET in series with C1 is turned off during the input OV, so it needs to have voltage rating of 650V so it can sustain a voltage as high as the rectified voltage of $450V_{AC}$ input. Also, it needs to survive a lightning events when a surge current passes through. Together with input surge energy absorbing components, the FET needs to have at least 200V at 10A pulse conduction rating, specified by its SOA curve. For details about the input stage design recommendation for surge energy control, refer to the *RTKA223182DR0000BU Demonstration Board Manual*.

7.9 OLV Pin Capacitor

The cap on the OLV programs the time duration when the short-time overload is allowed, which is recommended not to be more than 100ms. Use Equation 13 to calculate the cap value (C_{OVL}) using 100ms duration.

(EQ. 13)
$$C_{OLV} \le \frac{I_{OVL}}{10V_{OVL}} (\mu F)$$

7.10 HV Pin

When the maximum rectified bus voltage is less than 700V, connect the HV pin to the bus directly. If the application has a rectified voltage higher than 700V, a resistor is required between bus and the HV pin to ensure the HV pin voltage does not exceed its rating. Use Equation 14 to estimate the required resistor value.

(EQ. 14)
$$R_{HV} \ge \frac{V_{bus\_max} - 700}{0.3} (k\Omega)$$

Note: The resistor value should not be much bigger than the calculated value to ensure VCC can start up normally.

7.11 Output Capacitance

The minimum output capacitance is chosen by consideration of switching ripple, step load response, and in some applications, the required output hold-time when input is cut off.

7.12 PCB Layout Guidance

Proper layout is important to ensure a stable operation, good thermal behavior, EMI performance, and reliable operation for various operating environments. Pay attention to the following layout recommendations:

- Leave proper spacing. Recommend a minimum of 1.5mm between traces with voltage differences up to 400V and 2mm between traces with voltage differences up to 780V.
- Keep a small loop from the input bulk capacitor, transformer primary winding, D pin, S pin to the input bulk capacitor ground pin. Also keep a small loop consisting of the secondary winding, rectifier diode, and output capacitor.
- Use the star connection of ground traces as shown in the top layout picture (Figure 32). The connection point needs to be close to the IC ground pin.
- Place the VCC decoupling capacitor close to the VCC pin.
- Keep sufficient copper area on the IC drain pin (around 165mm^2 for single-phase 6W output or 3-phase 11W output) for better thermal performance.
- Make the traces connected to secondary rectifier diodes thick enough so they provide enough heat dissipation.

Figure 32 and Figure 33 show the PCB layout example.

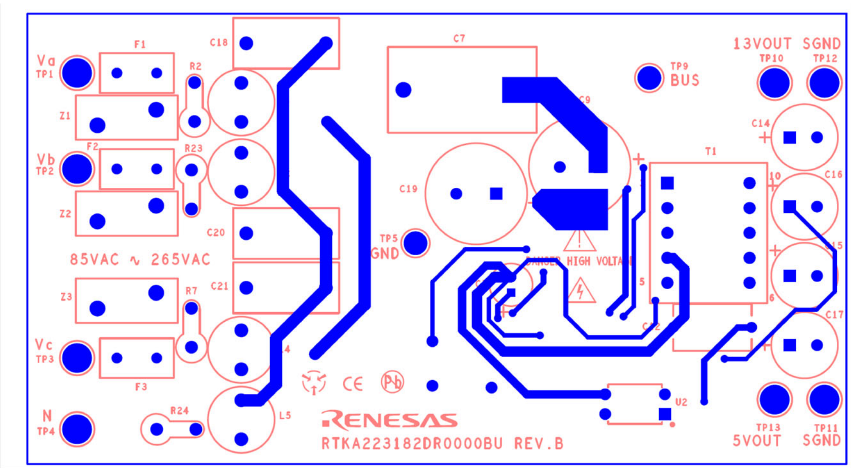


Figure 32. Top Layer

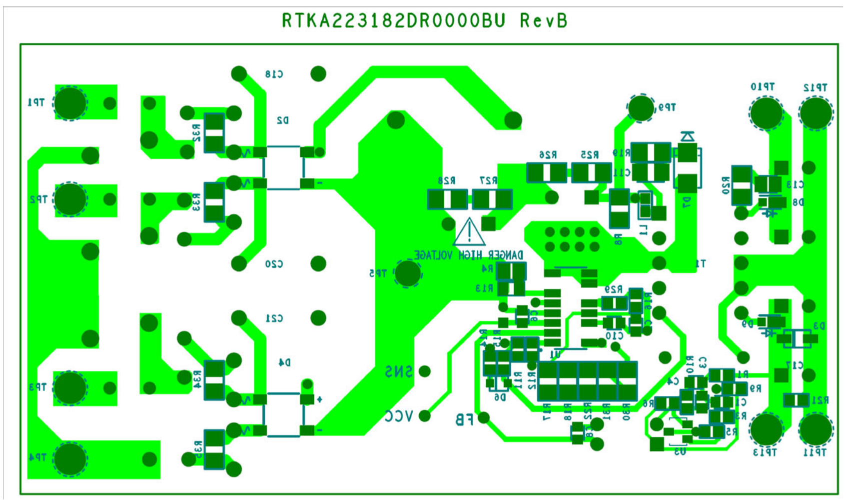


Figure 33. Bottom Layer

8. EMI Performance

Conducted EMI pre-compliance for EN55022/CISPR22 (V_{OUT} = 13V, I_{OUT} = 850mA, 3-phase input)

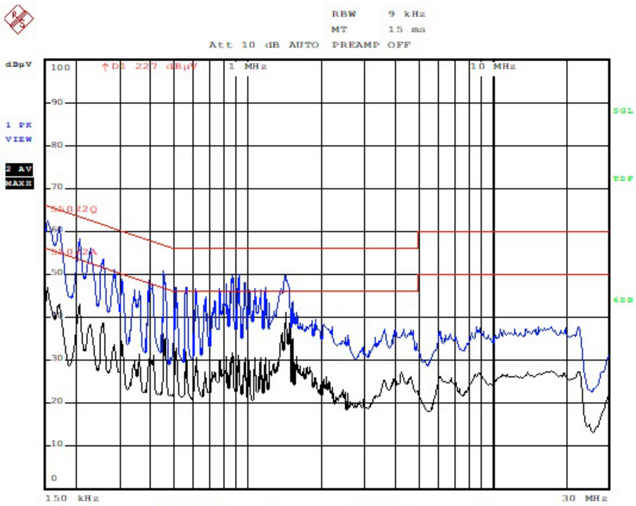


Figure 34. 207V_{AC} Phase-to-Phase, Line

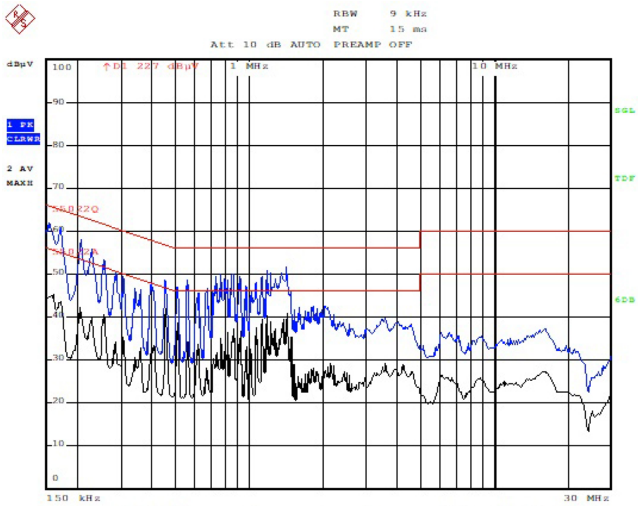


Figure 35. 207V_{AC} Phase-to-Phase, Neutral

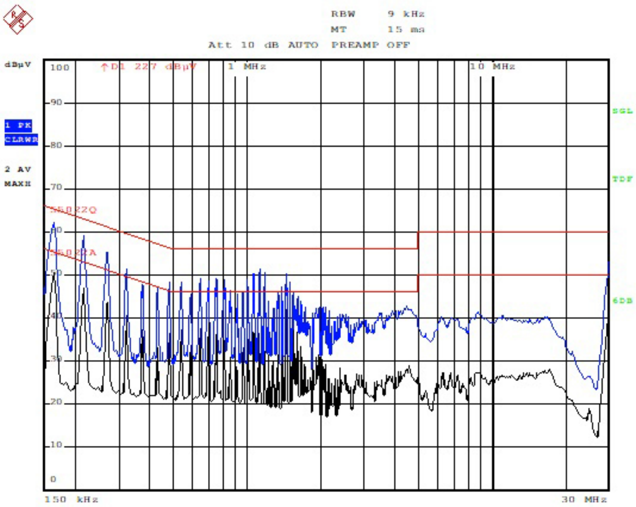


Figure 36. 276V_{AC} Phase-to-Phase, Line

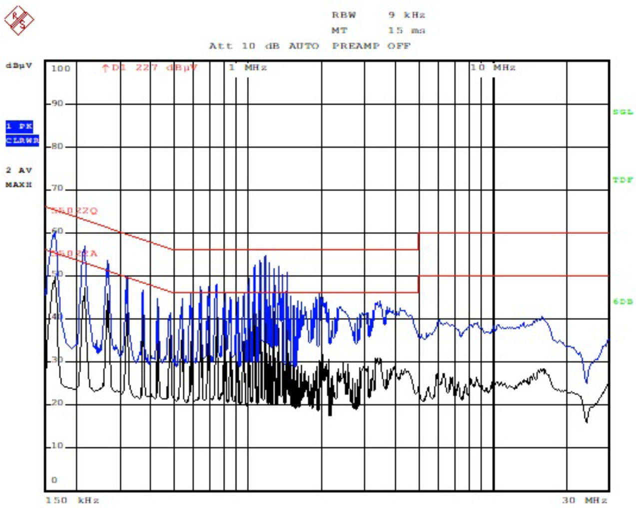
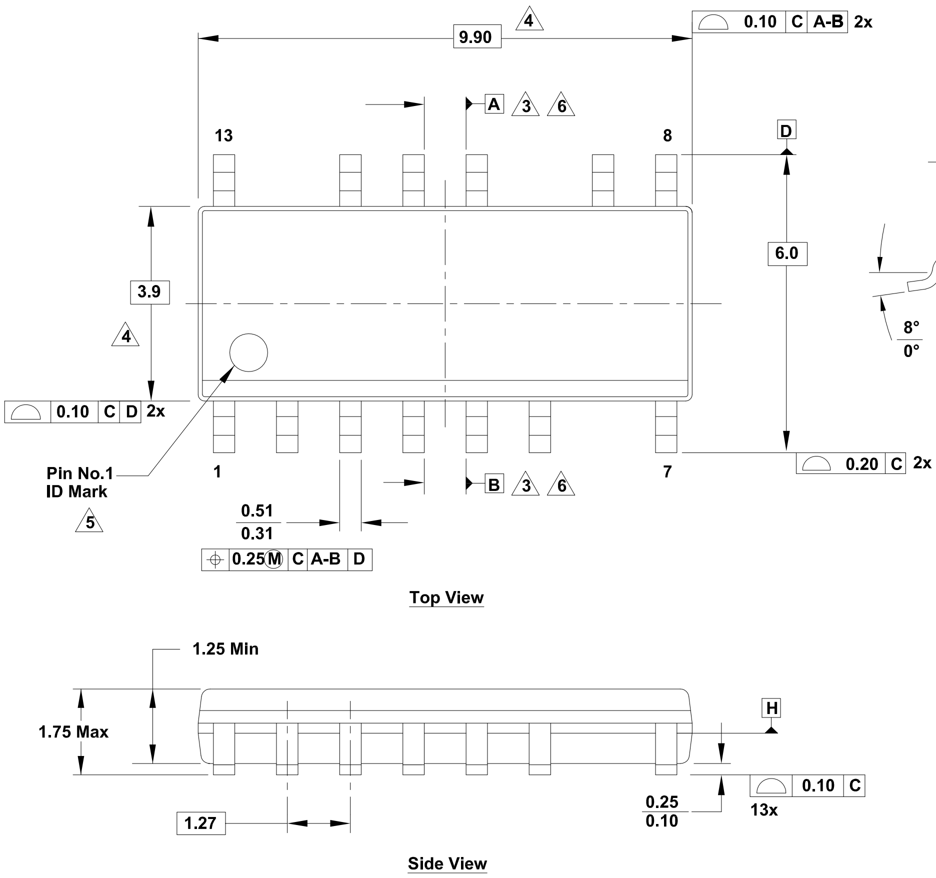


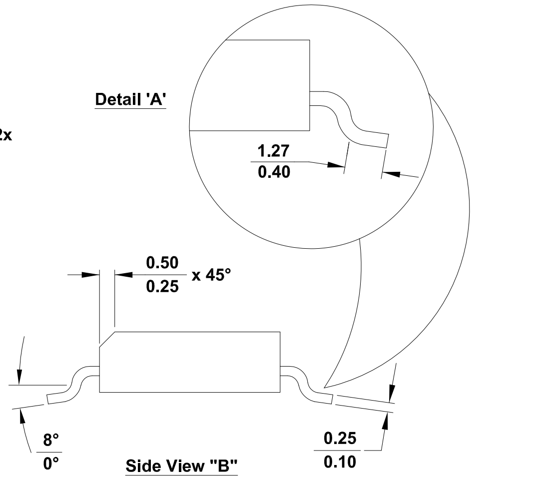
Figure 37. 276V_{AC} Phase-to-Phase, Neutral

9. Package Outline Drawing

For the most recent package outline drawing, see M13.15.

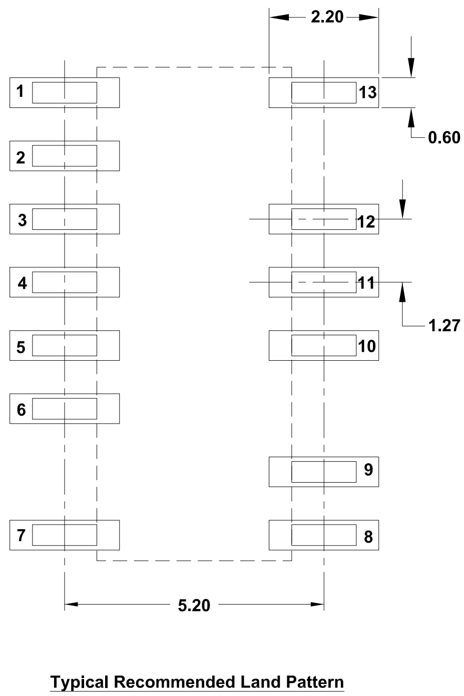
M13.15
13 Lead Narrow Body Small Outline Plastic Package
Rev 0, 6/20





Notes:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Datums A and B are determined at Datum H.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier can be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AC



Typical Recommended Land Pattern

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp Range (°C)
RAA2231824GSP#HA0	223182	SO13	M13.15	Reel, 2.5k	-40 to +150
RTKA223182DR0000BU	Demonstration Board with RAA223182 in SO13 package				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA223182 device page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, refer to TB493.
4. See TB347 for details about reel specifications.

Table 1. Key Differences of RAA22318x Products

Devices	Drain Voltage (V)	V_{IN} UV Threshold (V)	V_{IN} OV Threshold (V)	Action at V_{IN} OV
RAA223181	900	0.5/0.4	4.5/4	Stop Switching
RAA223182	1000	0.4/0.3	4.7/4.2	Stop Switching
RAA223183	1000	0.4/0.3	4.7/4.2	Keep Switching

11. Revision History

Revision	Date	Description
1.00	Jul 6, 2023	Initial release.

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www.renesas.com/contact/