

RJF0619JPE

60V, 30A Silicon N Channel Thermal FET
Power Switching

R07DS1072EJ0100
Rev.1.00
May 22, 2013

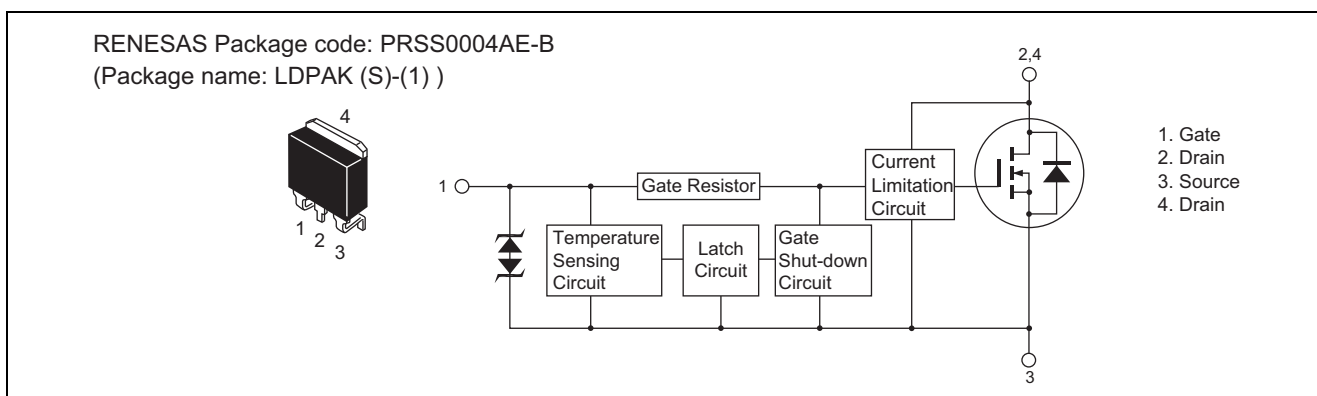
Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation (4 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Power supply voltage applies 12 V and 24 V.
- AEC-Q101 Compliant
- High endurance capability against to ESD.

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	16	V
Gate to source voltage	V_{GSS}	-2.5	V
Drain current	I_D ^{Note 3}	30	A
Body-drain diode reverse drain current	I_{DR}	30	A
Avalanche current	I_{AP} ^{Note 2}	6.7	A
Avalanche energy	E_{AR} ^{Note 2}	192	mJ
Channel dissipation	P_{ch} ^{Note 1}	50	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. Value at $T_c = 25^\circ\text{C}$
 2. $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	3.5	—	—	V	
	V_{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I_{IH1}	—	—	100	μA	$V_i = 8 V, V_{DS} = 0$
	I_{IH2}	—	—	50	μA	$V_i = 3.5 V, V_{DS} = 0$
	I_{IL}	—	—	1	μA	$V_i = 1.2 V, V_{DS} = 0$
Input current (Gate shut down)	$I_{IH(sD)1}$	—	0.8	—	mA	$V_i = 8 V, V_{DS} = 0$
	$I_{IH(sD)2}$	—	0.35	—	mA	$V_i = 3.5 V, V_{DS} = 0$
Shut down temperature	Tsd	—	175	—	°C	Channel temperature
Gate operation voltage	Vop	3.5	—	12	V	
Drain current (Current limitation value)	$I_{D \text{ limit}}$	30	—	—	A	$V_{GS} = 5 V, V_{DS} = 10 V$ ^{Note 4}

Note; 4. Pulse test

Electrical Characteristics

(Ta = 25°C)

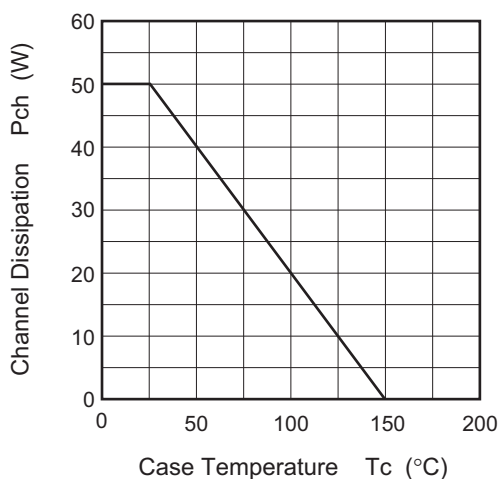
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_{D1}	—	—	45	A	$V_{GS} = 3.5 V, V_{DS} = 10 V$
	I_{D2}	—	—	10	mA	$V_{GS} = 1.2 V, V_{DS} = 10 V$
	I_{D3}	30	—	—	A	$V_{GS} = 5 V, V_{DS} = 10 V$ ^{Note 5}
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	16	—	—	V	$I_G = 800 \mu A, V_{DS} = 0$
	$V_{(BR)GSS}$	-2.5	—	—	V	$I_G = -100 \mu A, V_{DS} = 0$
Gate to source leak current	I_{GSS1}	—	—	100	μA	$V_{GS} = 8 V, V_{DS} = 0$
	I_{GSS2}	—	—	50	μA	$V_{GS} = 3.5 V, V_{DS} = 0$
	I_{GSS3}	—	—	1	μA	$V_{GS} = 1.2 V, V_{DS} = 0$
	I_{GSS4}	—	—	-100	μA	$V_{GS} = -2.4 V, V_{DS} = 0$
Input current (shut down)	$I_{GS(OP)1}$	—	0.8	—	mA	$V_{GS} = 8 V, V_{DS} = 0$
	$I_{GS(OP)2}$	—	0.35	—	mA	$V_{GS} = 3.5 V, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 32 V, V_{GS} = 0, T_c = 110^\circ C$
Gate to source cutoff voltage	$V_{GS(off)}$	1.1	—	2.1	V	$V_{DS} = 10 V, I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	12	27	—	S	$I_D = 15 \text{ A}, V_{DS} = 10 V$ ^{Note 5}
Static drain to source on state resistance	$R_{DS(on)}$	—	33	40	m Ω	$I_D = 15 \text{ A}, V_{GS} = 4 V$ ^{Note 5}
	$R_{DS(on)}$	—	25	30	m Ω	$I_D = 15 \text{ A}, V_{GS} = 10 V$ ^{Note 5}
Output capacitance	Coss	—	523	—	pF	$V_{DS} = 10 V, V_{GS} = 0, f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	3.8	—	μs	$V_{GS} = 10 V, I_D = 15 \text{ A}, R_L = 2 \Omega$
Rise time	t_r	—	13.5	—	μs	
Turn-off delay time	$t_{d(off)}$	—	4.1	—	μs	
Fall time	t_f	—	7.3	—	μs	
Body-drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_F = 30 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	110	—	ns	$I_F = 30 \text{ A}, V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu s$
Over load shut down operation time ^{Note 6}	t_{os1}	—	0.34	—	ms	$V_{GS} = 5 V, V_{DD} = 16 V$
	t_{os2}	—	0.23	—	ms	$V_{GS} = 5 V, V_{DD} = 24 V$

Notes: 5. Pulse test

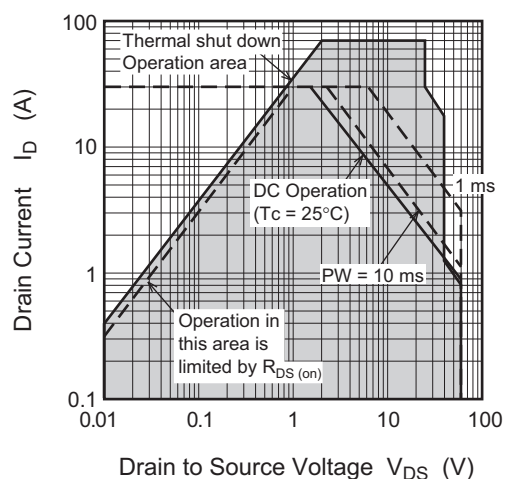
6. Including the junction temperature rise of the over loaded condition.

Main Characteristics

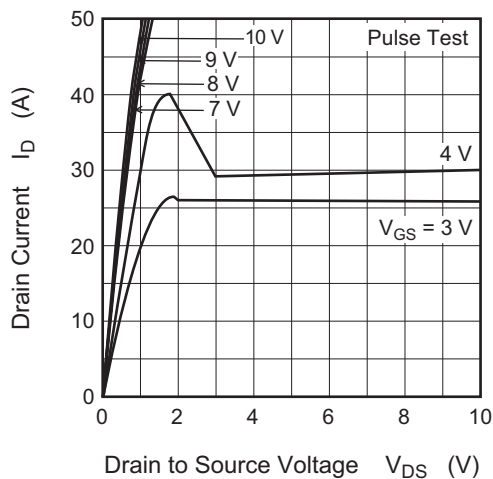
Power vs. Temperature Derating



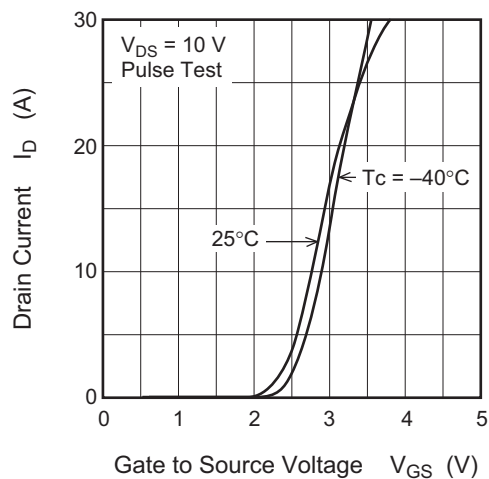
Maximum Safe Operation Area



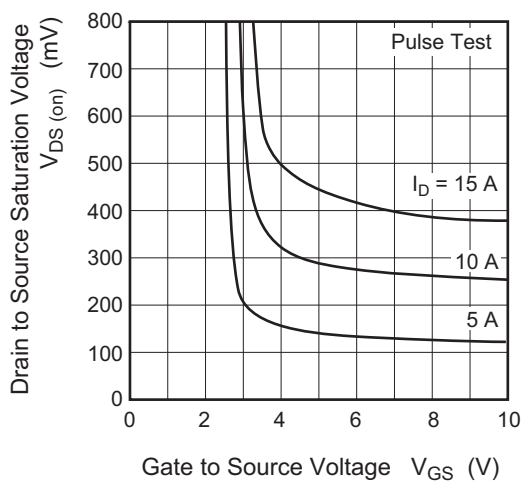
Typical Output Characteristics



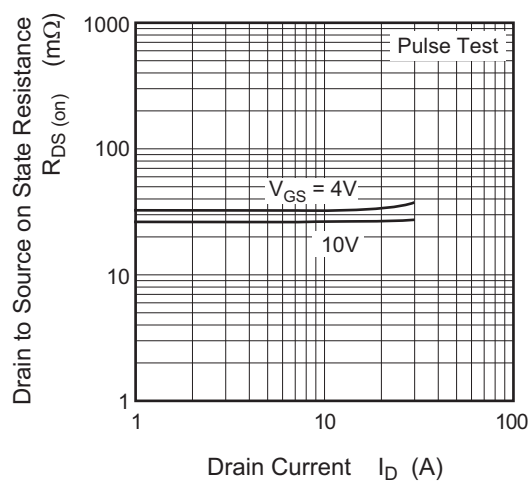
Typical Transfer Characteristics

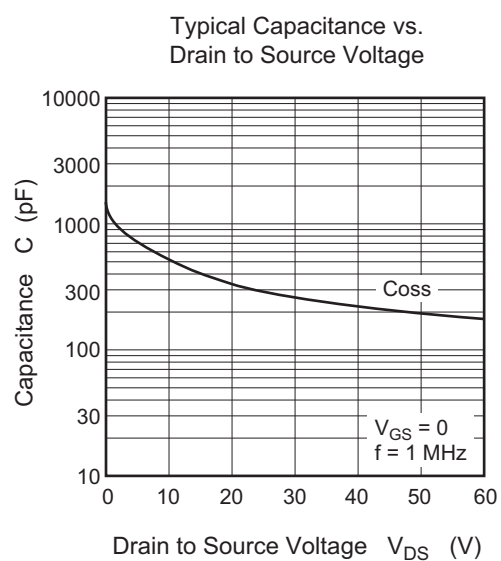
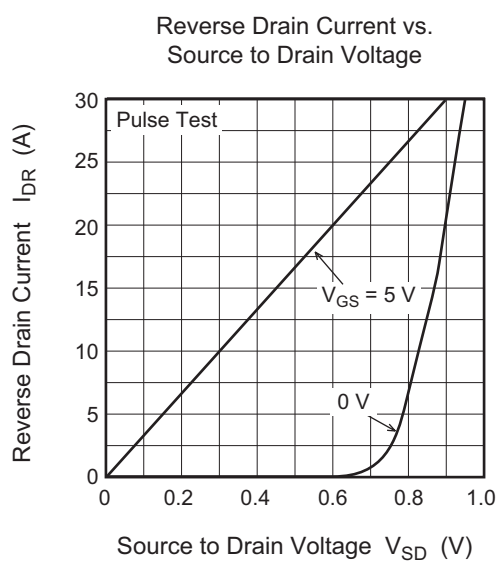
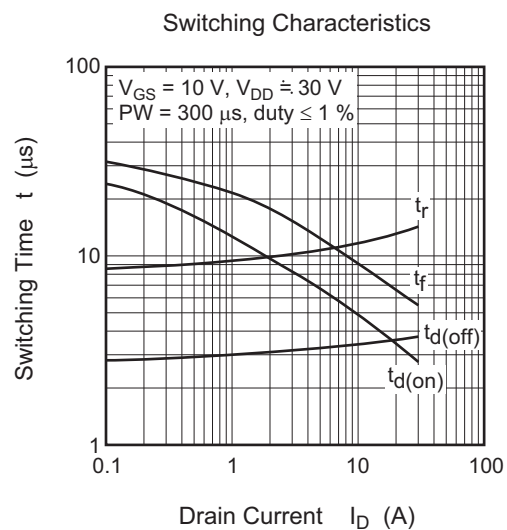
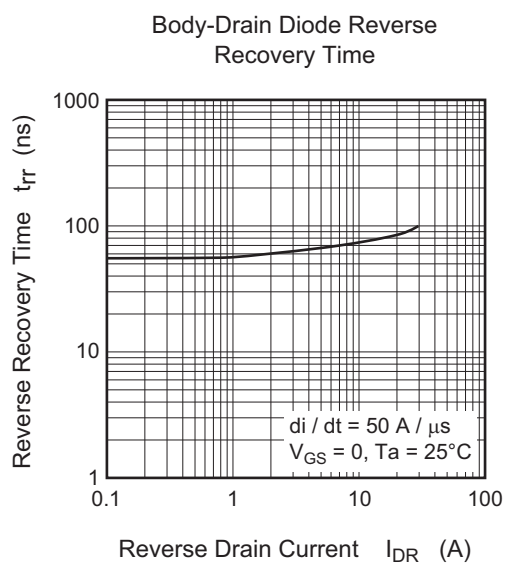
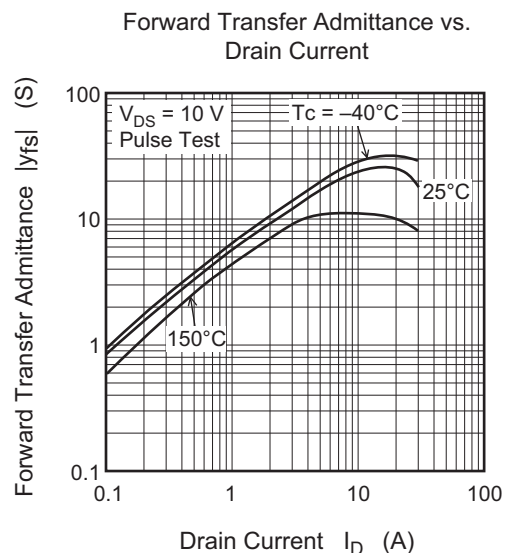
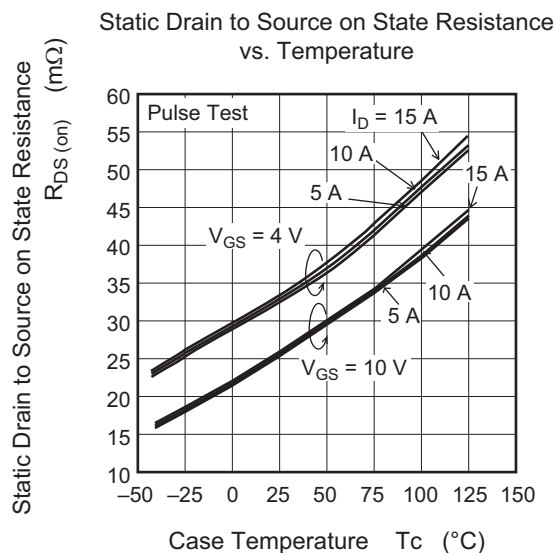


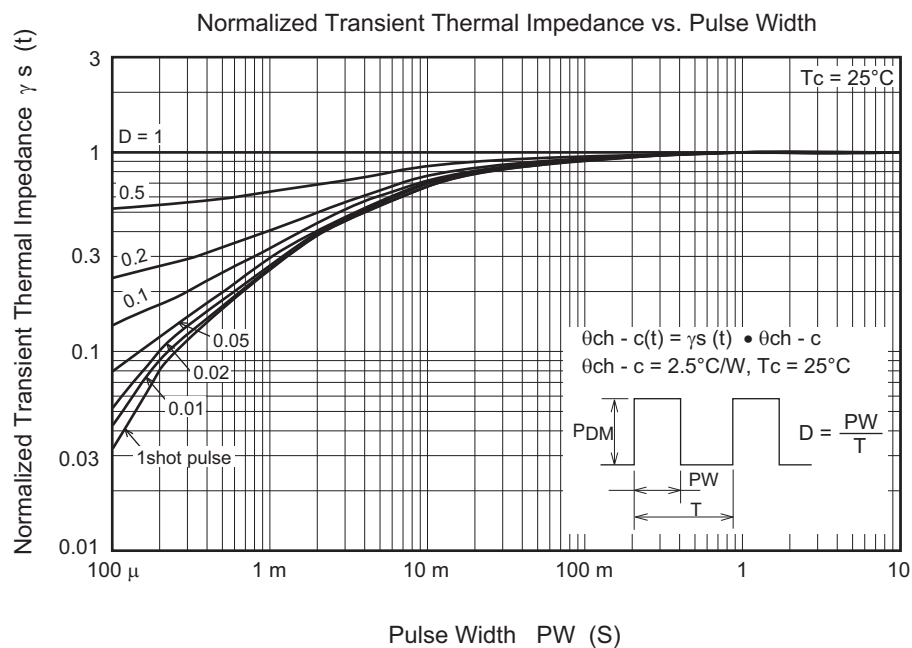
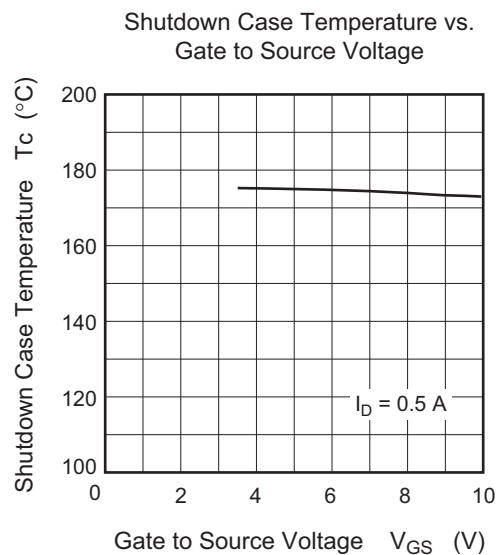
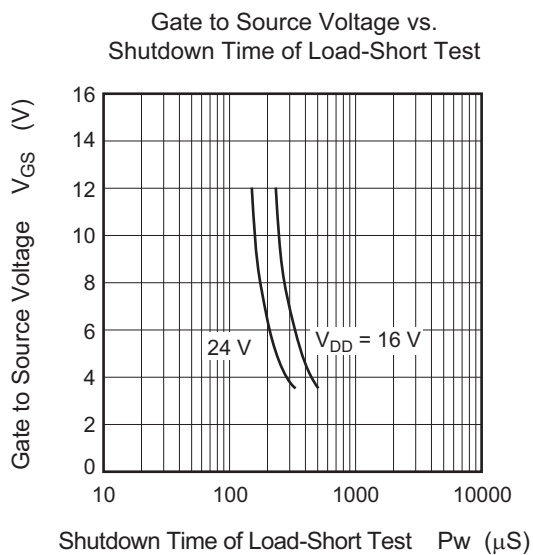
Drain to Source Saturation Voltage vs. Gate to Source Voltage



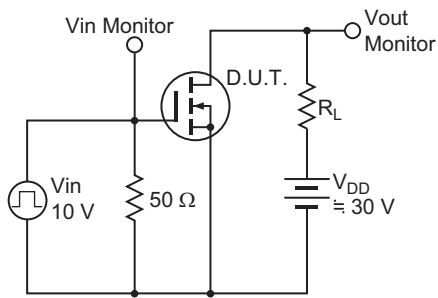
Static Drain to Source on State Resistance vs. Drain Current



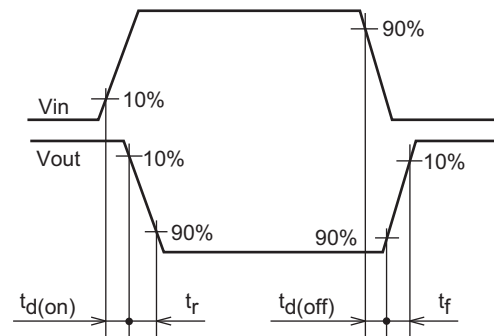




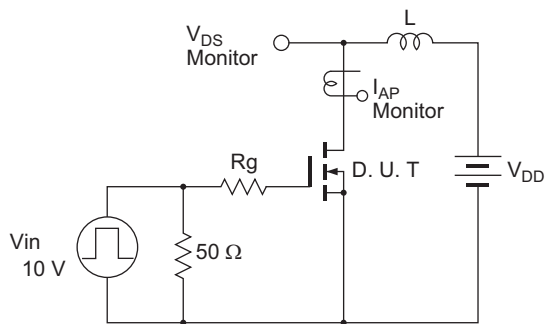
Switching Time Test Circuit



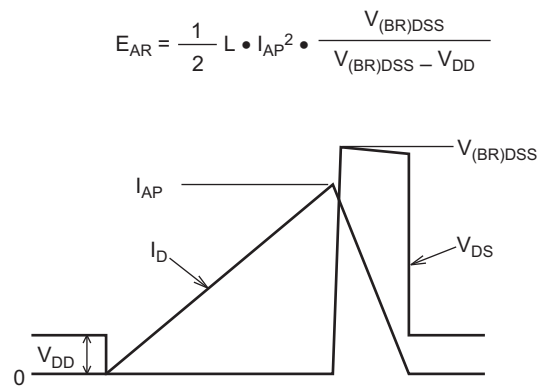
Waveform



Avalanche Test Circuit



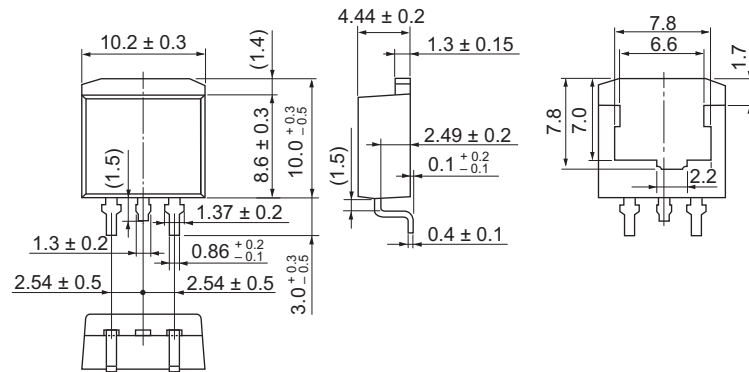
Avalanche Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBAK(S)-(1)	SC-83	PRSS0004AE-B	LDBAK(S)-(1) / LDBAK(S)-(1)V	1.30g

Unit: mm



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJF0619JPE-00-J3	1000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

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Tel: +65-6213-0200, Fax: +65-6213-0300

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