RA0E1 Group
Renesas Microcontrollers

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Ultra low power 32 MHz Arm® Cortex®-M23 core, up to 64-KB code flash memory, 12-KB SRAM, 12-bit A/D Converter, Serial interfaces and Safety features.

Features

■ Arm Cortex-M23 Core

- Armv8-M architecture
- Maximum operating frequency: 32 MHz
- Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

■ Memory

- Up to 64-KB code flash memory
- 1-KB data flash memory (100,000 program/erase cycles)
- 12-KB SRAM
- Flash read protection (FRP)
- 128-bit unique ID

■ Connectivity

- Serial Array Unit (SAU)
  - Simplified SPI × 3
  - Simplified IIC × 3
  - UART × 2
  - UART (LIN-bus supported) × 1
- Serial Interface UARTA (UARTA) × 1
- I^{2}C Bus interface (IICA) × 1

■ Analog

- 12-bit A/D Converter (ADC12)
- Temperature Sensor (TSN)

■ Timers

- 16-bit Timer Array Unit (TAU) × 8
- 32-bit interval timer (TML32) × 1
  - 1 channel in 32-bit counter mode
  - 2 channels in 16-bit counter mode
  - 4 channels in 8-bit counter mode

■ Safety

- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Cyclic Redundancy Check (CRC)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Illegal memory access detection

■ Security

- True Random Number Generator (TRNG)

■ System and Power Management

- Low power modes
- Realtime Clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Multiple Clock Sources

- Main clock oscillator (MOSC) （1 to 20 MHz）
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (24/32 MHz)
- Middle-speed on-chip oscillator (MOCO) (4 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ Up to 29 pins for general I/O ports

- 5-V tolerance, open drain, input pull-up

■ Operating Voltage

- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 32-pin HWQFN (5 mm × 5 mm, 0.5 mm pitch)
  - 24-pin HWQFN (4 mm × 4 mm, 0.5 mm pitch)
  - 20-pin LSSOP (4.4 mm × 6.5 mm, 0.65 mm pitch)
  - 16-pin HWQFN (3 mm × 3 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M23 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 64-KB code flash memory
- 12-KB SRAM
- Serial Interface (SAU, UARTA, IICA)
- General Purpose Timer (TAU, TML32)
- 12-bit A/D Converter (ADC12)

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M23 core	● Maximum operating frequency: up to 32 MHz ● Arm Cortex-M23 core: – Revision: r1p0-00rel0 – Armv8-M architecture profile – Single-cycle integer multiplier – 19-cycle integer divider ● SysTick timer: – Driven by SYSTICCLK (LOCO) or ICLK

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 64-KB of code flash memory.
Data flash memory	1-KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with parity bit.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Operating mode: ● Single-chip mode
Resets	The MCU provides 7 resets (RES pin reset, power-on reset, independent watchdog timer reset, voltage monitor 0/1 resets, SRAM parity error reset, software reset).
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of two separate voltage level detectors (LVD0, LVD1). LVD0 and LVD1 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	● Main clock oscillator (MOSC) ● Sub-clock oscillator (SOSC) ● High-speed on-chip oscillator (HOCO) ● Middle-speed on-chip oscillator (MOCO) ● Low-speed on-chip oscillator (LOCO) ● Clock output / Buzzer output support
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.

Table 1.3 System (2 of 2)

Feature	Functional description
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Flash Read Protection	The MCU incorporates the flash read protection with one secure regions that include the code flash. The secure region can be protected from non-secure program accesses. A non-secure program cannot access a protected region.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with the LOCO, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.6 Timers

Feature	Functional description
Timer Array Unit (TAU)	The timer array unit has eight 16-bit timers.Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more channels can be used to create a high-resolution timer.
32-bit Interval Timer (TML32)	The 32-bit interval timer is made up of four 8-bit interval timers (referred to as channels 0 to 3). Each is capable of operating independently and in that case they all have the same functions. Two 8-bit interval timer channels can be connected to operate as a 16-bit interval timer. Four 8-bit interval timer channels can be connected to operate as a 32-bit interval timer.
Realtime Clock (RTC)	The Realtime Clock (RTC) has the following features. ● Capable of counting years, months, days of the week, dates, hours, minutes, and seconds, for up to 99 years ● Fixed-cycle interrupt (with period selectable from among 0.5 of a second, 1 second, 1 minute, 1 hour, 1 day, or 1month) ● Alarm interrupt (alarm set by day of week, hour, and minute) ● Pin output function of 1 Hz

Table 1.7 Communication interfaces

Feature	Functional description
Serial Array Unit (SAU)	A Serial Array Unit (SAU) has up to four channels. Each channel can achieve simplified SPI, UART, and simplified IIC communication.
I^{2}C Bus Interface (IICA)	The I^{2}C Bus Interface (IICA) has 1 channel. The IICA module conforms I^{2}C (Inter-Integrated Circuit) Bus Interface functions.
Serial Interface UARTA (UARTA)	The Serial Interface UARTA (UARTA) has 1 channel. UARTA performs an asynchronous communication.

Table 1.8 Analog (1 of 2)

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter is provided. Up to 10 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.

Table 1.8 Analog (2 of 2)

Feature	Functional description
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.9 Data processing

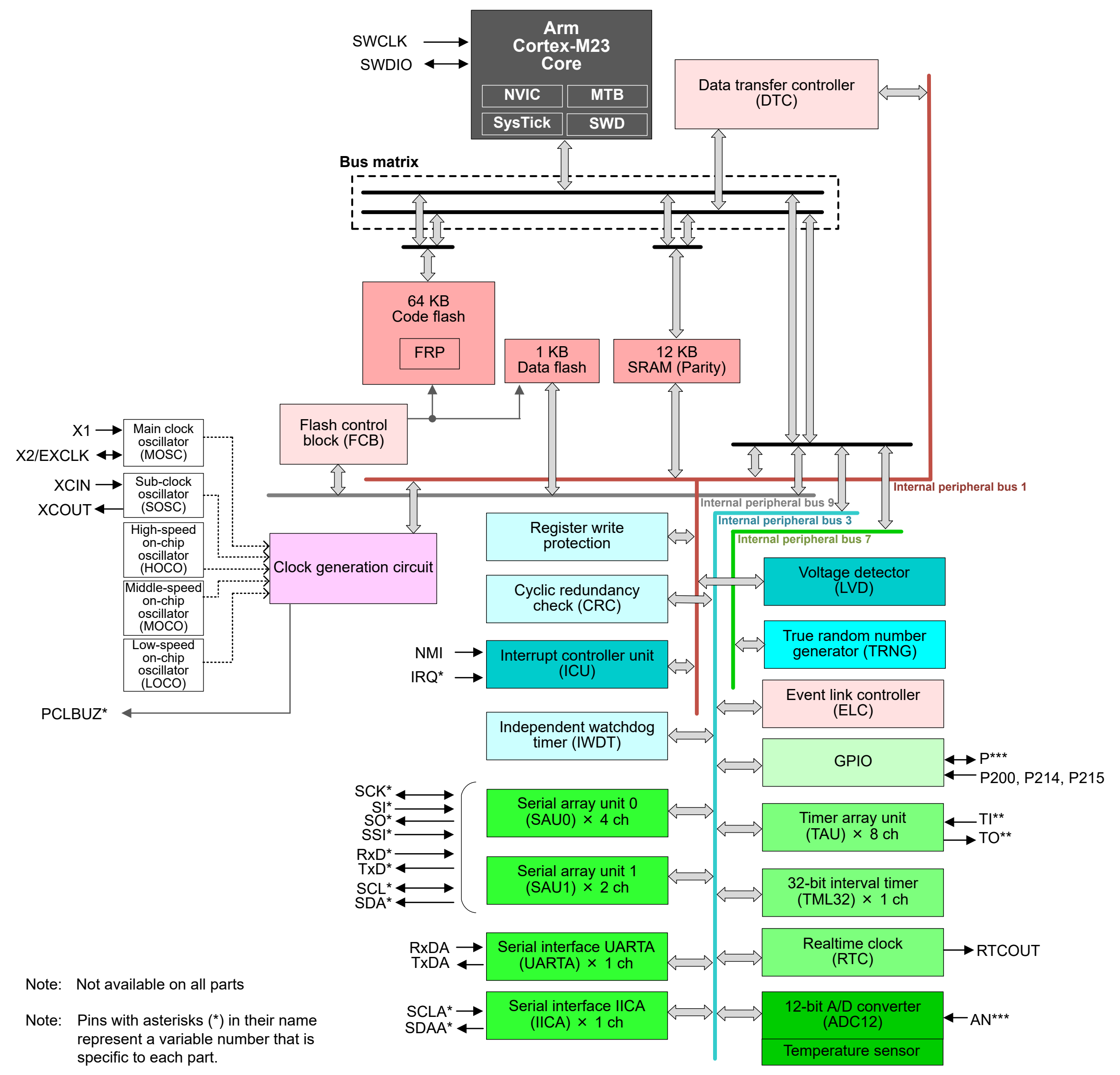
Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. Two CRC-generation polynomials (CRC-CCITT, CRC-32) are available.

Table 1.10 I/O ports

Feature	Functional description
I/O ports	● I/O ports for the 32-pin LQFP/HWQFN – I/O pins: 26 – Input pins: 3 – Pull-up resistors: 16 – N-ch open-drain outputs: 15 – 5-V tolerance: 2 ● I/O ports for the 24-pin HWQFN – I/O pins: 20 – Input pins: 1 – Pull-up resistors: 12 – N-ch open-drain outputs: 11 – 5-V tolerance: 2 ● I/O ports for the 20-pin LSSOP – I/O pins: 16 – Input pins: 1 – Pull-up resistors: 12 – N-ch open-drain outputs: 9 ● I/O ports for the 16-pin HWQFN – I/O pins: 12 – Input pins: 1 – Pull-up resistors: 9 – N-ch open-drain outputs: 6

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.



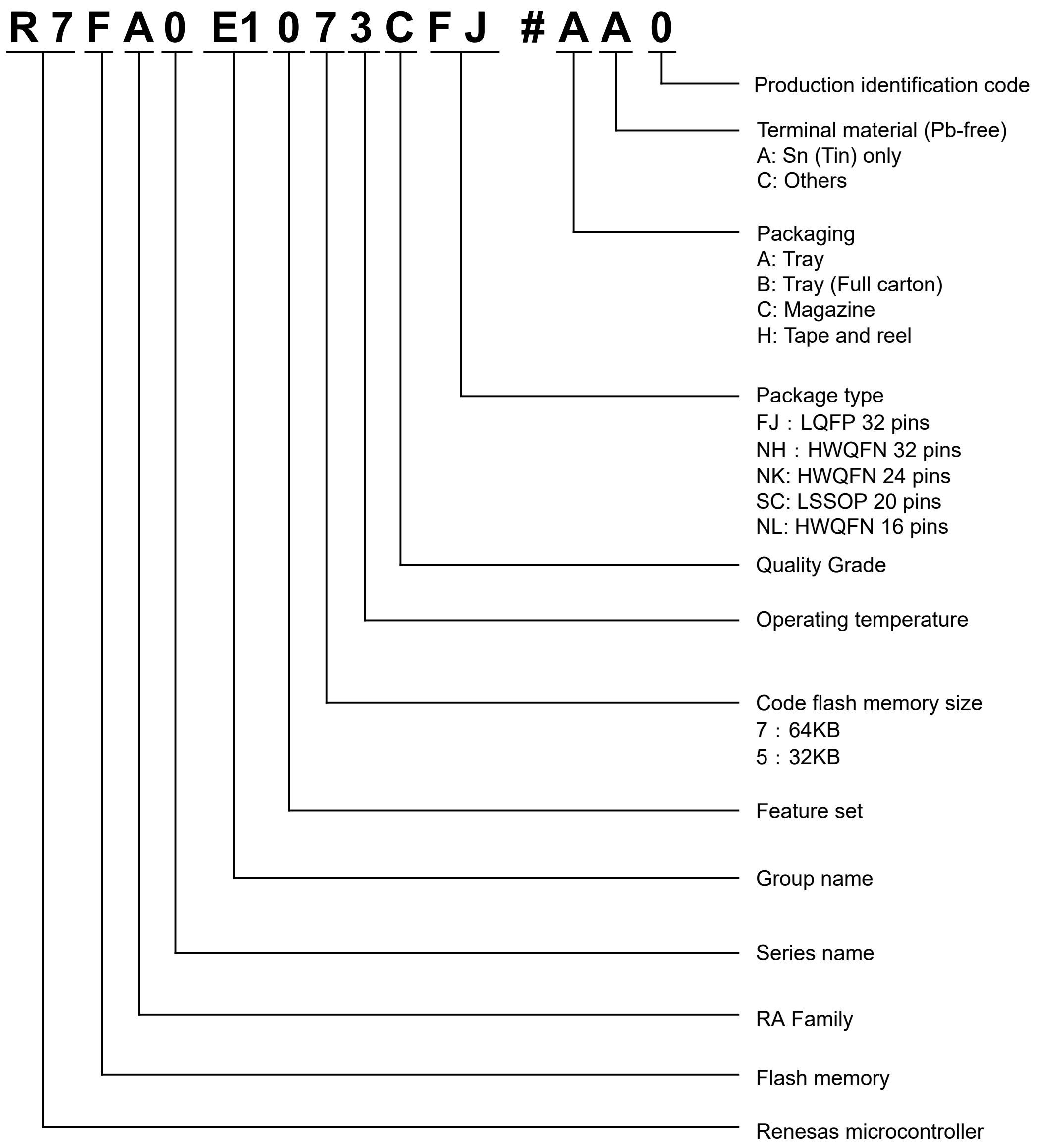
Note: Not available on all parts

Note: Pins with asterisks (*) in their name represent a variable number that is specific to each part.

Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.11 shows a list of products.



Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.11 Product list (1 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA0E1073CFJ	PLQP0032GB-A	64 KB	1 KB	12 KB	-40 to +105°C
R7FA0E1073CNH	PWQN0032KE-A				
R7FA0E1073CNK	PWQN0024KG-A				
R7FA0E1073CSC	PLSP0020JB-A				
R7FA0E1073CNL	PWQN0016KD-A				

Table 1.11 Product list (2 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA0E1053CFJ	PLQP0032GB-A	32 KB	1 KB	12 KB	-40 to +105°C
R7FA0E1053CNH	PWQN0032KE-A				
R7FA0E1053CNK	PWQN0024KG-A				
R7FA0E1053CSC	PLSP0020JB-A				
R7FA0E1053CNL	PWQN0016KD-A				

1.4 Function Comparison

Table 1.12 Function comparison

Parts number		**R7FA0E1073CFJ** **R7FA0E1073CNH**	**R7FA0E1053CFJ** **R7FA0E1053CNH**	**R7FA0E1073CNK**	**R7FA0E1053CNK**	**R7FA0E1073CSC**	**R7FA0E1053CSC**	**R7FA0E1073CNL**	**R7FA0E1053CNL**
Pin count		32		24		20		16	
Package		LQFP/HWQFN		HWQFN		LSSOP		HWQFN	
Code flash memory		64 KB	32 KB	64 KB	32 KB	64 KB	32 KB	64 KB	32 KB
Data flash memory		1 KB		1 KB		1 KB		1 KB	
SRAM(Parity)		12 KB		12 KB		12 KB		12 KB	
System	CPU clock	32 MHz		32 MHz		32 MHz		32 MHz	
	Sub clock oscillator	Yes		Yes (CMC.XTSEL=1)		Yes (CMC.XTSEL=1)		Yes (CMC.XTSEL=1)	
	ICU	Yes		Yes		Yes		Yes	
Event control	ELC	Yes		Yes		Yes		Yes	
DMA	DTC	Yes		Yes		Yes		Yes	
Timers	TAU	8 (PWM outputs: 7)		8 (PWM outputs: 7)		8 (PWM outputs: 7)		8 (PWM outputs: 7)	
	TML32	1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)		1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)		1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)		1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)	
	RTC	Yes		Yes		Yes		Yes	
	IWDT	Yes		Yes		Yes		Yes	
Communication	SAU	3 (simplified SPI), 3 (simplified IIC), 2 (UART), 1 (UART supporting LIN-bus)		3 (simplified SPI), 3 (simplified IIC), 2 (UART), 1 (UART supporting LIN-bus)		3 (simplified SPI), 3 (simplified IIC), 2 (UART), 1 (UART supporting LIN-bus)		2 (simplified SPI), 2 (simplified IIC), 2 (UART)	
	UARTA	1		1		1		1	
	IICA	1		1		1		1	
Analog	ADC12	10		8		6		5	
	TSN	Yes		Yes		Yes		Yes	
Data processing	CRC	Yes		Yes		Yes		Yes	
Security		TRNG		TRNG		TRNG		TRNG	
I/O ports	I/O pins	26		20		16		12	
	Input pins	3		1		1		1	
	Pull-up resistors	16		12		12		9	
	N-ch open-drain outputs	15		11		9		6	
	5-V tolerance	2		2		—		—	

1.5 Pin Functions

Table 1.13 Pin functions (1 of 2)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-µF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	X2	I/O	Pins for a crystal resonator. An external clock signal can be input through the X2 pin.
	X1	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	PCLBUZ0	Output	Clock output / Buzzer output
	EXCLK	Input	External clock input for the main clock
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ5	Input	Maskable interrupt request pins
TAU	TI00 to TI07	Input	Pins for inputting an external counting clock/capture trigger to 16-bit timers 00 to 07
	TO00 to TO07	I/O	Timer output pins for 16-bit timers 00 to 07
RTC	RTCOUT	Output	Output pin for 1-Hz clock
IICA	SCLAn (n = 0)	I/O	Input/output pins for the clock
	SDAAn (n = 0)	I/O	Input/output pins for data
SAU	SCK00, SCK11, SCK20	I/O	Serial clock I/O pins for serial interfaces SPI00, SPI11 and SPI20
	SI00, SI11, SI20	Input	Serial data input pins for serial interfaces SPI00, SPI11 and SPI20
	SO00, SO11, SO20	Output	Serial data output pins for serial interfaces SPI00, SPI11, and SPI20
	SSI00	Input	Chip select pin for serial interfaces SPI00
	SCL00, SCL11, SLC20	Output	Serial clock output pins for serial interfaces IIC00, IIC11, and IIC20
	SDA00, SDA11, SDA20	I/O	Serial data I/O pins for serial interfaces IIC00, IIC11, and IIC20
	RXD0, RXD1, RXD2	Input	Serial data input pins for serial interfaces UART0, UART1, and UART2
	TXD0, TXD1, TXD2	Output	Serial data output pins for serial interfaces UART0, UART1, and UART2
UARTA	RXDAn (n = 0)	Input	Serial data input pin for the UARTA serial interface
	TXDAn (n = 0)	Output	Serial data output pin for the UARTA serial interface
Analog power supply	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to VCC when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12.
ADC12	AN000 to AN007, AN021 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter.

Table 1.13 Pin functions (2 of 2)

Function	Signal	I/O	Description
I/O ports	P008 to P015	I/O	General-purpose input/output pins
	P100 to P103, P108 to P110, P112	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P206 to P208, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300	I/O	General-purpose input/output pins
	P407	I/O	General-purpose input/output pins
	P913, P914	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.6 show the pin assignments from the top view.

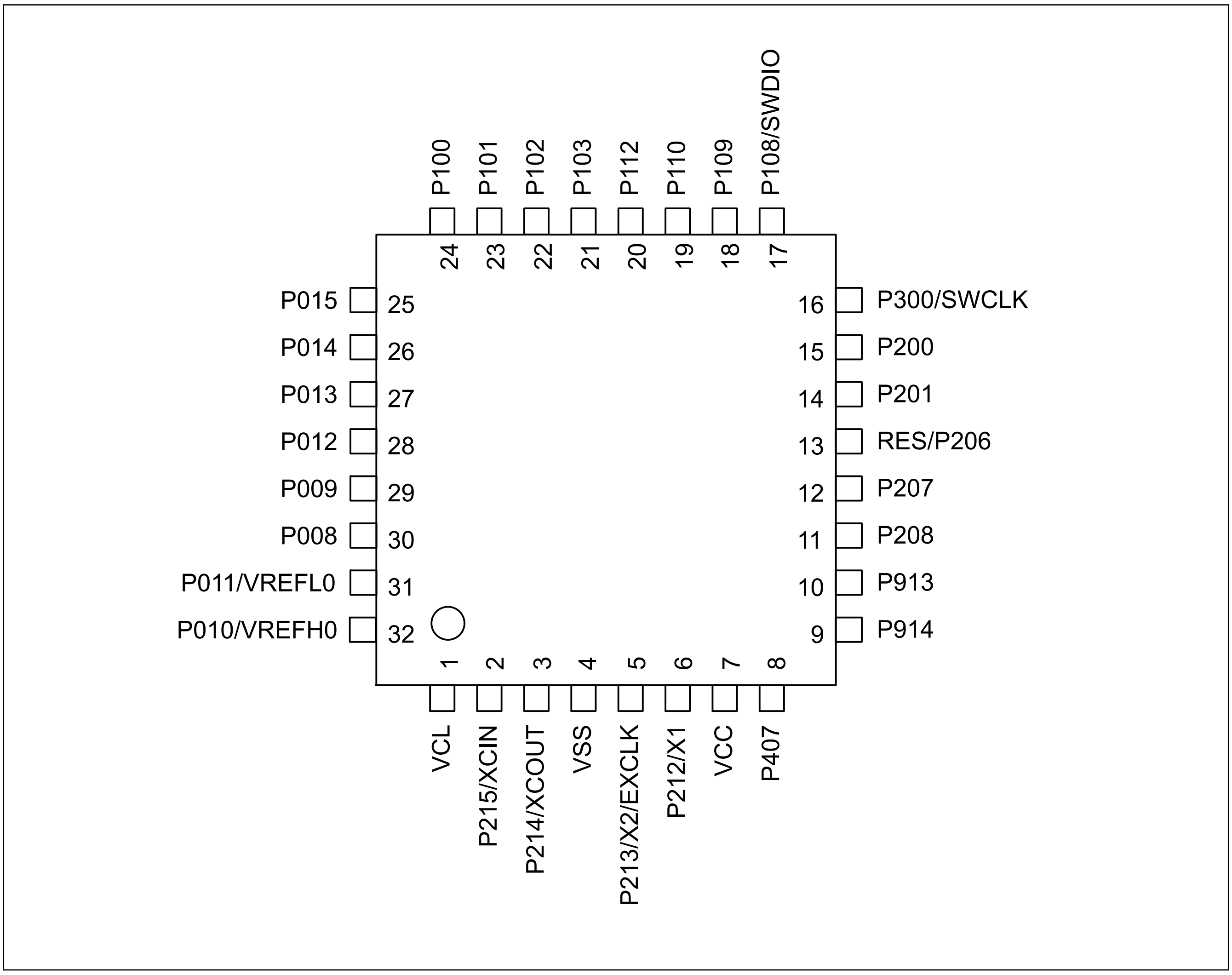
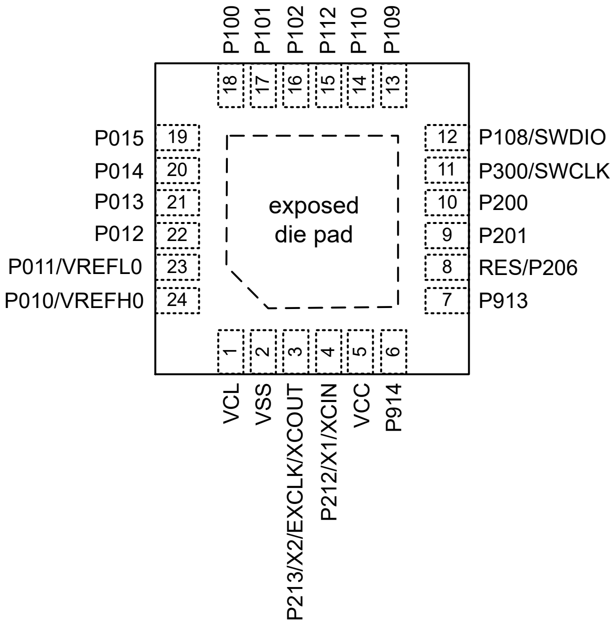


Figure 1.3 Pin assignment for LQFP / HWQFN 32-pin (top view)

Note: For the QFN package product, solder the exposed die pad to the PCB.
The potential of the exposed die pad is recommended to design as electrically open.



Note: For the QFN package product, solder the exposed die pad to the PCB.
The potential of the exposed die pad is recommended to design as electrically open.

Figure 1.4 Pin assignment for HWQFN 24-pin (top view)

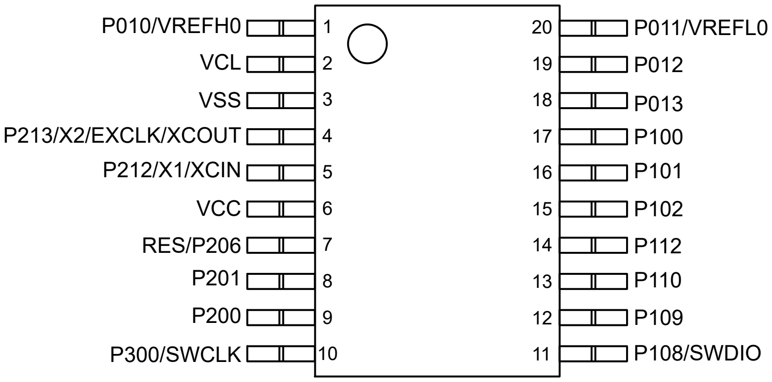
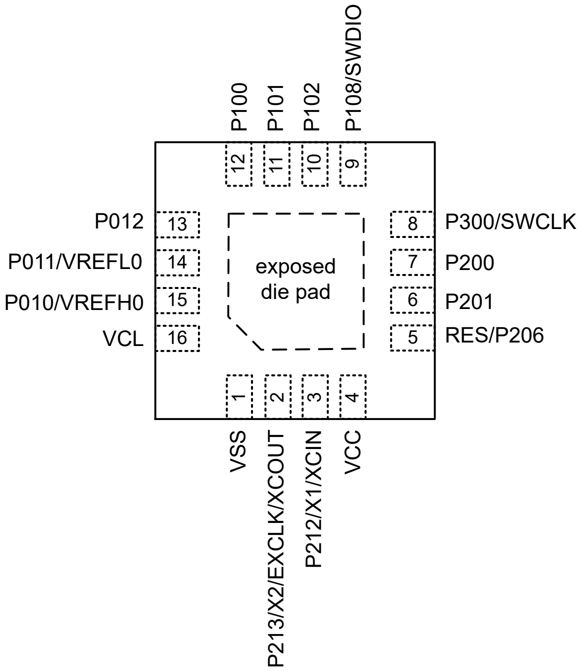


Figure 1.5 Pin assignment for LSSOP 20-pin (top view)



Note: For the QFN package product, solder the exposed die pad to the PCB.
The potential of the exposed die pad is recommended to design as electrically open.

Figure 1.6 Pin assignment for HWQFN 16-pin (top view)

1.7 Pin Lists

Table 1.14 Pin list

Pin number				Power, System, Clock, Debug	I/O ports	Interrupt	Timers		Communication interfaces			Analogs
32-pin	24-pin	20-pin	16-pin				TAU	RTC	SAU	UARTA	IICA	ADC
1	1	2	16	VCL	—	—	—	—	—	—	—	—
2	—	—	—	XCIN	P215	—	—	—	—	—	—	—
3	—	—	—	XCOUT	P214	—	—	—	—	—	—	—
4	2	3	1	VSS	—	—	—	—	—	—	—	—
5	3	4	2	X2/EXCLK/ XCOUT[1]	P213	IRQ0_B	TI00_A/TI02_B/ TO02_B	—	TXD1_A/ SO11_A	TXDA0_B	SDAA0_B	—
6	4	5	3	X1/XCIN[1]	P212	IRQ1_B	TO00_A/ TI03_C/TO03_C	—	RXD1_A/ SI11_A/ SDA11_A	RXDA0_B	SCLA0_B	—
7	5	6	4	VCC	—	—	—	—	—	—	—	—
8	—	—	—	PCLBUZ0_C	P407	IRQ4_C	—	RTCOUT_A	SCK11_A/ SCL11_A	—	—	—
9	6	—	—	—	P914	—	—	—	—	—	SCLA0_A	—
10	7	—	—	—	P913	—	—	—	—	—	SDAA0_A	—
11	—	—	—	—	P208	IRQ3_C	TI00_B	—	—	TXDA0_A	—	—
12	—	—	—	—	P207	IRQ2_C	TO00_B	—	—	RXDA0_A	—	—
13	8	7	5	RES	P206	—	—	—	—	—	—	—
14	9	8	6	PCLBUZ0_A	P201	IRQ5_B	TI05_B/TO05_B	RTCOUT_B	SSI00_B/ SCK11_B/ SCL11_B	—	—	—
15	10	9	7	—	P200	IRQ0_A/NMI	—	—	—	—	—	—
16	11	10	8	SWCLK	P300	—	TI04_B/TO04_B	—	—	—	—	—
17	12	11	9	SWDIO	P108	—	TI03_B/TO03_B	—	—	—	—	—
18	13	12	—	—	P109	IRQ4_B	TI02_A/TO02_A	—	TXD2_A/ SO20_A	TXDA0_C	SDAA0_C	—
19	14	13	—	—	P110	IRQ3_B	TI01_A/TO01_A	—	RXD2_A/ SI20_A/ SDA20_A	RXDA0_C	SCLA0_C	—
20	15	14	—	—	P112	IRQ2_B	TI03_A/TO03_A	—	SCK20_A/ SCL20_A/ SSI00_C	—	—	—
21	—	—	—	—	P103	IRQ5_A	TI05_A/TO05_A	—	SSI00_A	—	—	—
22	16	15	10	PCLBUZ0_B	P102	IRQ4_A	TI06_A/ TO06_A/ TO00_C	RTCOUT_C	SCK00_A/ SCL00_A	—	—	—
23	17	16	11	—	P101	IRQ3_A	TI07_A/ TO07_A/TI00_C	—	TXD0_A/ SO00_A	TXDA0_D	SDAA0_D	AN021
24	18	17	12	—	P100	IRQ2_A	TI04_A/ TO04_A/ TI01_B/TO01_B	—	RxD0_A/ SI00_A/ SDA00_A	RXDA0_D	SCLA0_D	AN022
25	19	—	—	—	P015	IRQ1_A	—	—	—	—	—	AN007
26	20	—	—	—	P014	—	—	—	—	—	—	AN006
27	21	18	—	—	P013	—	—	—	—	—	—	AN005
28	22	19	13	—	P012	—	—	—	—	—	—	AN004
29	—	—	—	—	P009	—	—	—	—	—	—	AN003
30	—	—	—	—	P008	—	—	—	—	—	—	AN002
31	23	20	14	VREFL0	P011	—	—	—	—	—	—	AN001
32	24	1	15	VREFH0	P010	—	—	—	—	—	—	AN000

Note 1. When setting CMC.XTSEL = 1 for 24-, 20-, and 16-pin products

Note: Some signal names have _A, _B, _C, _D, _E, or _F suffixes, but these suffixes can be ignored when assigning functionality, except for SAU and IICA. For SAU and IICA, only signals, except for SCL11 and SCK11, bearing the same suffix can be selected. The simultaneous use of the same signal with different suffixes is prohibited.

2. Electrical Characteristics

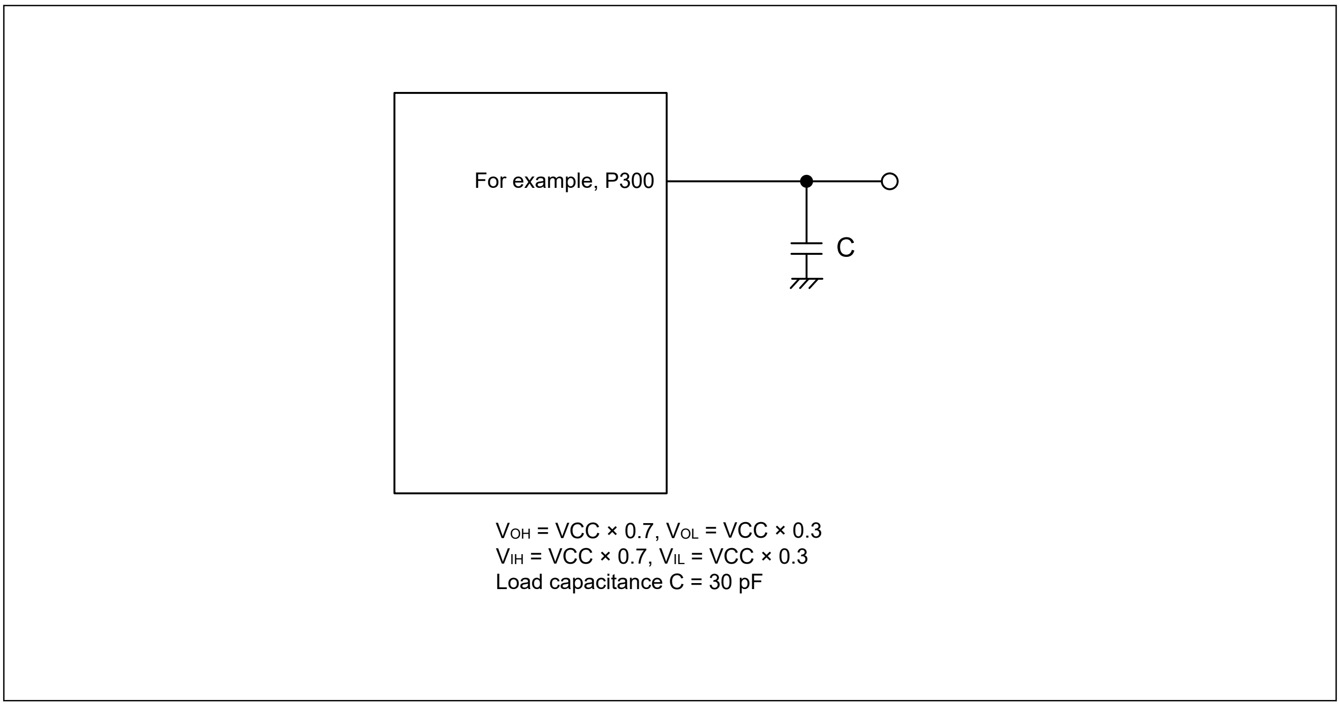
Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC^{*1} = VREFH0 = 1.6 to 5.5 V

VSS = VREFL0 = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.

Figure 2.1 shows the timing conditions.



V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
Load capacitance C = 30 pF

Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC characteristics of each function are not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
VCL pin input voltage		V_{IVCL}	-0.3 to +2.1 and -0.3 to VCC + 0.3^{*1}	V
Input voltage	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407	V_I1	-0.3 to VCC + 0.3	V
	P913, P914 (5 V tolerant)	V_I2	-0.3 to +6.5	V
	P008 to P015, P212 to P215	V_I3	-0.3 to VCC + 0.3	V
Output voltage	P100 to P103, P108 to P110, P112, P201, P206 to P208, P300, P407	V_O1	-0.3 to VCC + 0.3	V
	P913, P914 (N-ch open-drain)	V_O2	-0.3 to +6.5	V
	P008 to P015, P212, P213	V_O3	-0.3 to VCC + 0.3^{*2}	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter			Symbol	Value	Unit
Analog input voltage	AN000 to AN007		$V_{AI}1$	-0.3 to VCC + 0.3 and -0.3 to VREFH0 + 0.3[*2] [*3]	V
	AN021 to AN022		$V_{AI}2$	-0.3 to VCC + 0.3 and -0.3 to VREFH0 + 0.3[*2] [*3]	V
High-level output current	P100 to P103, P108 to P110, P112, P201 to P207, P208, P300, P407	Per pin	$I_{OH}1$	-40	mA
		Total of all pins		-100	mA
	P008 to P015, P212, P213	Per pin	$I_{OH}2$	-5	mA
		Total of all pins		-20	mA
Low-level output current	P100 to P103, P108 to P110, P112, P201, P206 to P208, P300, P407, P913, P914	Per pin	$I_{OL}1$	40	mA
		Total of all pins		100	mA
	P008 to P015, P212, P213	Per pin	$I_{OL}2$	10	mA
		Total of all pins		20	mA
Ambient operating temperature	In normal operation mode		Ta	-40 to +105	°C
	In flash memory programming mode			-40 to +105	°C
Storage temperature			Tstg	-65 to +150	°C

Note 1. Connect the VCL pin to VSS via a capacitor (0.47 to 1 µF). The listed value is the absolute maximum rating of the VCL pins. Only use the capacitor connection. Do not apply a specific voltage to this pin.
Note 2. This voltage must be no higher than 6.5 V.
Note 3. The voltage on a pin in use for A/D conversion must not exceed VREFH0 + 0.3.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Note: VREFH0 refers to the positive reference voltage of the A/D converter.

Note: The reference voltage is VSS.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Table 2.2 Recommended operating conditions

Parameter	Symbol		Min	Typ	Max	Unit
Power supply voltages	VCC		1.6	—	5.5	V
	VSS		—	0	—	V
Analog power supply voltages	VREFH0	When used as ADC12 Reference	1.6	—	VCC	V
	VREFL0		—	0	—	V

2.1.1 Tj/Ta Definition

Table 2.3 Tj/Ta definition

Conditions: Products with operating temperature Ta = -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	—	125[*1]	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode

Note 1. The upper limit of operating temperature is 105°C.

Note: Make sure that $Tj = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

2.2 Oscillators Characteristics

2.2.1 Main clock Oscillator Characteristics

Table 2.4 Main clock oscillator characteristics

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Min	Typ	Max	Unit	Test conditions
Main clock oscillation allowable input cycle time[*1]	Ceramic resonator Crystal resonator	0.05	—	1	μs	—

Note 1. The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

Note: Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.

2.2.2 Sub-clock Oscillator Characteristics

Table 2.5 Sub-clock oscillator characteristics

Conditions: VCC = 2.4 to 5.5 V (16- to 24-pin products), VCC = 1.6 to 5.5 V (32-pin products), VSS = 0 V, Ta = -40 to +105°C

Parameter		Min	Typ	Max	Unit	Test conditions
Sub-clock oscillation frequency (f_{SOSC})[*1]	Crystal resonator	—	32.768	—	kHz	—

Note 1. The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

2.2.3 On-chip Oscillators Characteristics

Table 2.6 On-chip oscillators characteristics (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
High-speed on-chip oscillator clock frequency		f_{HOCO}	1	—	32	MHz	—
High-speed on-chip oscillator clock frequency accuracy	OSCSF.HOCOSF = 1	—	-1.0	—	+1.0	%	Ta = -40 to +105°C, 1.6 V ≤ VCC ≤ 5.5 V
	OSCSF.HOCOSF = 0[*3]	—	-15	—	0	%	—
High-speed on-chip oscillator clock correction resolution		—	—	0.05	—	%	—
Middle-speed on-chip oscillator clock frequency[*1]		f_{MOCO}	1	—	4	MHz	—
Middle-speed on-chip oscillator clock frequency accuracy		—	-12	—	12	%	—
Middle-speed on-chip oscillator clock correction resolution		—	—	0.15	—	%	—
Middle-speed on-chip oscillator frequency temperature coefficient		—	—	—	±0.17[*2]	%/°C	—
Low-speed on-chip oscillator clock frequency[*1]		f_{LOCO}	—	32.768	—	kHz	—
Low-speed on-chip oscillator clock frequency accuracy		—	-15	—	15	%	—
Low-speed on-chip oscillator clock correction resolution		—	—	0.3	—	%	—

Table 2.6 On-chip oscillators characteristics (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Low-speed on-chip oscillator frequency temperature coefficient	—	—	—	±0.21[*2]	%/°C	—

Note 1. The listed values only indicate the characteristics of the oscillators. Refer to AC Characteristics for instruction execution time.
Note 2. Guaranteed by characterization results.
Note 3. The listed condition applies when OFS1.HOCOFRQ1[2:0] = 010b.

2.3 DC Characteristics

2.3.1 Pin Characteristics

Table 2.7 I/O I_{OH}

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Allowable high-level output current[*1]	Per pin for P100 to P103, P108 to P110, P112, P201, P206 to P208, P300, P407	I_{OH}1	—	—	-10[*2]	mA	1.6 V ≤ VCC ≤ 5.5 V
	Total of all pins (when duty ≤ 70%[*3])		—	—	-80[*4]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-19	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-10	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-5	mA	1.6 V ≤ VCC < 1.8 V
	Per pin for P008 to P015, P212, P213	I_{OH}2	—	—	-3[*2]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-1[*2]	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-1[*2]	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-0.5[*2]	mA	1.6 V ≤ VCC < 1.8 V
	Total of all pins (when duty ≤ 70%[*3])		—	—	-20	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-10	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-5	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-5	mA	1.6 V ≤ VCC < 1.8 V

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the VCC pin to an output pin.
Note 2. The combination of these and other pins must also not exceed the value for maximum total current.
Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = (I_{OH} × 0.7)/(n × 0.01)
  Example when n = 80% and I_{OH} = -10.0 mA
  Total output current from the listed pins = (-10.0 × 0.7)/(80 × 0.01) = -8.75 mA
  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is -50 mA with an ambient operating temperature range of 85°C to 105°C.

Note: The following pins are not capable of the output of high-level signals in the N-ch open-drain mode.

P100 to P103, P109, P110, P112, P201, P207, P208, P212, P213 and P407.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.8 I/O I_{OL}

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Allowable low-level output current[*1]	Per pin for P100 to P103, P108 to P110, P112, P201, P206 to P208, P300, P407	$I_{OL}1$	—	—	20[*2]	mA	—
	Per pin for P913, P914		—	—	15[*2]	mA	—
	Total of all pins (when duty ≤ 70%[*3])		—	—	80[*4]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	35	mA	2.7 V ≤ VCC < 4.0 V
			—	—	20	mA	1.8 V ≤ VCC < 2.7 V
			—	—	10	mA	1.6 V ≤ VCC < 1.8 V
	Per pin for P008 to P015, P212, P213	$I_{OL}2$	—	—	8.5[*2]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	1.5[*2]	mA	2.7 V ≤ VCC < 4.0 V
			—	—	0.6[*2]	mA	1.8 V ≤ VCC < 2.7 V
			—	—	0.4[*2]	mA	1.6 V ≤ VCC < 1.8 V
	Total of all pins (when duty ≤ 70%[*3])		—	—	20	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	20	mA	2.7 V ≤ VCC < 4.0 V
			—	—	15	mA	1.8 V ≤ VCC < 2.7 V
			—	—	10	mA	1.6 V ≤ VCC < 1.8 V

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to VSS pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = (I_{OL} × 0.7)/(n × 0.01)
  Example when n = 80% and I_{OL} = 10.0 mA
  Total output current from the listed pins = (10.0 × 0.7)/(80 × 0.01) = 8.75 mA
  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin.
  A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is 40 mA with an ambient operating temperature range of 85°C to 105°C.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.9 I/O V_{IH}, V_{IL} (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage, high	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407	Normal input buffer	$V_{IH}1$	VCC × 0.8	—	VCC	V	—
	P100 to P103, P108 to P110, P112, P201, P207, P208, P300, P407	TTL input buffer	$V_{IH}2$	2.2	—	VCC	V	4.0 V ≤ VCC ≤ 5.5 V
				2.0	—	VCC	V	3.3 V ≤ VCC < 4.0 V
				1.5	—	VCC	V	1.6 V ≤ VCC < 3.3 V
	P008 to P015		$V_{IH}3$	VCC × 0.7	—	VCC	V	—
	P913, P914		$V_{IH}4$	VCC × 0.7	—	6.0	V	—
	P212 to P215		$V_{IH}5$	VCC × 0.8	—	VCC	V	—

Table 2.9 I/O V_{IH}, V_{IL} (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage, low	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407	Normal input buffer	$V_{IL}1$	0	—	VCC × 0.2	V	—
	P100 to P103, P108 to P110, P112, P201, P207, P208, P300, P407	TTL input buffer	$V_{IL}2$	0	—	0.8	V	4.0 V ≤ VCC ≤ 5.5 V
				0	—	0.5	V	3.3 V ≤ VCC < 4.0 V
				0	—	0.32	V	1.6 V ≤ VCC < 3.3 V
	P008 to P015		$V_{IL}3$	0	—	VCC × 0.3	V	—
	P913, P914		$V_{IL}4$	0	—	VCC × 0.3	V	—
	P212 to P215		$V_{IL}5$	0	—	VCC × 0.2	V	—

Note: The maximum value of V_{IH} of pins P100 to P103, P109, P110, P112, P201, P207, P208, P212, P213 and P407 is VCC, even in the N-ch open-drain mode.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.10 I/O V_{OH}, V_{OL} (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage, high	P100 to P103, P108 to P110, P112, P201, P206 to P208, P300, P407	$V_{OH}1$	VCC - 1.5	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -10 mA
			VCC - 0.7	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -3 mA
			VCC - 0.6	—	—	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -2 mA
			VCC - 0.5	—	—	V	1.8 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -1.5 mA
			VCC - 0.5	—	—	V	1.6 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -1 mA
	P008 to P015, P212, P213	$V_{OH}2$	VCC - 0.7	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}2$ = -3 mA
			VCC - 0.5	—	—	V	2.7 V ≤ VCC < 4.0 V $I_{OH}2$ = -1 mA
			VCC - 0.5	—	—	V	1.8 V ≤ VCC < 2.7 V $I_{OH}2$ = -1 mA
			VCC - 0.5	—	—	V	1.6 V ≤ VCC < 1.8 V $I_{OH}2$ = -0.5 mA

Table 2.10 I/O V_{OH}, V_{OL} (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage, low	P100 to P103, P108 to P110, P112, P201, P206 to P208, P300, P407	$V_{OL}1$	—	—	1.3	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 20 mA
			—	—	0.7	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 8.5 mA
			—	—	0.6	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 3 mA
			—	—	0.4	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 1.5 mA
			—	—	0.4	V	1.8 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 0.6 mA
			—	—	0.4	V	1.6 V ≤ VCC ≤ 5.5 V $I_{OL}1$ = 0.3 mA
	P008 to P015, P212, P213	$V_{OL}2$	—	—	0.7	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}2$ = 8.5 mA
			—	—	0.5	V	2.7 V ≤ VCC < 4.0 V $I_{OL}2$ = 1.5 mA
			—	—	0.4	V	1.8 V ≤ VCC < 2.7 V $I_{OL}2$ = 0.6 mA
			—	—	0.4	V	1.6 V ≤ VCC < 1.8 V $I_{OL}2$ = 0.4 mA
	P913, P914	$V_{OL}3$	—	—	2.0	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}3$ = 15 mA
			—	—	0.4	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OL}3$ = 5 mA
			—	—	0.4	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OL}3$ = 3 mA
			—	—	0.4	V	1.8 V ≤ VCC ≤ 5.5 V $I_{OL}3$ = 2 mA
			—	—	0.4	V	1.6 V ≤ VCC ≤ 5.5 V $I_{OL}3$ = 1 mA

Note: P100 to P103, P109, P110, P112, P201, P207, P208, P212, P213 and P407 do not output high-level signals in the N-ch open-drain mode.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.11 I/O other characteristics (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current, high	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407, P913, P914	$I_{LIH}1$	—	—	1	μA	V_I = VCC
	P008 to P015	$I_{LIH}2$	—	—	1	μA	V_I = VCC
	P212 to P214	$I_{LIH}3$	—	—	1	μA	V_I = VCC

Table 2.11 I/O other characteristics (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current, low	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407, P913, P914	$I_{LIL}1$	—	—	-1	μA	V_I = VSS
	P008 to P015	$I_{LIL}2$	—	—	-1	μA	V_I = VSS
	P212 to P214	$I_{LIL}3$	—	—	-1	μA	V_I = VSS
On-chip pll-up resistance	P100 to P103, P108 to P110, P112, P201, P206 to P208, P212, P213, P300, P407	R_U	10	20	100	kΩ	V_I = VSS In input port
Input capacitance	P200	Cin	—	—	30	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
	Other input pins		—	—	15		

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.3.2 Operating and Standby Current

Table 2.12 Operating and standby current (1) (1 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ*5	Max	Unit	Test Conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 32 MHz	Icc	2.7	—	mA	—
			All peripheral clocks enabled, CoreMark code executing from flash*6	ICLK = 32 MHz		—	5.0		—
		Sleep mode	All peripheral clocks disabled	ICLK = 32 MHz		0.82	—		—
			All peripheral clocks enabled*6	ICLK = 32 MHz		—	2.7		—
	Middle-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 24 MHz		2.1	—		—
				ICLK = 16 MHz		1.5	—		—
				ICLK = 8 MHz		1.0	—		—
				ICLK = 4 MHz		0.70	—		—
			All peripheral clocks enabled, CoreMark code executing from flash*6	ICLK = 24 MHz		—	3.8		—
				ICLK = 16 MHz		—	2.7		—
				ICLK = 8 MHz		—	1.6		—
				ICLK = 4 MHz		—	1.1		—
		Sleep mode	All peripheral clocks disabled	ICLK = 24 MHz		0.67	—		—
				ICLK = 16 MHz		0.61	—		—
				ICLK = 8 MHz		0.50	—		—
				ICLK = 4 MHz		0.44	—		—
			All peripheral clocks enabled*6	ICLK = 24 MHz		—	2.1		—
				ICLK = 16 MHz		—	1.6		—
				ICLK = 8 MHz		—	1.1		—
				ICLK = 4 MHz		—	0.8		—
	Low-speed mode*3	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 2 MHz		180	—	µA	—
			All peripheral clocks enabled, CoreMark code executing from flash*6	ICLK = 2 MHz		—	323		—
		Sleep mode	All peripheral clocks disabled	ICLK = 2 MHz		47	—		—
			All peripheral clocks enabled*6	ICLK = 2 MHz		—	161		—

Table 2.12 Operating and standby current (1) (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter						Symbol	Typ[*5]	Max	Unit	Test Conditions
Supply current[*1]	Subosc-speed mode[*4]	Normal mode	Peripheral clocks disabled	ICLK = 32.768 kHz	Ta = -40°C	Icc	3.3	—	μA	—
					Ta = 25°C		3.7	—		
					Ta = 50°C		3.9	—		
					Ta = 70°C		4.3	—		
					Ta = 85°C		4.8	—		
					Ta = 105°C		6.2	—		
			Peripheral clocks enabled[*6]	ICLK = 32.768 kHz	Ta = -40°C		—	7.2		
					Ta = 25°C		—	7.9		
					Ta = 50°C		—	9.6		
					Ta = 70°C		—	13.0		
					Ta = 85°C		—	18.8		
					Ta = 105°C		—	36.5		
		Sleep mode	Peripheral clocks disabled	ICLK = 32.768 kHz	Ta = -40°C		1.0	—		—
					Ta = 25°C		1.3	—		
					Ta = 50°C		1.5	—		
					Ta = 70°C		1.8	—		
					Ta = 85°C		2.2	—		
					Ta = 105°C		3.2	—		
			Peripheral clocks enabled[*6]	ICLK = 32.768 kHz	Ta = -40°C		—	4.8		
					Ta = 25°C		—	5.4		
					Ta = 50°C		—	7.0		
					Ta = 70°C		—	10.5		
					Ta = 85°C		—	16.1		
					Ta = 105°C		—	33.3		

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The clock source is high-speed on-chip oscillator (HOCO).
Note 3. The clock source is middle-speed on-chip oscillator (MOCO).
Note 4. The clock source is the Sub-clock oscillator (SOSC) and CMC.SODRV[1:0] are 10b (Low power mode 2).
Note 5. VCC = 3.3 V.
Note 6. Includes operating current for PCLBUZ, TAU, SAU, and IICA functions only. For other peripheral operating currents, please add the current in Peripheral Functions Supply current in Table 2.14.

Table 2.13 Operating and standby current (2)

Conditions: VCC = 1.6 to 5.5 V

Parameter						Symbol	Typ[3]	Max	Unit	Test conditions
Supply current [1]	Software Standby mode[2]	Peripheral modules stop	PSMCR.RAMSD[1:0] are 00b	All SRAMs (0x2000_4000 to 0x2000_6FFF) are on	Ta = -40°C	Icc	0.20	1.1	μA	—
					Ta = 25°C		0.20	1.1		
					Ta = 50°C		0.30	2.4		
					Ta = 70°C		0.50	5.5		
					Ta = 85°C		0.80	11		
					Ta = 105°C		1.8	28		
			PSMCR.RAMSD[1:0] are 11b	Only 4KB SRAM (0x2000_4000 to 0x2000_4FFF) is on	Ta = -40°C		0.20	1.1		—
					Ta = 25°C		0.20	1.1		
					Ta = 50°C		0.30	2.4		
					Ta = 70°C		0.50	5.0		
					Ta = 85°C		0.70	10		
					Ta = 105°C		1.7	25		

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.

Note 2. The IWDT and LVD are not operating.

Note 3. VCC = 3.3 V.

Table 2.14 Peripheral Functions Supply current

Conditions: VCC = 1.6 to 5.5 V

Parameter				Symbol	Typ*12	Max	Unit	Test conditions
Peripheral Functions Supply current*1	High-speed on chip oscillator operating current*1		OFS1.HOCOFRQ1[2:0] are 010b	I_{HOCO}	320	—	μA	—
	Middle-speed on chip oscillator operating current*1			I_{MOCO}	20	—	μA	—
	Low-speed on chip oscillator operating current*1			I_{LOCO}	0.24	—	μA	—
	Main-clock oscillator	AMPH=0	f_{MOSC} = 10MHz	I_{MOSC}	160	—	μA	—
		AMPH=1	f_{MOSC} = 20MHz		330	—	μA	—
	Sub-clock oscillator	SBYCR.RTCLPC is 1	CMC.SODRV[1:0] are 11b (Low power mode 3)	I_{SOSC}	0.13	—	μA	—
			CMC.SODRV[1:0] are 10b (Low power mode 2)		0.34	—	μA	—
			CMC.SODRV[1:0] are 00b (Low power mode 1)		0.49	—	μA	—
			CMC.SODRV[1:0] are 01b (Normal mode)		0.62	—	μA	—
		SBYCR.RTCLPC is 0	CMC.SODRV[1:0] are 11b (Low power mode 3)		0.30	—	μA	
			CMC.SODRV[1:0] are 10b (Low power mode 2)		0.51	—	μA	
			CMC.SODRV[1:0] are 00b (Low power mode 1)		0.65	—	μA	
			CMC.SODRV[1:0] are 01b (Normal mode)		0.80	—	μA	
	RTC*1*2*3	RTCC0.RTC128EN is 0		I_{RTC}	0.006	—	μA	—
		RTCC0.RTC128EN is 1			0.001	—	μA	—
	32-bit interval timer operating current*1*2*4			I_{IT}	0.06	—	μA	—
	Independent watchdog timer operating current*1*2*5		f_{LOCO} = 32.768 kHz (typ.)	I_{IWDT}	0.03	—	μA	—
	A/D converter operating current*1*6	When conversion at maximum speed	Normal mode, VREFH0 = VCC = 5.0 V	I_{ADC}	0.81	1.6	mA	—
			Low voltage mode, VREFH0 = VCC = 3.0 V		0.46	0.75	mA	—
	VREFH0 current*7		VREFH0 = 5.0 V	I_{ADREF}	62	—	μA	—
	A/D converter internal reference voltage current*1			I_{ADREF}	82	—	μA	—
	Temperature sensor operating current*1			I_{TMPS}	100	—	μA	—
	LVD operating current*1		LVD0 is enabled*8	I_{LVD0}	0.03	—	μA	—
			LVD1 is enabled*9	I_{LVD1}	0.03	—	μA	—
	Self-programming operating current*1*10			I_{FSP}	—	12.2	mA	—
	Data flash rewrite operating current*1*11			I_{BGO}	—	12.2	mA	—
	Operating current of the true random number generator*1			I_{TRNG}	1.1	—	mA	—
	DTC		Data transfer to RAM	I_{DTC}	1.82	—	mA	—

Note 1. This current flows into V_{CC}.

Note 2. The listed currents apply when the high-speed on-chip oscillator (HOCO), middle-speed on-chip oscillator (MOCO), and Main clock oscillator (MOSC) are stopped.

Note 3. This current flows into the realtime clock (RTC). It does not include the operating current of the low-speed on-chip oscillator (LOCO) or the Sub-clock oscillator (SOSC).
The supply current of the RA0 microcontrollers is the sum of either Icc, and I_{RTC}.

When the low-speed on-chip oscillator (LOCO) is selected, I_{LOCO} should be included in the supply current.
When the Sub-clock oscillator (SOSC) is selected, I_{SOSC} should be included in the supply current.

Note 4. This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator (LOCO) or Sub-clock oscillator (SOSC).
The supply current of the RA0 microcontrollers is the sum of either Icc and I_{IT}.
When the low-speed on-chip oscillator (LOCO) is selected, I_{LOCO} should be included in the supply current.
When the Sub-clock oscillator (SOSC) is selected, I_{SOSC} should be included in the supply current.

Note 5. This current only flows to the independent watchdog timer. It does not include the operating current of the low-speed on-chip oscillator (LOCO) .
The supply current of the RA0 microcontrollers is the sum of either Icc, I_{IWDT} and I_{LOCO}.

Note 6. This current only flows to the A/D converter. The supply current of the RA0 microcontrollers is the sum of Icc and I_{ADC} when the A/D converter is operating or in the SLEEP mode.

Note 7. This current flows into VREFH0.

Note 8. This current only flows to the LVD0 circuit. The supply current of the RA0 microcontrollers is the sum of Icc and I_{LVD0} when the LVD0 circuit is in operation.

Note 9. This current only flows to the LVD1 circuit. The supply current of the RA0 microcontrollers is the sum of Icc and I_{LVD1} when the LVD1 circuit is in operation.

Note 10. This current only flows during self programming.

Note 11. This current only flows while the data flash memory is being rewritten.

Note 12. VCC = 3.3 V.

2.4 AC Characteristics

Table 2.15 AC characteristics (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Instruction cycle (minimum instruction execution time)	Main system clock (FMAIN) operation	High-speed mode	T_{CY}	0.03125	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
				0.25	—	1	μs	1.6 V ≤ VCC < 1.8 V
		Middle-speed mode		0.04167	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
				0.25	—	1	μs	1.6 V ≤ VCC < 1.8 V
		Low-speed mode		0.5	—	1	μs	1.6 V ≤ VCC ≤ 5.5 V
	Subsystem clock (FSUB) operation			26.041	30.5	31.3	μs	1.6 V ≤ VCC ≤ 5.5 V
	In the self-programming mode	High-speed mode		0.03125	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
		Middle-speed mode		0.04167	—	1	μs	1.8 V ≤ VCC ≤ 5.5 V
External system clock frequency			f_{EX}	1.0	—	20.0	MHz	1.8 V ≤ VCC ≤ 5.5 V
				1.0	—	4.0	MHz	1.6 V ≤ VCC < 1.8 V
External system clock input high-level width, low-level width			$t_{EXH}t_{EXL}$	24	—	—	ns	1.8 V ≤ VCC ≤ 5.5 V
				120	—	—	ns	1.6 V ≤ VCC < 1.8 V
TI00 to TI07 input high-level width, low-level width			t_{TIH} t_{TIL}	$1/f_{MCK}$ +10*1	—	—	ns	
TO00 to TO07 output frequency		High-speed mode Middle-speed mode	f_{TO}	—	—	16	MHz	4.0 V ≤ VCC ≤ 5.5 V
				—	—	8	MHz	2.7 V ≤ VCC < 4.0 V
				—	—	4	MHz	1.8 V ≤ VCC < 2.7 V
				—	—	2	MHz	1.6 V ≤ VCC < 1.8 V
		Low-speed mode		—	—	2	MHz	1.6 V ≤ VCC ≤ 5.5 V

Table 2.15 AC characteristics (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
PCLBUZ0 output frequency	High-speed mode Middle-speed mode	f_{PCL}	—	—	16	MHz	4.0 V ≤ VCC ≤ 5.5 V
			—	—	8	MHz	2.7 V ≤ VCC < 4.0 V
			—	—	4	MHz	1.8 V ≤ VCC < 2.7 V
			—	—	2	MHz	1.6 V ≤ VCC < 1.8 V
	Low-speed mode		—	—	2	MHz	1.6 V ≤ VCC ≤ 5.5 V
Interrupt input high-level width, low-level width	NMI/IRQ0, IRQ1 to IRQ5	f_{IRQH} f_{IRQL}	1	—	—	μs	1.6 V ≤ VCC ≤ 5.5 V
RES low-level width		t_{RSL}	10	—	—	μs	—

Note 1. f_{MCK}: Timer array unit operating clock frequency
To set this operating clock, use the CKS[1:0] bits of the timer mode register 0n (TMR0n).
m: Unit number (m = 0), n: Channel number (n = 0 to 7)

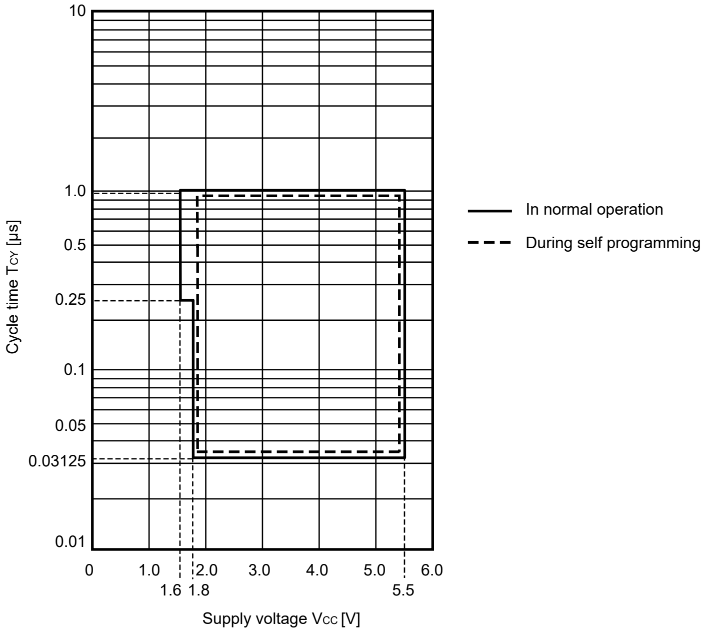


Figure 2.2 T_{CY} vs V_{CC} in High-speed mode

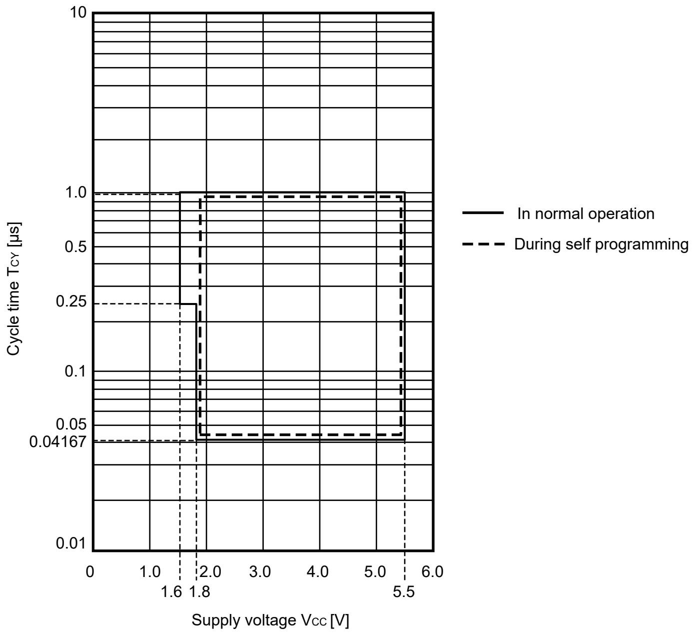


Figure 2.3 T_{CY} vs V_{CC} in Middle-speed mode

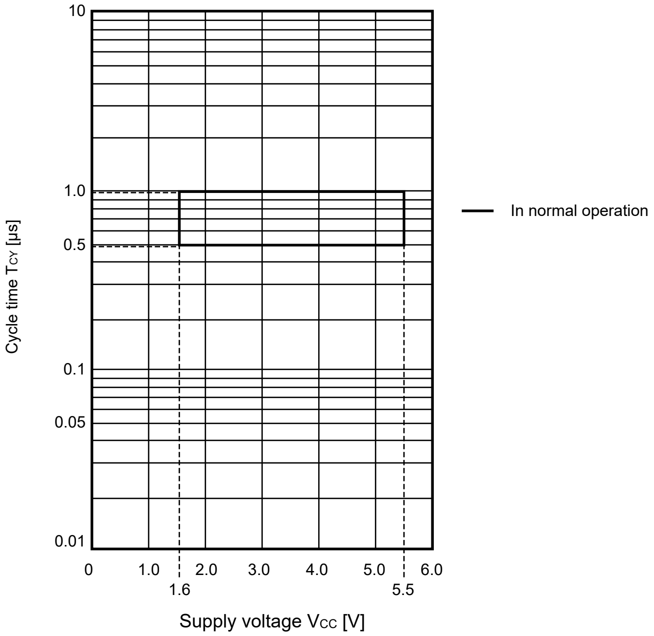


Figure 2.4 T_{CY} vs V_{CC} in Low-speed mode

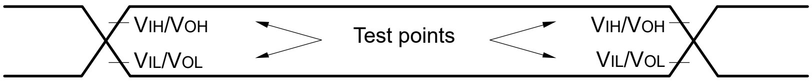


Figure 2.5 AC timing test points

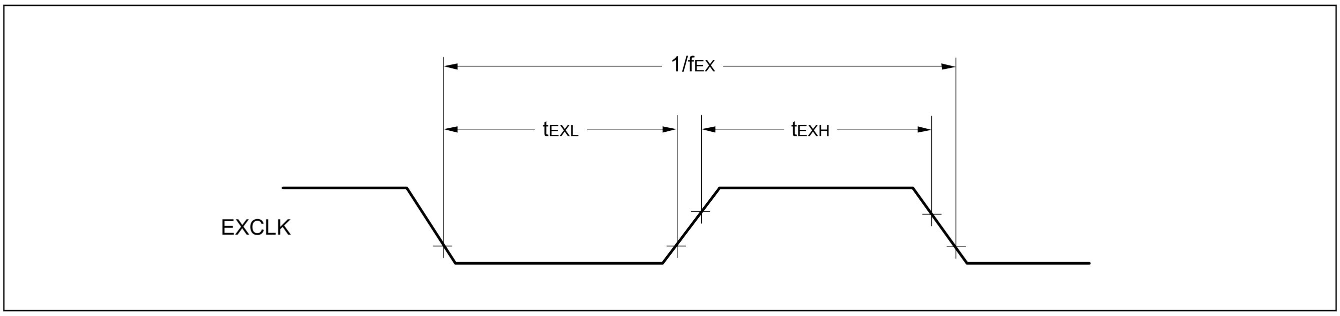


Figure 2.6 External system clock timing

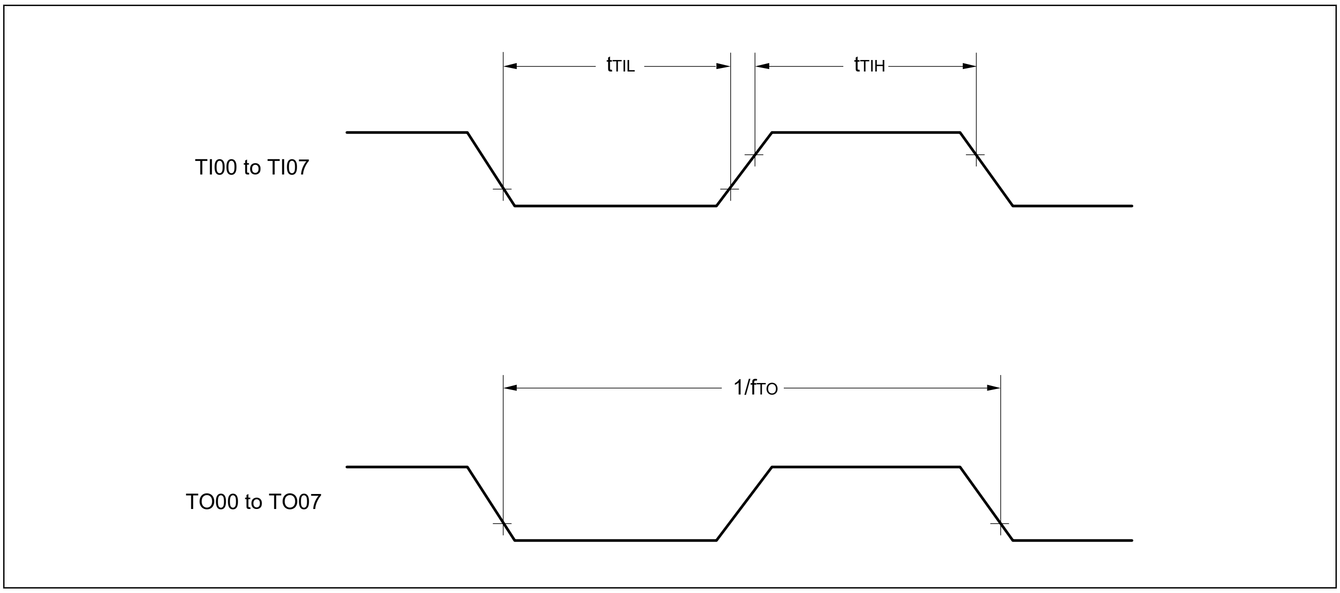


Figure 2.7 TI/TO timing

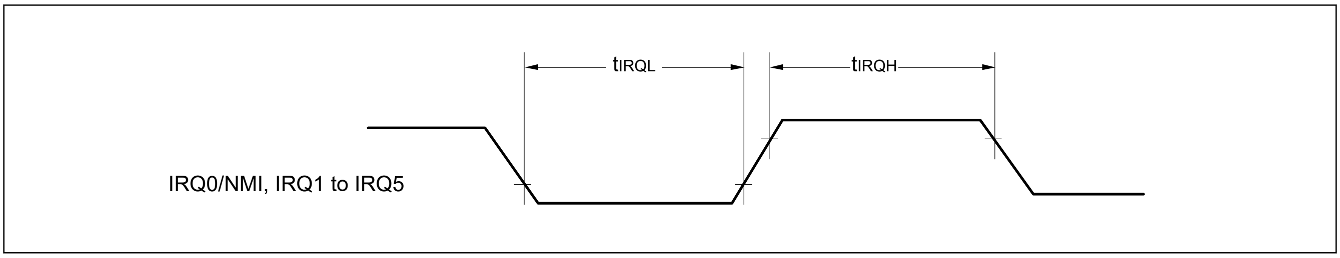


Figure 2.8 IRQ interrupt input timing

2.4.1 Reset Timing

Table 2.16 Reset timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on[*3]	t_{RESWP}	9.9	—	—	ms	—
	Not at power-on	t_{RESW}	10	—	—	μs	—
Wait time after RES cancellation (at power-on)	LVD0 enabled[*1]	t_{RESWT}	—	0.506	0.694	ms	—
	LVD0 disabled[*2]		—	0.201	0.335	ms	—
Wait time after RES cancellation (during powered-on state)	LVD0 enabled[*1]	t_{RESWT2}	—	0.476	0.616	ms	—
	LVD0 disabled[*2]		—	0.170	0.257	ms	—

Table 2.16 Reset timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after internal reset cancellation (Independent watchdog timer reset, SRAM parity error reset, software reset)	t_{RESWT3}	—	0.04	0.041	ms	—

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. When RES pin is not used as the external reset input, this specification can be ignore.

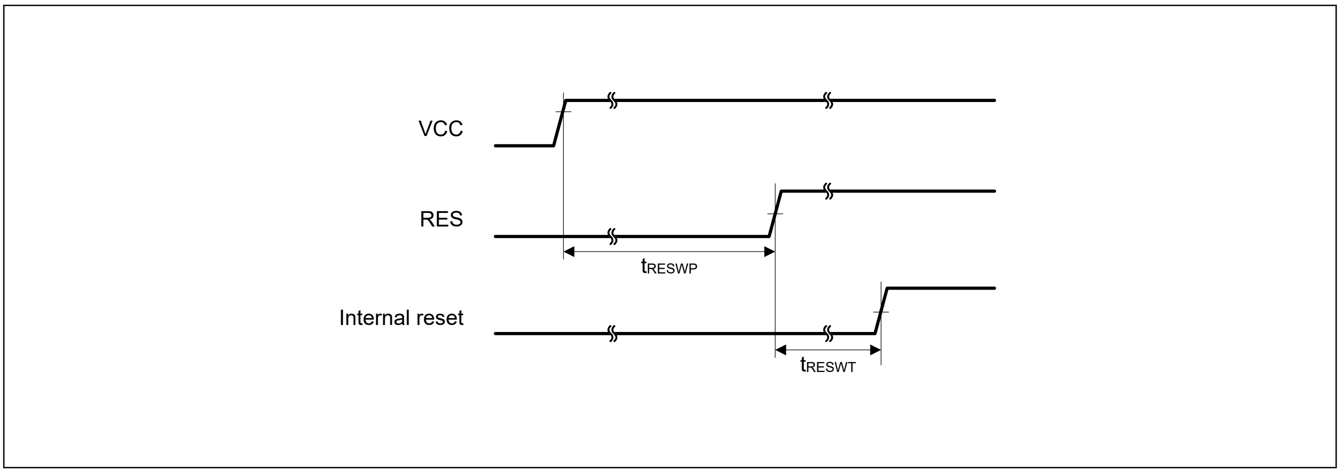


Figure 2.9 Reset input timing at power-on

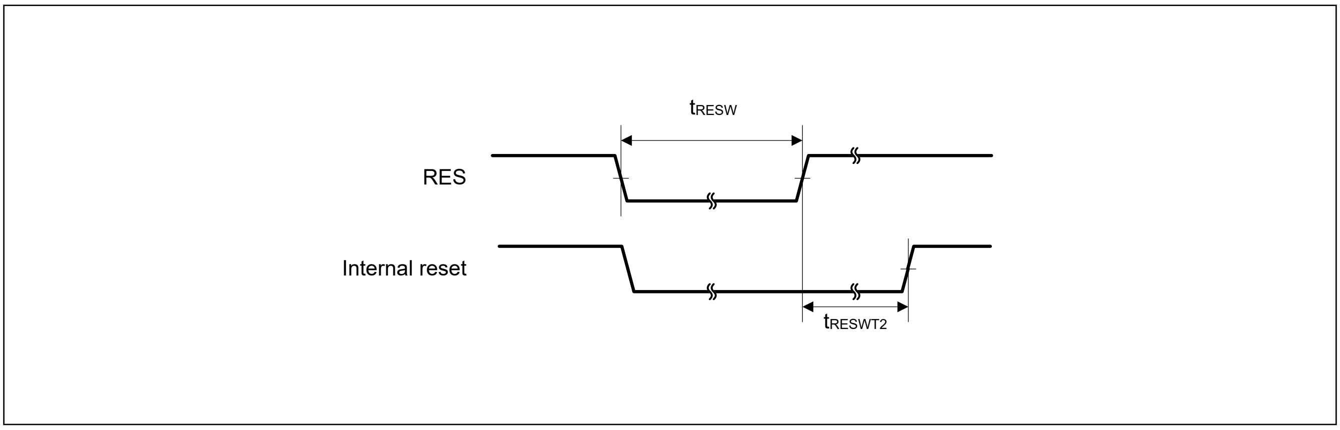


Figure 2.10 Reset input timing (1)

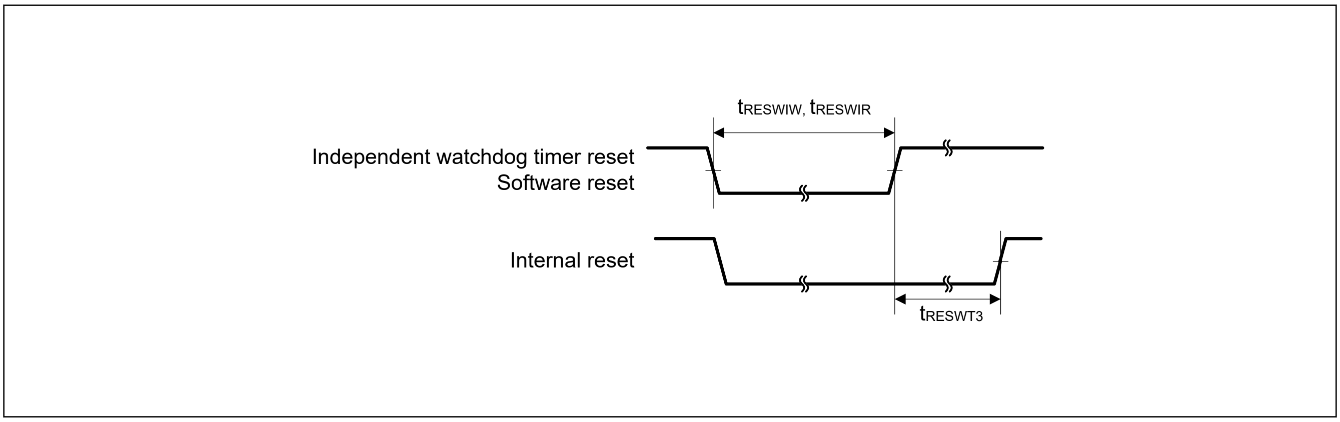


Figure 2.11 Reset input timing (2)

2.4.2 Wakeup Time

Table 2.17 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode[*1]	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)[*2] VCC = 1.8 V to 5.5 V	t_{SBYMC}	—	1.64	—	ms	Figure 2.12
			System clock source is main clock oscillator (4 MHz)[*2] VCC = 1.6 V to 1.8 V		—	8.19	—	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz) VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.8	2.8	μs	
			System clock source is main clock oscillator (4 MHz) VCC = 1.6 V to 1.8 V		—	13.8	14.0	μs	
		System clock source is HOCO	System clock source is HOCO (32 MHz) VCC = 1.8 V to 5.5 V SBYCR.FWKUP = 0	t_{SBYHO}	—	4.2	4.6	μs	
			System clock source is HOCO (32 MHz) VCC = 1.8 V to 5.5 V SBYCR.FWKUP = 1		—	0.9	1.1	μs	
			System clock source is HOCO (4 MHz) VCC = 1.6 V to 1.8 V		—	5.2	5.6	μs	
		System clock source is MOCO (4 MHz)		t_{SBYMO}	—	3.3	4.2	μs	

Note 1. The division ratio of ICLK is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Oscillation Stabilization Time Select Register (OSTS) is set to 0x05.

Table 2.18 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode[*1]	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)[*2] VCC = 1.8 V to 5.5 V	t_{SBYMC}	—	1.64	—	ms	Figure 2.12
			System clock source is main clock oscillator (4 MHz)[*2] VCC = 1.6 V to 1.8 V		—	8.19	—	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz) VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.8	2.8	µs	
			System clock source is main clock oscillator (4 MHz) VCC = 1.6 V to 1.8 V		—	13.8	14.0	µs	
		System clock source is HOCO	System clock source is HOCO (24 MHz) VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	5.1	5.5	µs	
			System clock source is HOCO (3 MHz) VCC = 1.6 V to 1.8 V		—	5.6	6.1	µs	
		System clock source is MOCO (4 MHz)		t_{SBYMO}	—	3.3	4.2	µs	

Note 1. The division ratio of ICLK is the minimum division ratio within the allowable frequency range.
The recovery time is determined by the system clock source.

Note 2. The Oscillation Stabilization Time Select Register (OSTS) is set to 0x05.

Table 2.19 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode[*1]	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)[*2]	t_{SBYMC}	—	4.1	—	ms	Figure 2.12
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)[*2]	t_{SBYEX}	—	27.5	28.0	µs	
		System clock source is MOCO (2 MHz)		t_{SBYMO}	—	6.0	7.5	µs	

Note 1. The division ratio of ICLK is the minimum division ratio within the allowable frequency range.
The recovery time is determined by the system clock source.

Note 2. The Oscillation Stabilization Time Select Register (OSTS) is set to 0x05.
Crystal resonator frequency is 8 MHz and the Main System Clock Division Register (MOSCDIV) is set to 0x02.

Table 2.20 Timing of recovery from low power modes (4)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode[*1]	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	SBYCR.RTCLPC = 0	t_{SBYSC}	—	0.29	0.31	ms	Figure 2.12
			SBYCR.RTCLPC = 1		—	0.32	0.34	ms	
		System clock source is LOCO (32.768 kHz)		t_{SBYLO}	—	0.29	0.36	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

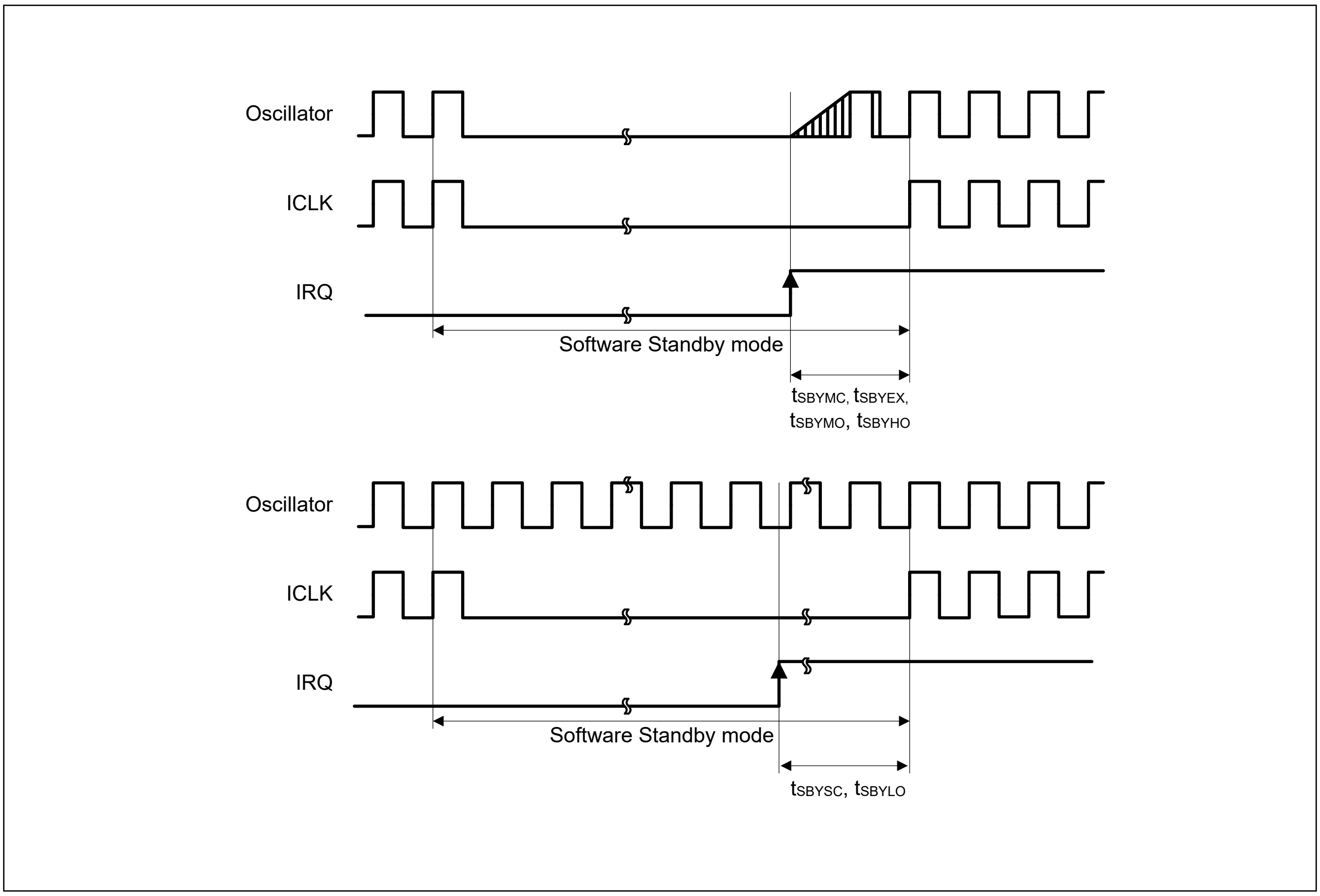
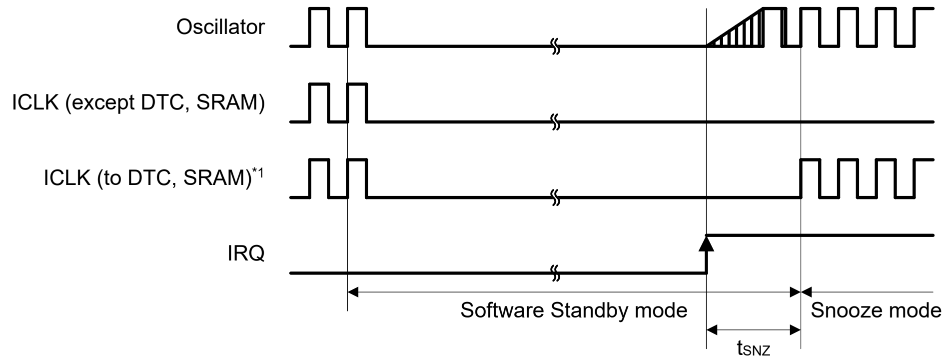


Figure 2.12 Software Standby mode cancellation timing

Table 2.21 Timing of recovery from low power modes (5)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	SBYCR.FWKUP = 0	t_{SNZ}	—	4.1	4.4	μs	Figure 2.13
		SBYCR.FWKUP = 1		—	0.9	1.0	μs	
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.8 V to 5.5 V		t_{SNZ}	—	4.2	4.4	μs	
	Middle-speed mode System clock source is HOCO (3 MHz) VCC = 1.6 V to 1.8 V		t_{SNZ}	—	4.8	5.3	μs	
	Low-speed mode System clock source is MOCO (2 MHz)		t_{SNZ}	—	4.0	5.4	μs	



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.13 Recovery timing from Software Standby mode to Snooze mode

2.5 Peripheral Function Characteristics

2.5.1 Serial Array Unit (SAU)

Table 2.22 In UART communications with devices operating at same voltage levels

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
Transfer rate[1]	1.6 V ≤ VCC ≤ 5.5 V		—	—	$f_{MCK}/6$	—	$f_{MCK}/6$	—	$f_{MCK}/6$	bps	Figure x.x
		Theoretical value of the maximum transfer rate f_{MCK} = ICLK[2]		—	5.3	—	4	—	0.33	Mbps	

Note 1. The transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

Note 2. The maximum operating frequencies of the system clock (ICLK) are as follows.
High-speed mode: 32 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Middle-speed mode: 24 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Low-speed mode: 2 MHz (1.6 V ≤ VCC ≤ 5.5 V)

Note: Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

gh: Port number (gh = 100, 101, 109, 110, 212, 213)

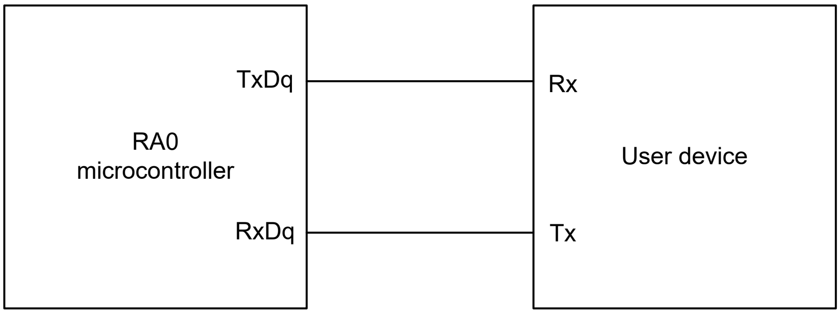


Figure 2.14 Connection in the UART communications with devices operating at same voltage levels

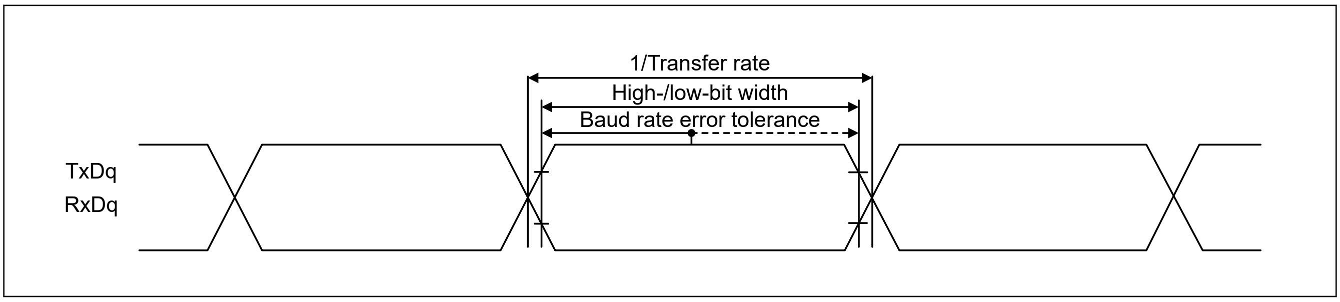


Figure 2.15 Bit width in the UART communications when interfacing devices operate at the same voltage level (reference)

Note:
- q: UART number (q = 0 to 2), gh: Port number (gh = 100, 101, 109, 110, 212, 213)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, set the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 01, 02, 03, 10, 11)

Table 2.23 In simplified SPI communications in the master mode with devices operating at same voltage levels with the internal SCKp clock (the ratings below are only applicable to SPI00)

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -40 to +85°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	t_{KCY1} ≥ 2/ICLK	4.0 V ≤ VCC ≤ 5.5 V	t_{KCY1}	62.5	—	83.3	—	1000	—	ns	Figure x.x
		2.7 V ≤ VCC ≤ 5.5 V		83.3	—	125	—	1000	—	ns	
SCKp high-/ low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH1}, t_{KL1}	t_{KCY1}/2 - 7	—	t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 15	—	t_{KCY1}/2 - 50	—	ns	
SIp setup time (to SCKp↑)[*1]	4.0 V ≤ VCC ≤ 5.5 V		t_{SIK1}	23	—	33	—	110	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			33	—	50	—	110	—	ns	
SIp hold time (from SCKp↑)[*1]	2.7 V ≤ VCC ≤ 5.5 V		t_{KSI1}	10	—	10	—	10	—	ns	
Delay time from SCKp↓ to SOp output[*2]	C = 20 pF[*3]		t_{KSO1}	—	10	—	10	—	10	ns	

Note 1. The setting applies when SCRmn.DCP0[1:0] = 00b or 11b. The setting for the SIp setup time becomes to SCKp↓ and that for the SIp hold time becomes from SCKp↓ when SCRmn.DCP0[1:0] = 01b or 10b.

Note 2. This setting applies when SCRmn.DCP0[1:0] = 00b or 11b. The setting for the delay time to SOp output becomes from SCKp↑ when SCRmn.DCP0[1:0] = 01b or 10b.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Note: Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Note:
- The listed times are only valid when the peripheral I/O redirect function of SPI00 is not in use.
- p: Simplified SPI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), gh: Port number (gh = 100 to 103, 112, 201)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00)

Table 2.24 In simplified SPI communications in the master mode with devices operating at same voltage levels with the internal SCKp clock

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	t_{KCY1} ≥ 4/ICLK	2.7 V ≤ VCC ≤ 5.5 V	t_{KCY1}	125	—	166	—	2000	—	ns	Figure x.x
		2.4 V ≤ VCC ≤ 5.5 V		250	—	250	—	2000	—	ns	
		1.8 V ≤ VCC ≤ 5.5 V		500	—	500	—	2000	—	ns	
		1.6 V ≤ VCC ≤ 5.5 V		1000	—	1000	—	2000	—	ns	
SCKp high-/ low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH1}, t_{KL1}	$t_{KCY1}/2 - 12$	—	$t_{KCY1}/2 - 21$	—	$t_{KCY1}/2 - 50$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			$t_{KCY1}/2 - 18$	—	$t_{KCY1}/2 - 25$	—	$t_{KCY1}/2 - 50$	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			$t_{KCY1}/2 - 38$	—	$t_{KCY1}/2 - 38$	—	$t_{KCY1}/2 - 50$	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$t_{KCY1}/2 - 50$	—	$t_{KCY1}/2 - 50$	—	$t_{KCY1}/2 - 50$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$t_{KCY1}/2 - 100$	—	$t_{KCY1}/2 - 100$	—	$t_{KCY1}/2 - 100$	—	ns	
SIp setup time (to SCKp↑)[*1]	4.0 V ≤ VCC ≤ 5.5 V		t_{SIK1}	44	—	54	—	110	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			44	—	54	—	110	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			75	—	75	—	110	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			110	—	110	—	110	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			220	—	220	—	220	—	ns	
SIp hold time (from SCKp↑)[*1]	1.6 V ≤ VCC ≤ 5.5 V		t_{KSI1}	19	—	19	—	19	—	ns	
Delay time from SCKp↓ to SOp output[*2]	1.6 V ≤ VCC ≤ 5.5 V C = 30 pF[*3]		t_{KSO1}	—	25	—	25	—	25	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the SIp setup time becomes to SCKp↓ and that for the SIp hold time becomes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.

Note 2. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the delay time to SOp output becomes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Note: Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Note:
- p: Simplified SPI number (p = 00, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 3), gh: Port number (gh= 100 to 103, 109, 110, 112, 201, 212, 213, 407)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03, 10)

Table 2.25 In simplified SPI communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Item	Conditions		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time[4]	4.0 V ≤ VCC ≤ 5.5 V	20 MHz < f_{MCK}	t_{KCY2}	$8/f_{MCK}$	—	$8/f_{MCK}$	—	—	—	ns	Figure x.x
		f_{MCK} ≤ 20 MHz		$6/f_{MCK}$	—	$6/f_{MCK}$	—	$6/f_{MCK}$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V	16 MHz < f_{MCK}		$8/f_{MCK}$	—	$8/f_{MCK}$	—	—	—	ns	
		f_{MCK} ≤ 16 MHz		$6/f_{MCK}$	—	$6/f_{MCK}$	—	$6/f_{MCK}$	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			$6/f_{MCK}$ and 500	—	$6/f_{MCK}$ and 500	—	$6/f_{MCK}$ and 500	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$6/f_{MCK}$ and 750	—	$6/f_{MCK}$ and 750	—	$6/f_{MCK}$ and 750	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$6/f_{MCK}$ and 1500	—	$6/f_{MCK}$ and 1500	—	$6/f_{MCK}$ and 1500	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH2}, t_{KL2}	$t_{KCY2}/2 - 7$	—	$t_{KCY2}/2 - 7$	—	$t_{KCY2}/2 - 7$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 8$	—	$t_{KCY2}/2 - 8$	—	$t_{KCY2}/2 - 8$	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 18$	—	$t_{KCY2}/2 - 18$	—	$t_{KCY2}/2 - 18$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 66$	—	$t_{KCY2}/2 - 66$	—	$t_{KCY2}/2 - 66$	—	ns	
SIp setup time (to SCKp↑)[1]	2.7 V ≤ VCC ≤ 5.5 V		t_{SIK2}	$1/f_{MCK} + 20$	—	$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 40$	—	$1/f_{MCK} + 40$	—	$1/f_{MCK} + 40$	—	ns	
SIp hold time (from SCKp↑)[1]	1.8 V ≤ VCC ≤ 5.5 V		t_{KSI2}	$1/f_{MCK} + 31$	—	$1/f_{MCK} + 31$	—	$1/f_{MCK} + 31$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 250$	—	$1/f_{MCK} + 250$	—	$1/f_{MCK} + 250$	—	ns	
Delay time from SCKp↓ to SOp output[2]	C = 30 pF[3]	2.7 V ≤ VCC ≤ 5.5 V	t_{KSO2}	—	$2/f_{MCK} + 44$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		2.4 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 75$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		1.8 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		1.6 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 220$	—	$2/f_{MCK} + 220$	—	$2/f_{MCK} + 220$	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the SIp setup time becomes to SCKp↓ and that for the SIp hold time becomes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.

Note 2. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the delay time to SOp output becomes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.

Note 3. C is the load capacitance of the SOp output line.

Note 4. Transfer rate in the SNOOZE mode is 1 Mbps at the maximum.

Note: Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Note:

- p: Simplified SPI number (p = 00, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 3), gh: Port number (gh = 100 to 103, 109, 110, 112, 201, 212, 213, 407)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03, 10)

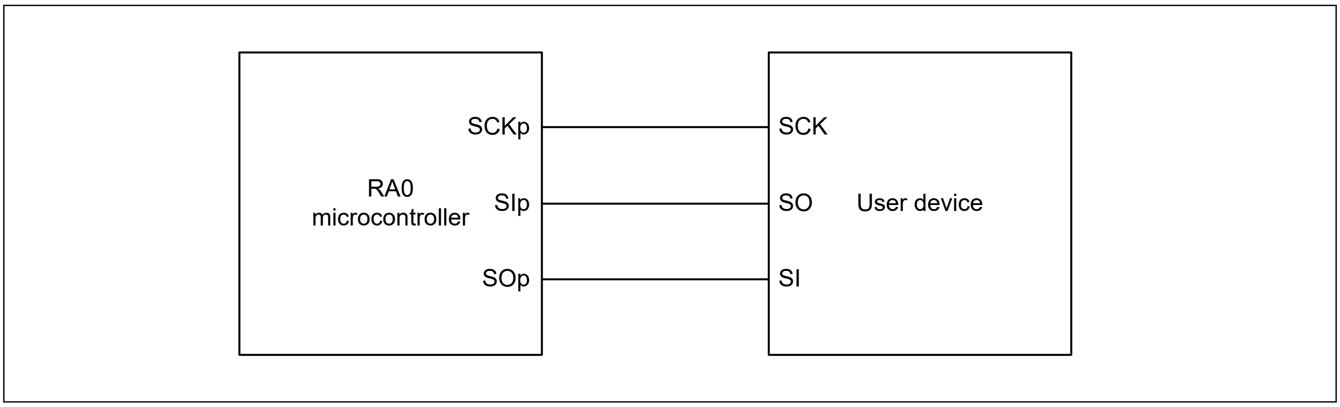


Figure 2.16 Connection in the simplified SPI communications with devices operating at same voltage levels

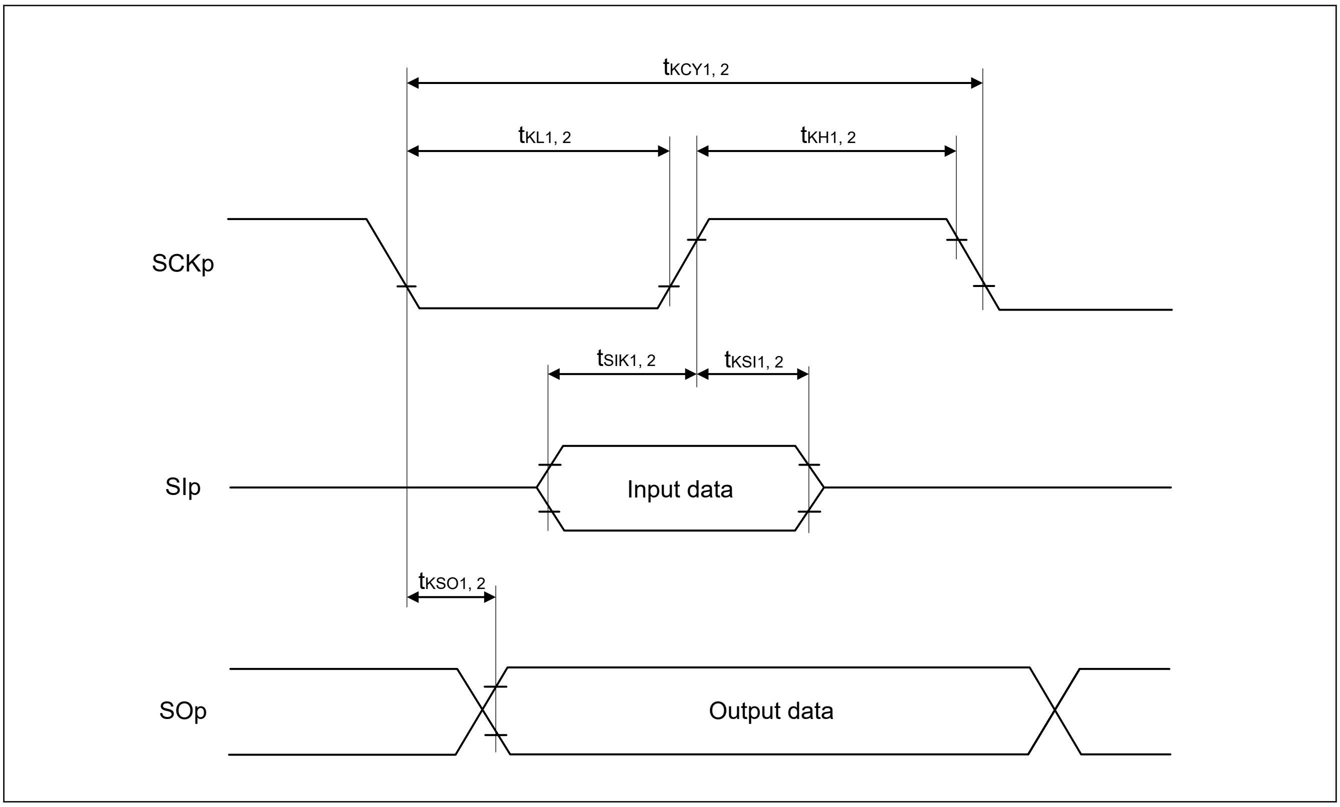


Figure 2.17 Timing of serial transfer in the simplified SPI communications with devices operating at same voltage levels when SCRmn.DCP[1:0] = 00b or 11b

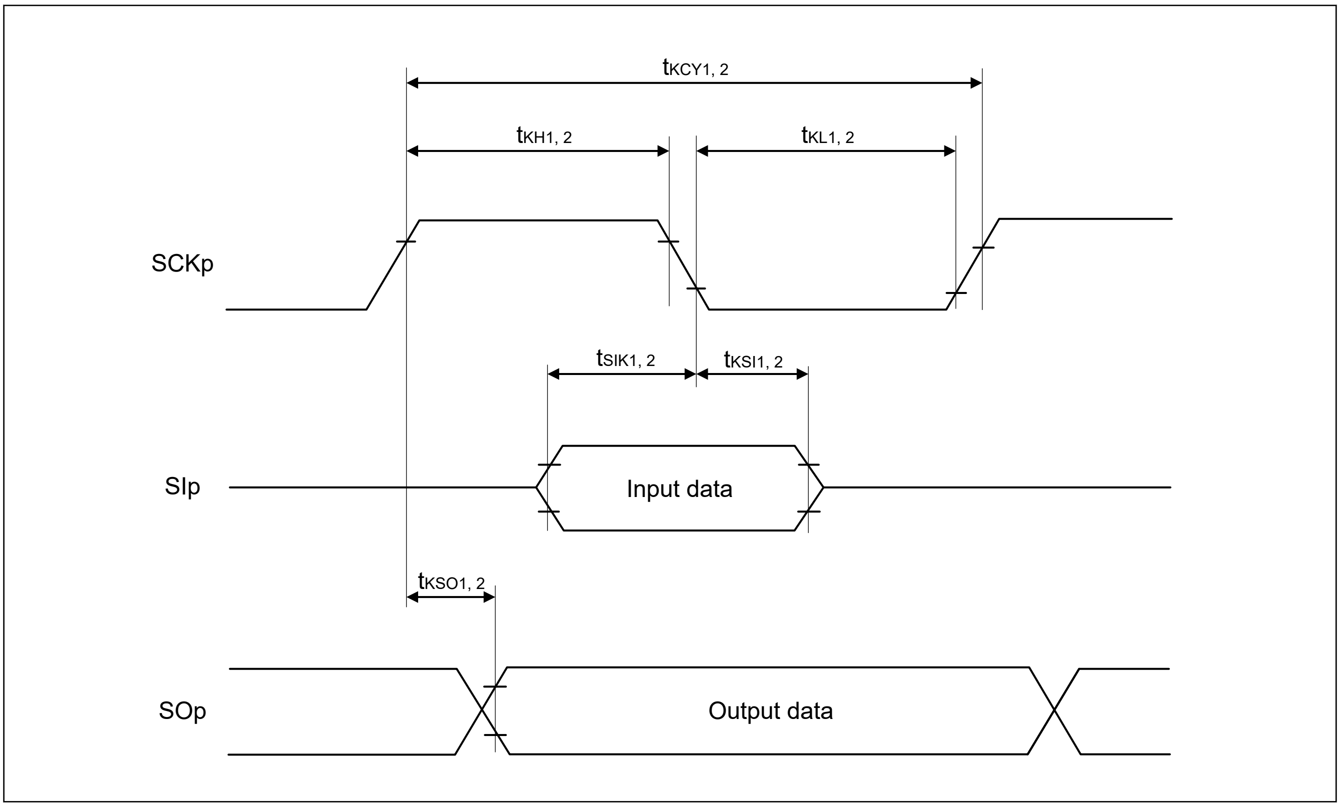


Figure 2.18 **Timing of serial transfer in the simplified SPI communications with devices operating at same voltage levels when SCRmn.DCP[1:0] = 01b or 10b**

Note:
- p: Simplified SPI number (p = 00, 11, 20)
- m: Unit number, n: Channel number (mn = 00, 03, 10)

Table 2.26 In simplified IIC communications with devices operating at same voltage levels (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SCLr clock frequency	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	f_{SCL}	—	1000[*1]	—	1000[*1]	—	400[*1]	kHz	Figure x.x
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		—	400[*1]	—	400[*1]	—	400[*1]	kHz	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		—	300[*1]	—	300[*1]	—	300[*1]	kHz	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—	250[*1]	—	250[*1]	—	250[*1]	kHz	
Hold time when SCLr is low	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{LOW}	475	—	475	—	1150	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		1150	—	1150	—	1150	—	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		1550	—	1550	—	1550	—	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		1850	—	1850	—	1850	—	ns	
Hold time when SCLr is high	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{HIGH}	475	—	475	—	1150	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		1150	—	1150	—	1150	—	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		1550	—	1550	—	1550	—	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		1850	—	1850	—	1850	—	ns	

Table 2.26 In simplified IIC communications with devices operating at same voltage levels (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
Data setup time (reception)	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{SU:DAT}$	1/f_{MCK} + 85^{*2}	—	1/f_{MCK} +85^{*2}	—	1/f_{MCK} +145^{*2}	—	ns	Figure x.x
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		1/f_{MCK} + 145^{*2}	—	1/f_{MCK} + 145^{*2}	—	1/f_{MCK} +145^{*2}	—	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		1/f_{MCK} + 230^{*2}	—	1/f_{MCK} + 230^{*2}	—	1/f_{MCK} + 230^{*2}	—	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		1/f_{MCK} + 290^{*2}	—	1/f_{MCK} + 290^{*2}	—	1/f_{MCK} + 290^{*2}	—	ns	
Data hold time (transmission)	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{HD:DAT}$	0	305	0	305	0	305	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		0	355	0	355	0	355	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		0	405	0	405	0	405	ns	
	1.6 V ≤ VCC < 1.8 V, C_b= 100 pF, R_b = 5 kΩ		0	405	0	405	0	405	ns	

Note 1. The listed times must be no greater than f_{MCK}/4.

Note 2. Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

Note: Select the normal input buffer and the N-ch open drain output [withstand voltage of VCC] mode for the SDAr pin and the normal output mode for the SCLr pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

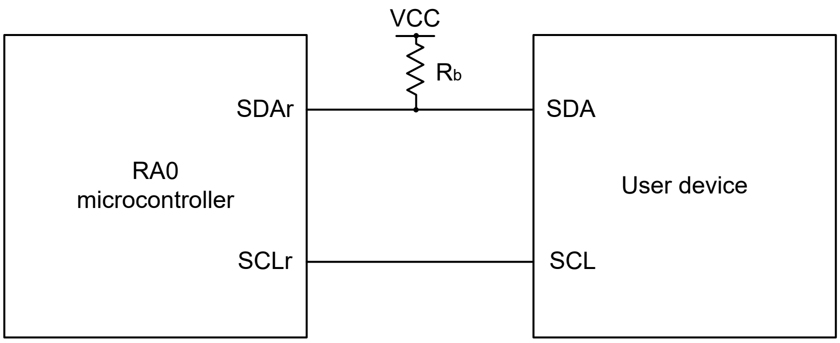


Figure 2.19 Connection in the simplified IIC communications with devices operating at same voltage levels

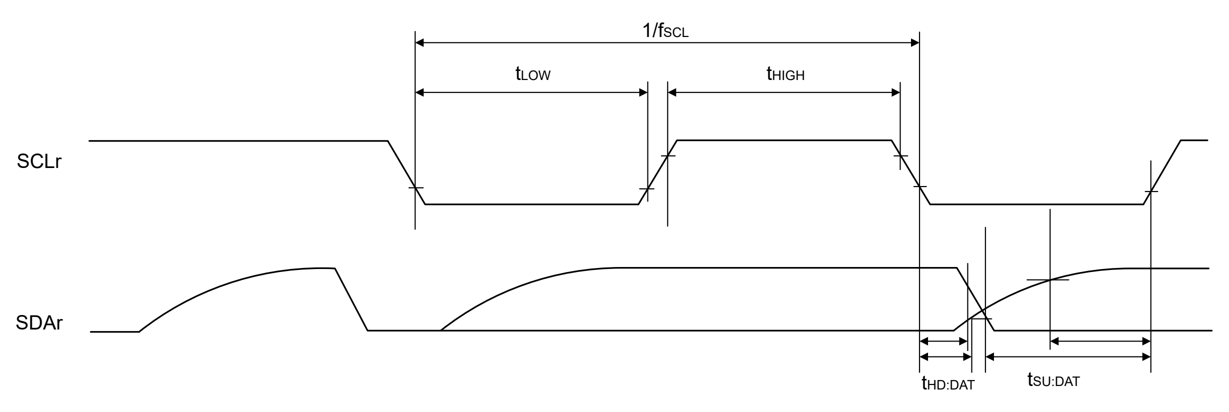


Figure 2.20 **Timing of serial transfer in the simplified IIC communications with devices operating at same voltage levels**

Note:
- $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance
- r: IIC number (r = 00, 11, 20), gh: Port number (gh = 100 to 102, 110, 112, 201, 212, 407)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03, 10)

Table 2.27 **In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V) (1)**

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter				**Symbol**	**High-speed mode**		**Middle-speed mode**		**Low-speed mode**		**Unit**	**Test Conditions**
					Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**		
Transfer rate	Reception	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		—	—	f_{MCK}/6*1	—	f_{MCK}/6*1	—	f_{MCK}/6*1	bps	Figure x.x
			Theoretical value of the maximum transfer rate f_{MCK} = ICLK*3		—	5.3	—	4	—	0.33	Mbps	
		2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			—	f_{MCK}/6*1	—	f_{MCK}/6*1	—	f_{MCK}/6*1	bps	
			Theoretical value of the maximum transfer rate f_{MCK}*3 = ICLK*3		—	5.3	—	4	—	0.33	Mbps	
		1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			—	f_{MCK}/6*1 *2	—	f_{MCK}/6*1 *2	—	f_{MCK}/6*1 *2	bps	
			Theoretical value of the maximum transfer rate f_{MCK} = ICLK*3		—	5.3	—	4	—	0.33	Mbps	

Note 1. Transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.
Note 2. Use this rate with VCC ≥ V_b.
Note 3. The maximum operating frequencies of the system clock (ICLK) are:
High-speed mode: 32 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Middle-speed mode: 24 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Low-speed mode: 2 MHz (1.6 V ≤ VCC ≤ 5.5 V)

Note: Select the TTL input buffer for the RxDq pin and the N-ch open drain output [withstand voltage of VCC] mode for the TxDq pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Note:
- V_b[V]: Communication line voltage
- q: UART number (q = 0 to 2), gh: Port number (gh=100, 101, 109, 110, 212, 213)
- f_{MCK}: Serial array unit operation clock frequency

To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 03, 10, 11)

- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Table 2.28 In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V) (2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter				Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
					Min.	Max.	Min.	Max.	Min.	Max.		
Transfer rate	Transmission	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		—	—	*1	—	*1	—	*1	bps	Figure x.x
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		—	2.8*2	—	2.8*2	—	2.8*2	Mbps	
		2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			—	*3	—	*3	—	*3	bps	
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		—	1.2*4	—	1.2*4	—	1.2*4	Mbps	
		1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			—	*5 *6	—	*5 *6	—	*5 *6	bps	
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		—	0.43*7	—	0.43*7	—	0.43*7	Mbps	

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\left\{-C_b \times R_b \times \ln\left(1 - \frac{2.2}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \left\{-C_b \times R_b \times \ln\left(1 - \frac{2.2}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100[\%]$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This rate is calculated as an example when the conditions described in the Conditions column are met. See *1 above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\left\{-C_b \times R_b \times \ln\left(1 - \frac{2.0}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \left\{-C_b \times R_b \times \ln\left(1 - \frac{2.0}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100[\%]$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This rate is calculated as an example when the conditions described in the Conditions column are met. See *3 above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use this rate with VCC ≥ V_b.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\left\{-C_b \times R_b \times \ln\left(1 - \frac{1.5}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \left\{-C_b \times R_b \times \ln\left(1 - \frac{1.5}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100[\%]$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 7. This rate is calculated as an example when the conditions described in the Conditions column are met. See [*6] above to calculate the maximum transfer rate under conditions of the customer.

Note: Select the TTL input buffer for the RxDq pin and the N-ch open drain output [withstand voltage of VCC] mode for the TxDq pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

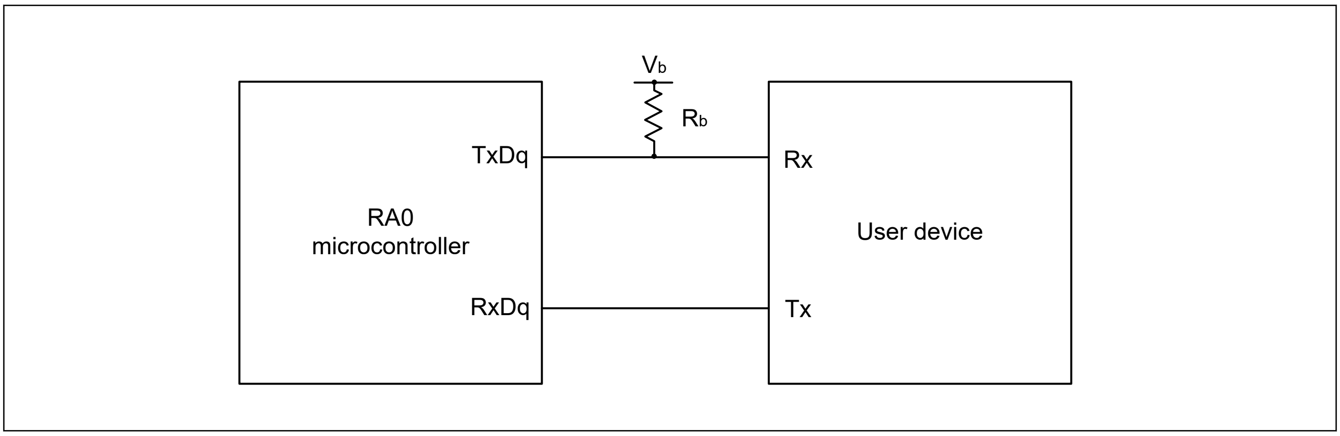


Figure 2.21 In UART communications with devices operating at different voltage levels

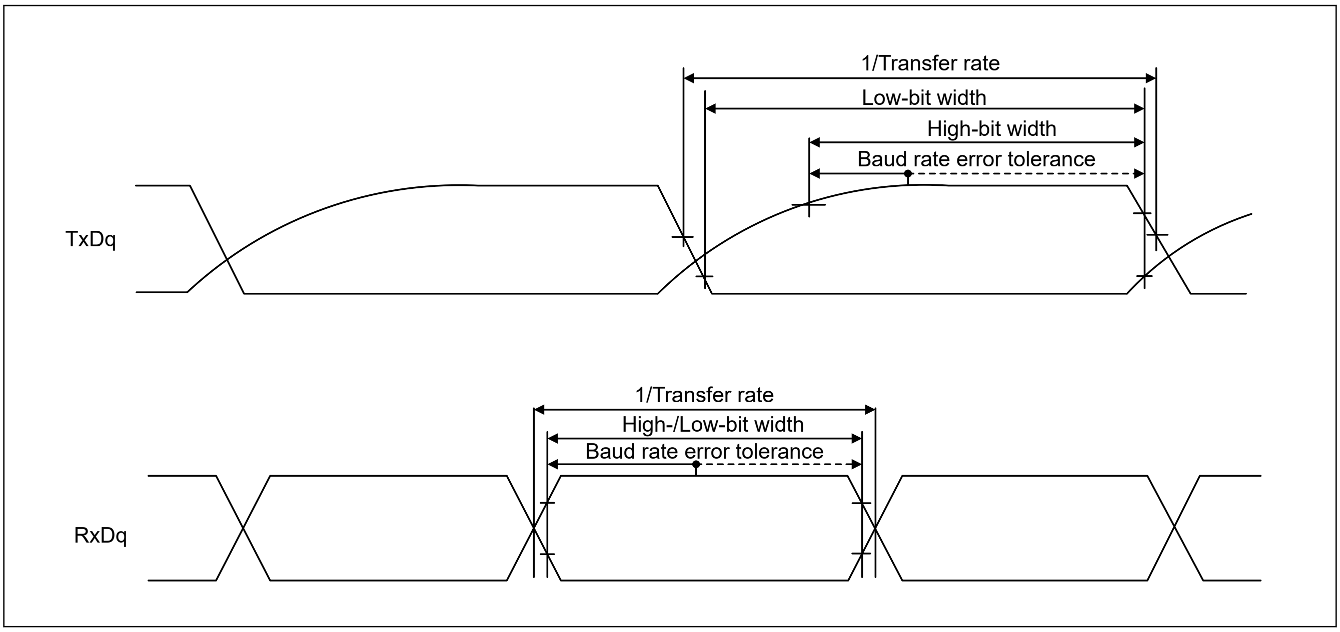


Figure 2.22 Bit width in the UART communications with devices operating at different voltage levels (reference)

Note:
- R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage
- q: UART number (q = 0 to 2), gh: Port number (gh = 100, 101, 109, 110, 212, 213)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 01, 02, 03, 10, 11)
- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Table 2.29 In simplified SPI communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to SPI00)

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	$t_{KCY1} \geq 2/ICLK$	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	t_{KCY1}	200	—	200	—	2300	—	ns	Figure x.x
		2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		300	—	300	—	2300	—	ns	
SCKp high-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KH1}	$t_{KCY1}/2$ - 50	—	$t_{KCY1}/2$ - 50	—	$t_{KCY1}/2$ - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			$t_{KCY1}/2$ - 120	—	$t_{KCY1}/2$ - 120	—	$t_{KCY1}/2$ - 120	—	ns	
SCKp low-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KL1}	$t_{KCY1}/2$ -7	—	$t_{KCY1}/2$ -7	—	$t_{KCY1}/2$ - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			$t_{KCY1}/2$ - 10	—	$t_{KCY1}/2$ - 10	—	$t_{KCY1}/2$ - 50	—	ns	
SIp setup time (to SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{SIK1}	58	—	58	—	479	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			121	—	121	—	479	—	ns	
SIp hold time (from SCKp↑)*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSI1}	10	—	10	—	10	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10	—	10	—	10	—	ns	
Delay time from SCKp↓ to SOp output*1	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSO1}	—	60	—	60	—	60	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			—	130	—	130	—	130	ns	
SIp setup time (to SCKp↓)*2	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{SIK1}	23	—	23	—	110	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			33	—	33	—	110	—	ns	
SIp hold time (from SCKp↓)*2	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSI1}	10	—	10	—	10	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10	—	10	—	10	—	ns	
Delay time from SCKp↑ to SOp output*2	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSO1}	—	10	—	10	—	10	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			—	10	—	10	—	10	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 00b or 11b.
Note 2. This setting applies when SCRmn.DCP[1:0] = 01b or 10b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Note:

- R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
- p: Simplified SPI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), gh: Port number (gh = 100 to 103, 112, 201)
- f_{MCK}: Serial array unit operation clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00)

Table 2.30 In simplified SPI communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock (1)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	t_{KCY1} ≥ 4/ICLK	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}	300	—	300	—	2300	—	ns	Figure x.x
		2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		500	—	500	—	2300	—	ns	
		1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V^{*1}, C_b = 30 pF, R_b = 5.5 kΩ		1150	—	1150	—	2300	—	ns	
SCKp high-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KH1}	t_{KCY1}/2 - 75	—	t_{KCY1}/2 - 75	—	t_{KCY1}/2 - 75	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			t_{KCY1}/2 - 170	—	t_{KCY1}/2 - 170	—	t_{KCY1}/2 - 170	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V^{*1}, C_b = 30 pF, R_b = 5.5 kΩ			t_{KCY1}/2 - 458	—	t_{KCY1}/2 - 458	—	t_{KCY1}/2 - 458	—	ns	
SCKp low-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KL1}	t_{KCY1}/2 -12	—	t_{KCY1}/2 -12	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			t_{KCY1}/2 - 18	—	t_{KCY1}/2 - 18	—	t_{KCY1}/2 - 50	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V^{*1}, C_b = 30 pF, R_b = 5.5 kΩ			t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	ns	

Note 1. Use this setting with VCC ≥ V_b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Table 2.31 In simplified SPI communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock (2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SIp setup time (to SCKp↑)[1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{SIK1}	81	—	81	—	479	—	ns	Figure x.x
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		177	—	177	—	479	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[2], C_b = 30 pF, R_b = 5.5 kΩ		479	—	479	—	479	—	ns	
SIp hold time (from SCKp↑)[1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSI1}	19	—	19	—	19	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		19	—	19	—	19	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[2], C_b = 30 pF, R_b = 5.5 kΩ		19	—	19	—	19	—	ns	
Delay time from SCKp↓ to SOp output[1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSO1}	—	100	—	100	—	100	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		—	195	—	195	—	195	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[2], C_b = 30 pF, R_b = 5.5 kΩ		—	483	—	483	—	483	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 00b or 11b.
Note 2. Use this setting with VCC ≥ V_b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Table 2.32 In simplified SPI communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock (3)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SIp setup time (to SCKp↓)[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{SIK1}	44	—	44	—	110	—	ns	Figure x.x
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		44	—	44	—	110	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ		110	—	110	—	110	—	ns	
SIp hold time (from SCKp↓)[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSI1}	19	—	19	—	19	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		19	—	19	—	19	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ		19	—	19	—	19	—	ns	
Delay time from SCKp↑ to SOp output[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSO1}	—	25	—	25	—	25	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		—	25	—	25	—	25	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ		—	25	—	25	—	25	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 01b or 10b.
Note 2. Use this setting with VCC ≥ V_b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

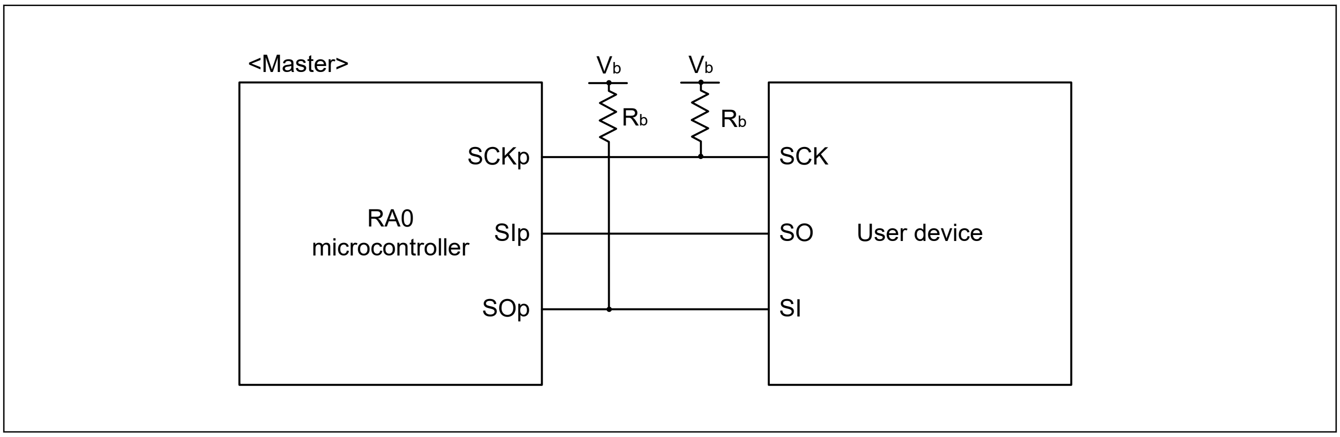


Figure 2.23 Connection in the simplified SPI communications with devices operating at different voltage levels

Note:
- R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

- p: Simplified SPI number (p = 00, 11, 20), m: Unit number, n: Channel number (mn = 00, 03, 10), gh: Port number (gh = 100 to 103, 109, 110, 112, 201, 212, 213, 407)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03, 10)
- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

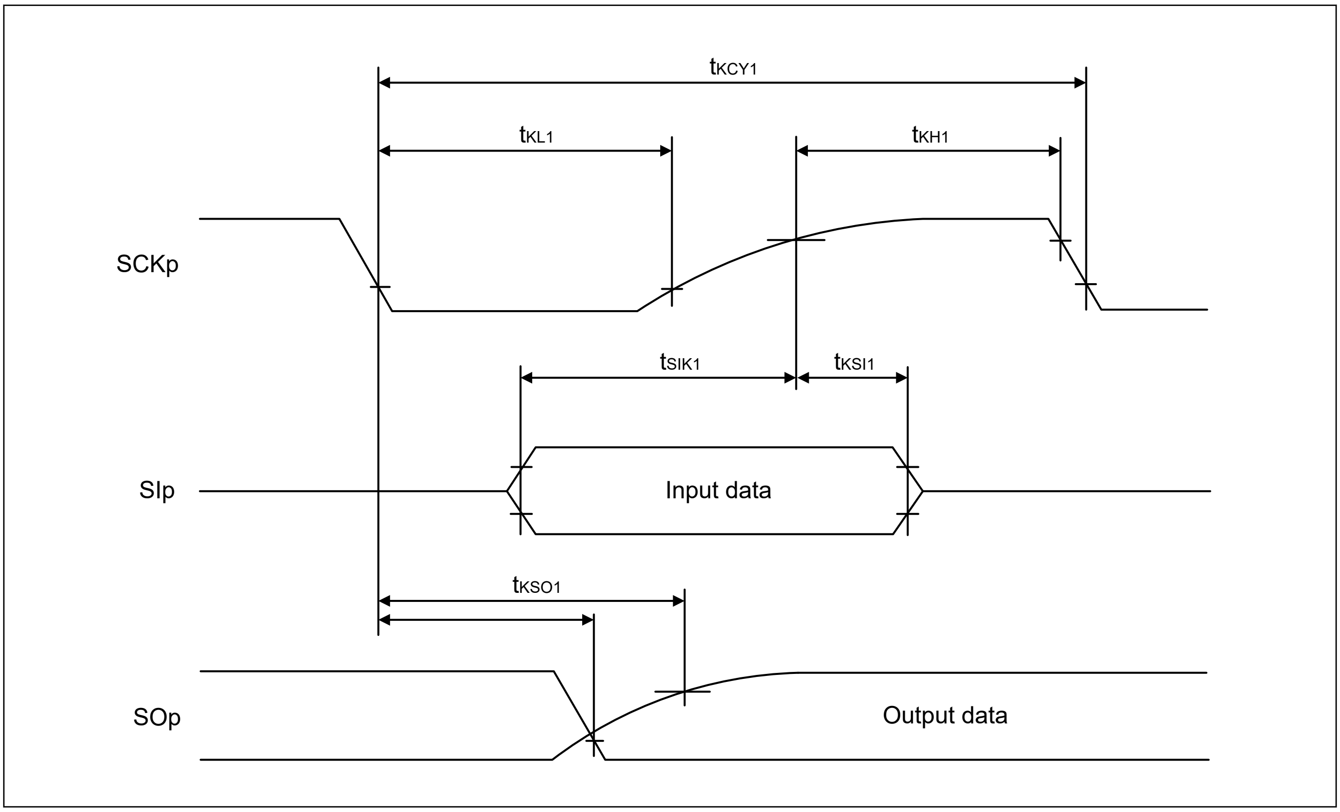


Figure 2.24 Timing of serial transfer in the simplified SPI communications in the master mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 00b or 11b

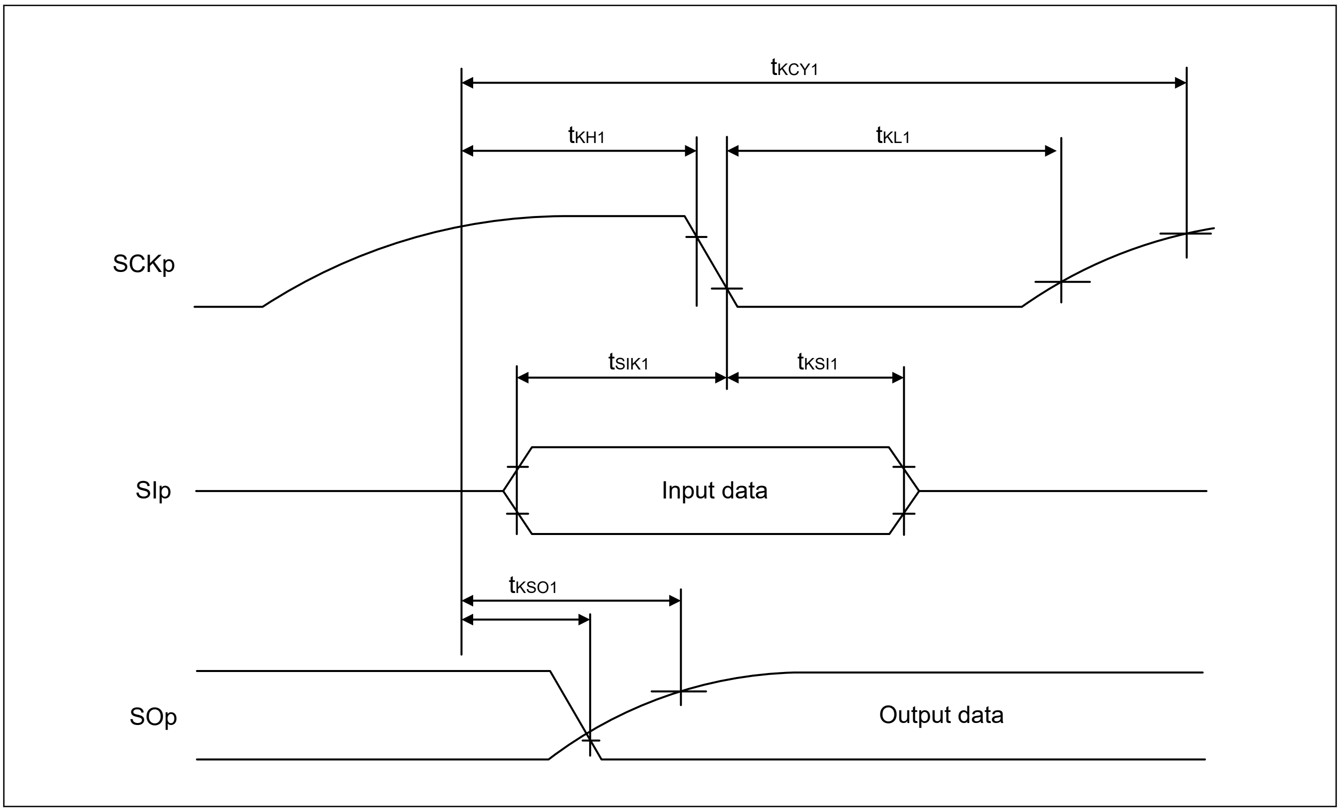


Figure 2.25 **Timing of serial transfer in the simplified SPI communications in the master mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 01b or 10b**

Note:
- p: Simplified SPI number (p = 00, 11, 20), m: Unit number, n: Channel number (mn = 00, 03, 10), gh: Port number (gh = 100 to 103, 109, 110, 112, 201, 212, 213, 407)
- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Table 2.33 In simplified SPI communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	t_{KCY2}	14/f_{MCK}	—	—	—	—	—	ns	Figurex.x
		20 MHz < f_{MCK} ≤ 24 MHz		12/f_{MCK}	—	12/f_{MCK}	—	—	—	ns	
		8 MHz < f_{MCK} ≤ 20 MHz		10/f_{MCK}	—	10/f_{MCK}	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		8/f_{MCK}	—	8/f_{MCK}	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		6/f_{MCK}	—	6/f_{MCK}	—	10/f_{MCK}	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}		20/f_{MCK}	—	—	—	—	—	ns	
		20 MHz < f_{MCK} ≤ 24 MHz		16/f_{MCK}	—	16/f_{MCK}	—	—	—	ns	
		16 MHz < f_{MCK} ≤ 20 MHz		14/f_{MCK}	—	14/f_{MCK}	—	—	—	ns	
		8 MHz < f_{MCK} ≤ 16 MHz		12/f_{MCK}	—	12/f_{MCK}	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		8/f_{MCK}	—	8/f_{MCK}	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		6/f_{MCK}	—	6/f_{MCK}	—	10/f_{MCK}	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2]	24 MHz < f_{MCK}		48/f_{MCK}	—	—	—	—	—	ns	
		20 MHz < f_{MCK} ≤ 24 MHz		36/f_{MCK}	—	36/f_{MCK}	—	—	—	ns	
		16 MHz < f_{MCK} ≤ 20 MHz		32/f_{MCK}	—	32/f_{MCK}	—	—	—	ns	
		8 MHz < f_{MCK} ≤ 16 MHz		26/f_{MCK}	—	26/f_{MCK}	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		16/f_{MCK}	—	16/f_{MCK}	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		10/f_{MCK}	—	10/f_{MCK}	—	10/f_{MCK}	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KH2}, t_{KL2}	t_{KCY2}/2 - 12	—	t_{KCY2}/2 - 12	—	t_{KCY2}/2 - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			t_{KCY2}/2 - 18	—	t_{KCY2}/2 - 18	—	t_{KCY2}/2 - 50	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2]			t_{KCY2}/2 - 50	—	t_{KCY2}/2 - 50	—	t_{KCY2}/2 - 50	—	ns	
SIp setup time (to SCKp↑)[*3]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{SIK2}	1/f_{MCK} + 20	—	1/f_{MCK} + 20	—	1/f_{MCK} + 30	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			1/f_{MCK} + 20	—	1/f_{MCK} + 20	—	1/f_{MCK} + 30	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2]			1/f_{MCK} + 30	—	1/f_{MCK} + 30	—	1/f_{MCK} + 30	—	ns	
SIp hold time (from SCKp↑)[*3]			t_{KSI2}	1/f_{MCK} + 31	—	1/f_{MCK} + 31	—	1/f_{MCK} + 31	—	ns	
Delay time from SCKp↓ to SOp output[*4]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KSO2}	—	2/f_{MCK} + 120	—	2/f_{MCK} + 120	—	2/f_{MCK} + 573	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			—	2/f_{MCK} + 214	—	2/f_{MCK} + 214	—	2/f_{MCK} + 573	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ			—	2/f_{MCK} + 573	—	2/f_{MCK} + 573	—	2/f_{MCK} + 573	ns	

Note 1. Transfer rate in the SNOOZE mode: 1 Mbps (max.)

Note 2. Use this setting with VCC ≥ V_b.

Note 3. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The SIp setup time becomes to SCKp↓ and SIp hold time becomes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.

Note 4. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The delay time to SOp output becomes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

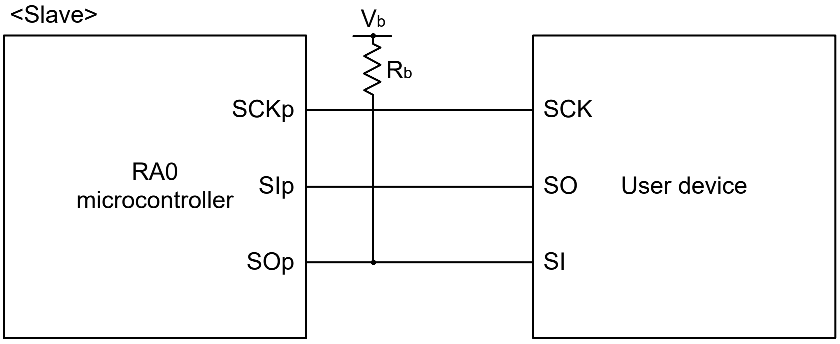


Figure 2.26 Connection in the simplified SPI communications with devices operating at different voltage levels

Note:

- R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage
- p: Simplified SPI number (p = 00, 11, 20), m: Unit number, n: Channel number (mn = 00, 03, 10), gh: Port number (gh = 100 to 103, 109, 110, 112, 201, 212, 213, 407)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03, 10)
- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

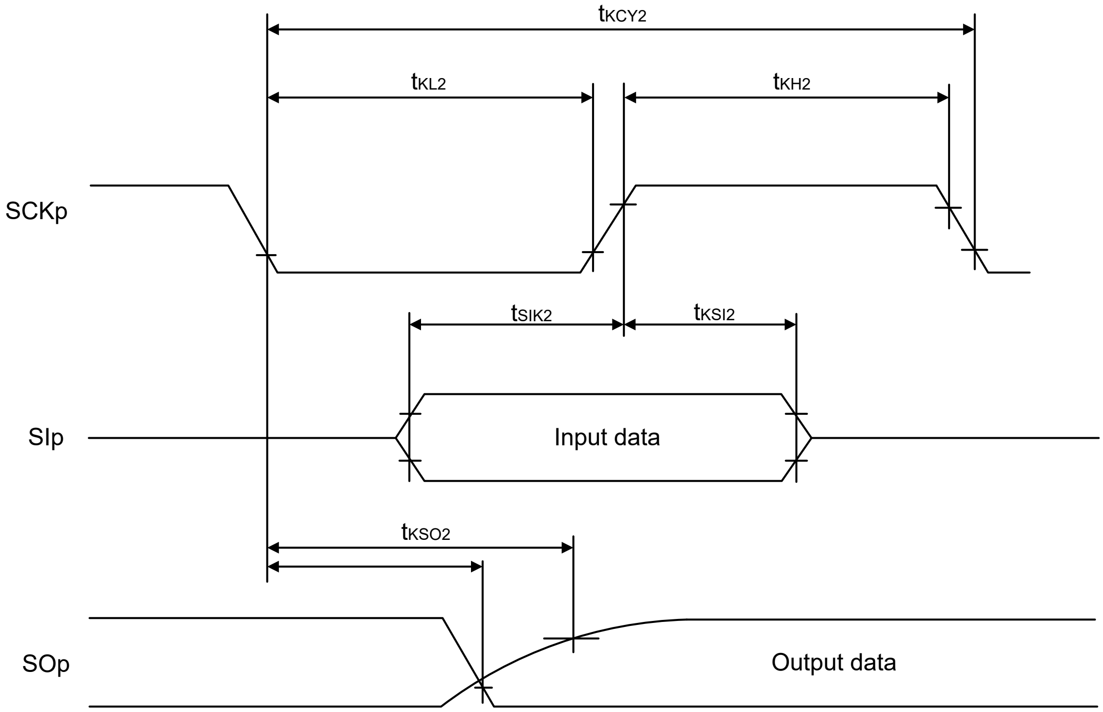


Figure 2.27 Timing of serial transfer in the simplified SPI communications in the slave mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 00b or 11b

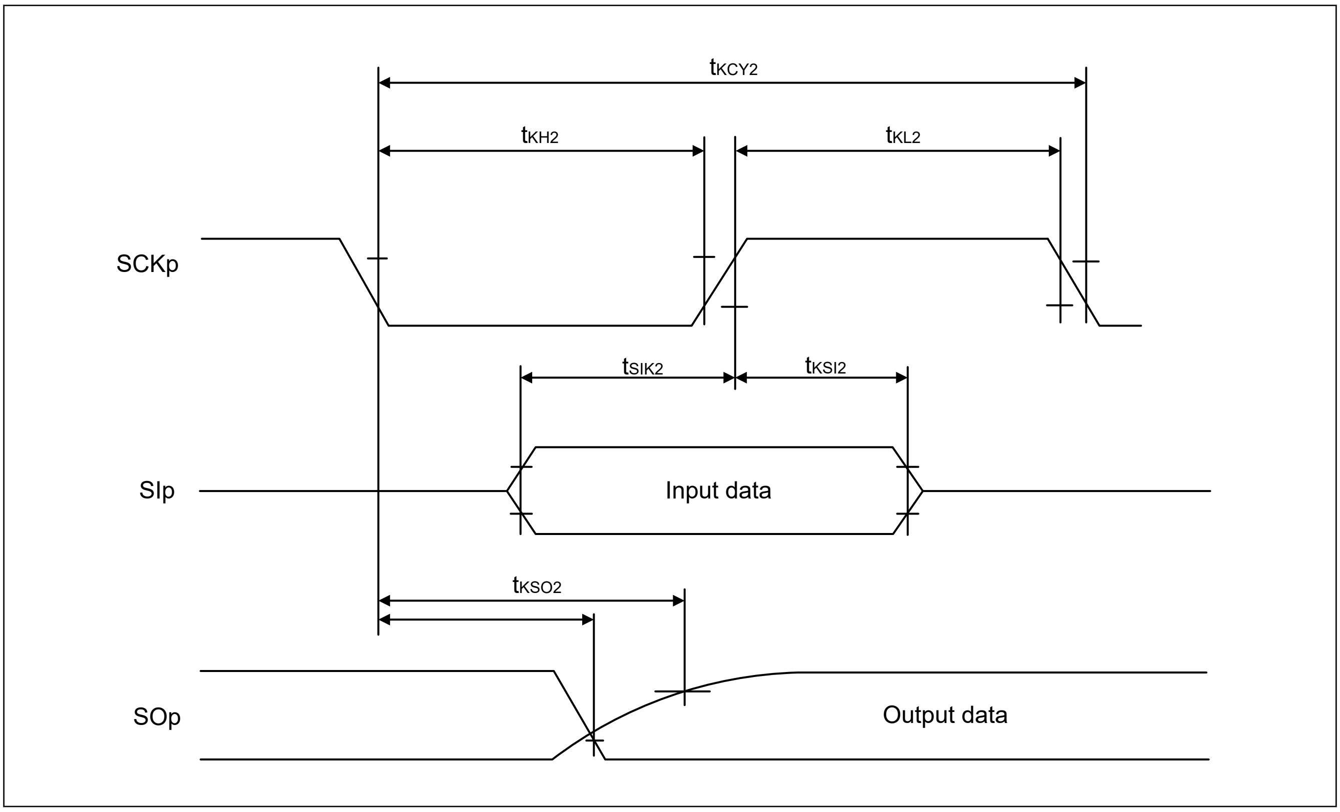


Figure 2.28 Timing of serial transfer in the simplified SPI communications in the slave mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 01b or 10b

Note:
- p: Simplified SPI number (p = 00, 11, 20), m: Unit number, n: Channel number (mn = 00, 03, 10), gh: Port number (gh = 100 to 103, 109, 110, 112, 201, 212, 213, 407)
- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Table 2.34 Simplified IIC communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) (1 of 2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SCLr clock frequency	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	f_{SCL}	—	1000[*1]	—	1000[*1]	—	300[*1]	kHz	Figure x.x
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		—	1000[*1]	—	1000[*1]	—	300[*1]	kHz	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		—	400[*1]	—	400[*1]	—	300[*1]	kHz	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		—	400[*1]	—	400[*1]	—	300[*1]	kHz	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		—	300[*1]	—	300[*1]	—	300[*1]	kHz	
Hold time when SCLr is low	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{LOW}	475	—	475	—	1550	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		475	—	475	—	1550	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		1150	—	1550	—	1550	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		1150	—	1550	—	1550	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		1550	—	1550	—	1550	—	ns	
Hold time when SCLr is high	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{HIGH}	245	—	245	—	610	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		200	—	200	—	610	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		675	—	675	—	610	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		600	—	600	—	610	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		610	—	610	—	610	—	ns	

Table 2.34 Simplified IIC communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) (2 of 2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
Data setup time (reception)	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{SU:DAT}$	$1/f_{MCK}+135^{*3}$	—	$1/f_{MCK}+135^{*3}$	—	$1/f_{MCK}+190^{*3}$	—	ns	Figure x.x
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		$1/f_{MCK}+135^{*3}$	—	$1/f_{MCK}+135^{*3}$	—	$1/f_{MCK}+190^{*3}$	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		$1/f_{MCK}+190^{*3}$	—	$1/f_{MCK}+190^{*3}$	—	$1/f_{MCK}+190^{*3}$	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		$1/f_{MCK}+190^{*3}$	—	$1/f_{MCK}+190^{*3}$	—	$1/f_{MCK}+190^{*3}$	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V^{*2}, C_b = 100 pF, R_b = 5.5 kΩ		$1/f_{MCK}+190^{*3}$	—	$1/f_{MCK}+190^{*3}$	—	$1/f_{MCK}+190^{*3}$	—	ns	
Data hold time (transmission)	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{HD:DAT}$	0	305	0	305	0	305	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		0	305	0	305	0	305	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		0	355	0	355	0	355	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		0	355	0	355	0	355	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V^{*2}, C_b = 100 pF, R_b = 5.5 kΩ		0	405	0	405	0	405	ns	

Note 1. The listed times must be no greater than $f_{MCK}/4$.

Note 2. Use this setting with VCC ≥ V_b.

Note 3. Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

Note: Select the TTL input buffer and the N-ch open drain output [withstand voltage of VCC] mode for the SDAr pin and the N-ch open drain output [withstand voltage of VCC] mode for the SCLr pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

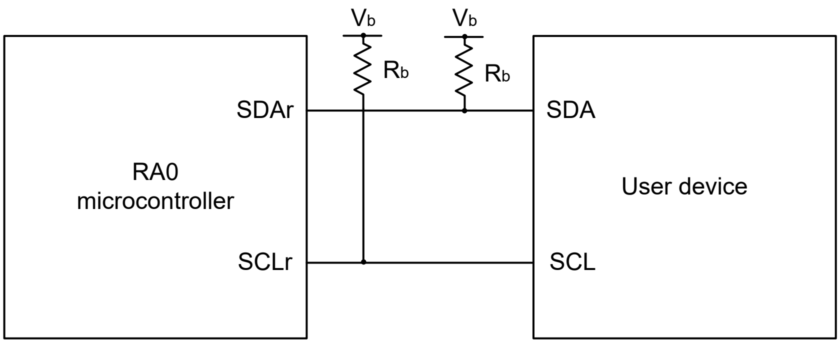


Figure 2.29 Connection in the IIC communications with devices operating at different voltage levels

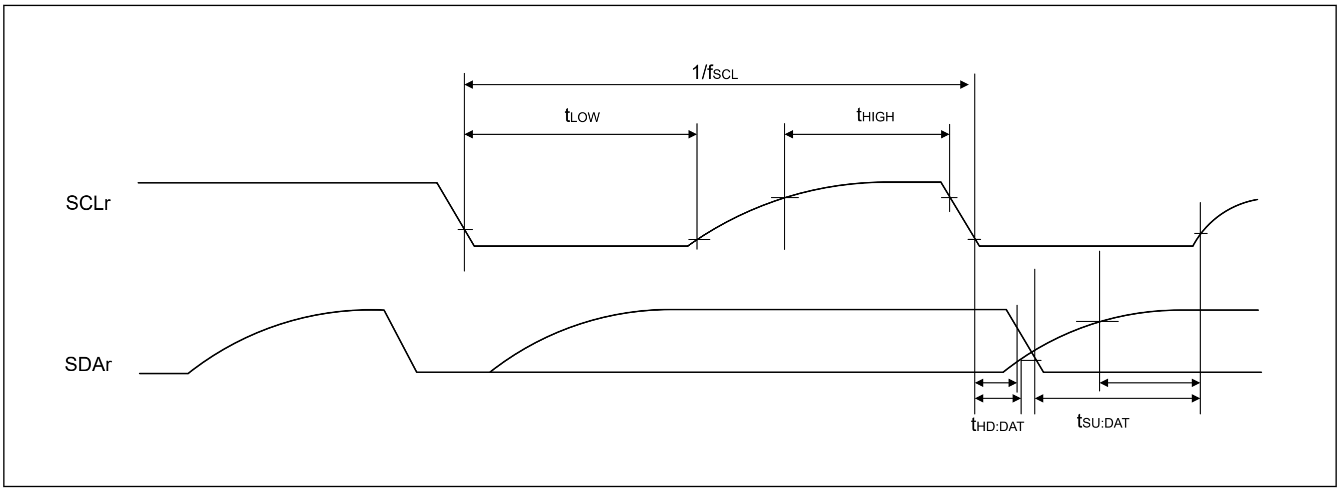


Figure 2.30 **Timing of serial transfer in the simplified IIC communications with devices operating at different voltage levels**

Note:

- R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage
- r: Simplified IIC number (r = 00, 11, 20), gh: Port number (gh = 100 to 102, 110, 112, 201, 212, 407)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03, 10)

2.5.2 UART Interface (UARTA)

Table 2.35 **UARTA communications**

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Transfer rate	—	200	0	153600	bps	—

Note: Select the normal input buffer for the RxDA0 pin and the normal output mode for the TxDA0 pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Note: n: Unit number (n = 0), gh: Port number (gh = 100, 101, 109, 110, 207, 208, 212, 213)

Note: Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

2.5.3 I^{2}C Bus Interface (IICA)

Table 2.36 I^{2}C standard mode

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLA0 clock frequency	Standard mode: ICLK ≥ 1 MHz	f_{SCL}	0	—	100	kHz	Figure x.x
Setup time of restart condition	—	$t_{SU:STA}$	4.7	—	—	μs	
Hold time[*1]	—	$t_{HD:STA}$	4	—	—	μs	
Hold time when SCLA0 is low	—	t_{LOW}	4.7	—	—	μs	
Hold time when SCLA0 is high	—	t_{HIGH}	4	—	—	μs	
Data setup time (reception)	—	$t_{SU:DAT}$	250	—	—	ns	
Data hold time (transmission)[*2]	—	$t_{HD:DAT}$	0	—	3.45	μs	
Setup time of stop condition	—	$t_{SU:STO}$	4	—	—	μs	
Bus-free time	—	t_{BUF}	4.7	—	—	μs	

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Note: Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Note: The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.

C_b = 400 pF, R_b = 2.7 kΩ

Table 2.37 I^{2}C fast mode

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLA0 clock frequency	Fast mode: ICLK ≥ 3.5 MHz 1.8 V ≤ VCC ≤ 5.5 V	f_{SCL}	0	—	400	kHz	Figure x.x
Setup time of restart condition	1.8 V ≤ VCC ≤ 5.5 V	$t_{SU:STA}$	0.6	—	—	μs	
Hold time[*1]	1.8 V ≤ VCC ≤ 5.5 V	$t_{HD:STA}$	0.6	—	—	μs	
Hold time when SCLA0 is low	1.8 V ≤ VCC ≤ 5.5 V	t_{LOW}	1.3	—	—	μs	
Hold time when SCLA0 is high	1.8 V ≤ VCC ≤ 5.5 V	t_{HIGH}	0.6	—	—	μs	
Data setup time (reception)	1.8 V ≤ VCC ≤ 5.5 V	$t_{SU:DAT}$	100	—	—	ns	
Data hold time (transmission)[*2]	1.8 V ≤ VCC ≤ 5.5 V	$t_{HD:DAT}$	0	—	0.9	μs	
Setup time of stop condition	1.8 V ≤ VCC ≤ 5.5 V	$t_{SU:STO}$	0.6	—	—	μs	
Bus-free time	1.8 V ≤ VCC ≤ 5.5 V	t_{BUF}	1.3	—	—	μs	

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Note: Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Note: The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.

C_b = 320 pF, R_b = 1.1 kΩ

Table 2.38 I^2C fast mode plus

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLA0 clock frequency	Fast mode plus: ICLK ≥ 10 MHz 2.7 V ≤ VCC ≤ 5.5 V	f_{SCL}	0	—	1000	kHz	Figure x.x
Setup time of restart condition	2.7 V ≤ VCC ≤ 5.5 V	$t_{SU:STA}$	0.26	—	—	µs	
Hold time[*1]	2.7 V ≤ VCC ≤ 5.5 V	$t_{HD:STA}$	0.26	—	—	µs	
Hold time when SCLA0 is low	2.7 V ≤ VCC ≤ 5.5 V	t_{LOW}	0.5	—	—	µs	
Hold time when SCLA0 is high	2.7 V ≤ VCC ≤ 5.5 V	t_{HIGH}	0.26	—	—	µs	
Data setup time (reception)	2.7 V ≤ VCC ≤ 5.5 V	$t_{SU:DAT}$	50	—	—	ns	
Data hold time (transmission)[*2]	2.7 V ≤ VCC ≤ 5.5 V	$t_{HD:DAT}$	0	—	0.45	µs	
Setup time of stop condition	2.7 V ≤ VCC ≤ 5.5 V	$t_{SU:STO}$	0.26	—	—	µs	
Bus-free time	2.7 V ≤ VCC ≤ 5.5 V	t_{BUF}	0.5	—	—	µs	

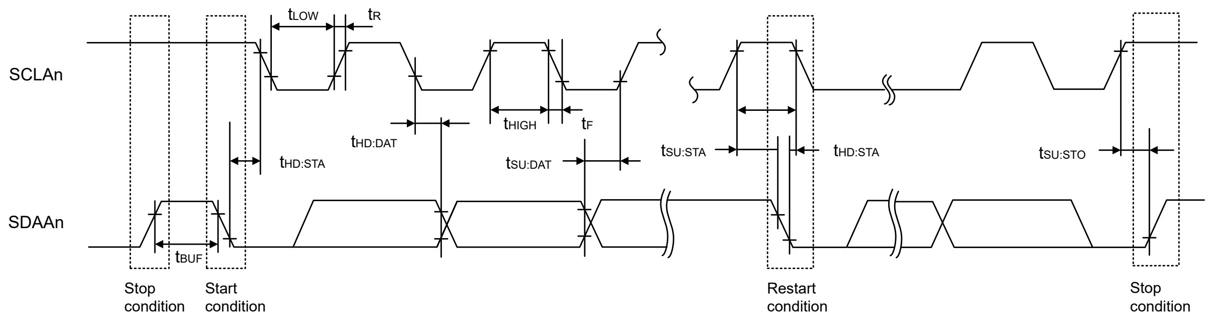
Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Note: Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Note: The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.

C_b = 120 pF, R_b = 1.1 kΩ



Note: n = 0

Figure 2.31 IICA serial transfer timing

2.6 Analog Characteristics

2.6.1 A/D Converter Characteristics

Table 2.39 A/D conversion characteristics in Normal modes 1 and 2 (1 of 2)

Conditions: 2.4V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C
Reference voltage range applied to the VREFH0 (ADVREFP[1:0] = 01b) and VREFL0 (ADVREFM = 1b).
Target pins: AN000 to AN007, internal reference voltage, and temperature sensor output voltage

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution	RES	8	—	12	bit	—
Conversion clock	f_{AD}	1	—	32	MHz	—

Table 2.39 A/D conversion characteristics in Normal modes 1 and 2 (2 of 2)

Conditions: 2.4V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C
Reference voltage range applied to the VREFH0 (ADVREFP[1:0] = 01b) and VREFL0 (ADVREFM = 1b).
Target pins: AN000 to AN007, internal reference voltage, and temperature sensor output voltage

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Overall error[*1 *3 *4 *5]	12-bit resolution	AINL	—	—	±7.5	LSB	4.5 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±9.0	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±9.0	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
Conversion time[*6]	12-bit resolution	t_{CONV}	2.0	—	—	μs	4.5 V ≤ VREFH0 = VCC ≤ 5.5 V
			2.0	—	—	μs	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			2.0	—	—	μs	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
Zero-scale error[*1 *2 *3 *4 *5]	12-bit resolution	E_{ZS}	—	—	±0.17	%FSR	4.5 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.21	%FSR	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.21	%FSR	2.4 V ≤ VREFH 0 =VCC ≤ 5.5 V
Full-scale error[*1 *2 *3 *4 *5]	12-bit resolution	E_{FS}	—	—	±0.17	%FSR	4.5 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.21	%FSR	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.21	%FSR	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
Integral linearity error[*1 *4 *5]	12-bit resolution	ILE	—	—	±3.0	LSB	4.5 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±3.0	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±3.0	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
Differential linearity error[*1]	12-bit resolution	DLE	—	±1.0	—	LSB	4.5 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±1.0	—	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±1.0	—	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
Analog input voltage		V_{AIN}	0	—	VREFH0	V	—

Note 1. This value does not include the quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3. When pins AN021 to AN022 are selected as the target pins for conversion, the maximum values are as follows.
Overall error: Add ±3 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.
Note 4. When reference voltage (+) = VCC (ADVREF[1:0] = 00b) and reference voltage (-) = VSS (ADVREFM = 0b), the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.
Integral linearity error: Add ±4 LSB to the maximum value.
Note 5. When VREFH0 < VCC, the maximum values are as follows.
Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (VCC voltage (V) - VREFH0 voltage (V)) to the maximum value.
Integral linearity error: Add (±0.2 LSB × (VCC voltage (V) - VREFH0 voltage (V)) to the maximum value.
Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 μs. Accordingly, use standard mode 2 with the longer sampling time.

Table 2.40 A/D conversion characteristics in Low-voltage modes 1 and 2 (1) (1 of 2)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C
Reference voltage range applied to the VREFH0 (ADVREFP[1:0] = 01b) and VREFL0 (ADVREFM = 1b).
Target pins: AN000 to AN007, internal reference voltage[*7], and temperature sensor output voltage[*7]

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		RES	8	—	12	bit	—
Conversion clock		f_{AD}	1	—	24	MHz	—
Overall error[*1 *3 *4 *5]	12-bit resolution	AINL	—	—	±9	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±9	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±11.5	LSB	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±12.0	LSB	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V

Table 2.40 A/D conversion characteristics in Low-voltage modes 1 and 2 (1) (2 of 2)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C
Reference voltage range applied to the VREFH0 (ADVREFP[1:0] = 01b) and VREFL0 (ADVREFM = 1b).
Target pins: AN000 to AN007, internal reference voltage[7], and temperature sensor output voltage[7]

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Conversion time[6]	12-bit resolution	t_{CONV}	3.3	—	—	μs	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			5.0	—	—	μs	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			10.0	—	—	μs	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			20.0	—	—	μs	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Zero-scale error[1] [2] [3] [4] [5]	12-bit resolution	E_{ZS}	—	—	±0.21	%FSR	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.21	%FSR	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.27	%FSR	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.28	%FSR	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Full-scale error[1] [2] [3] [4] [5]	12-bit resolution	E_{FS}	—	—	±0.21	%FSR	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.21	%FSR	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.27	%FSR	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±0.28	%FSR	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Integral linearity error[1] [4] [5]	12-bit resolution	ILE	—	—	±4.0	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±4.0	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±4.5	LSB	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	—	±4.5	LSB	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Differential linearity error[1]	12-bit resolution	DLE	—	±1.5	—	LSB	2.7 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±1.5	—	LSB	2.4 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±2.0	—	LSB	1.8 V ≤ VREFH0 = VCC ≤ 5.5 V
			—	±2.0	—	LSB	1.6 V ≤ VREFH0 = VCC ≤ 5.5 V
Analog input voltage		V_{AIN}	0	—	VREFH0	V	—

Note 1. This value does not include the quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3. When pins AN021 to AN022 are selected as the target pins for conversion, the maximum values are as follows.
Overall error: Add ±3 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.
Note 4. When reference voltage (+) = VCC (ADVREF[1:0] = 00b) and reference voltage (-) = VSS (ADVREFM = 0b), the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.
Integral linearity error: Add ±4 LSB to the maximum value.
Note 5. When VREFH0 < VCC, the maximum values are as follows.
Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (VCC voltage (V) - VREFH0 voltage (V)) to the maximum value.
Integral linearity error: Add (±0.2 LSB × (VCC voltage (V) - VREFH0 voltage (V)) to the maximum value.
Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 μs. Accordingly, use standard mode 2 with the longer sampling time, and use the conversion clock (f_{AD}) of no more than 16 MHz.
Note 7. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VCC must be at least 1.8 V.

Table 2.41 A/D conversion characteristics in Low-voltage modes 1 and 2 (2) (1 of 2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C
Reference voltage range applied to the internal reference voltage (ADVREFP[1:0] = 10b) and VREFL0 (ADVREFM = 1b).

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution	RES	8			bit	—
Conversion clock	f_{AD}	1	—	2	MHz	1.8 V ≤ VCC ≤ 5.5 V
Zero-scale error[1] [2] [4]	E_{ZS}	—	—	±0.6	%FSR	1.8 V ≤ VCC ≤ 5.5 V
Integral linearity error[1] [4]	ILE	—	—	±2.0	LSB	1.8 V ≤ VCC ≤ 5.5 V

Table 2.41 A/D conversion characteristics in Low-voltage modes 1 and 2 (2) (2 of 2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C
Reference voltage range applied to the internal reference voltage (ADVREFP[1:0] = 10b) and VREFL0 (ADVREFM = 1b).

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Differential linearity error[*1]	DLE	—	±1.0	—	LSB	1.8 V ≤ VCC ≤ 5.5 V
Analog input voltage	V_{AIN}	0	—	VBGR[*3]	V	—

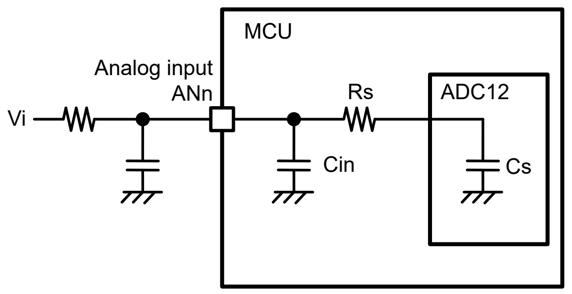
Note 1. This value does not include the quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3. Refer to Table 2.43.
Note 4. When reference voltage (-) is selected as VSS, the maximum values are as follows.
Zero-scale error: Add ±0.35%FSR to the maximum value.
Integral linearity error: Add ±0.5 LSB to the maximum value.

Table 2.42 Resistance and capacitance values of equivalent circuit (Reference data)

Parameter			Min	Typ	Max	Unit	Test conditions
Analog input capacitance	Cin	Refer to I/O input capacitance (Cin), see Table 2.11.					
	Cs[*2]	High-precision channel[*1]	—	—	9	pF	—
		Normal-precision channel[*1]	—	—	10		—
Analog input resistance	Rs[*2]	High-precision channel[*1]	—	—	11	kΩ	VCC = 2.4 to 5.5 V
			—	—	55		VCC = 1.8 to 2.4 V
			—	—	110		VCC = 1.6 to 1.8 V
		Normal-precision channel[*1]	—	—	12		VCC = 2.4 to 5.5 V
			—	—	60		VCC = 1.8 to 2.4 V
			—	—	120		VCC = 1.6 to 1.8 V

Note 1. AN000 to AN007 are the High-precision channels. AN021 and AN022 are the Normal- precision channels.
Note 2. These values are based on simulation. They are not production tested.

Figure 2.32 shows the equivalent circuit for analog input.



Note: Terminal leakage current is not shown in this figure.

Figure 2.32 Equivalent circuit for analog input

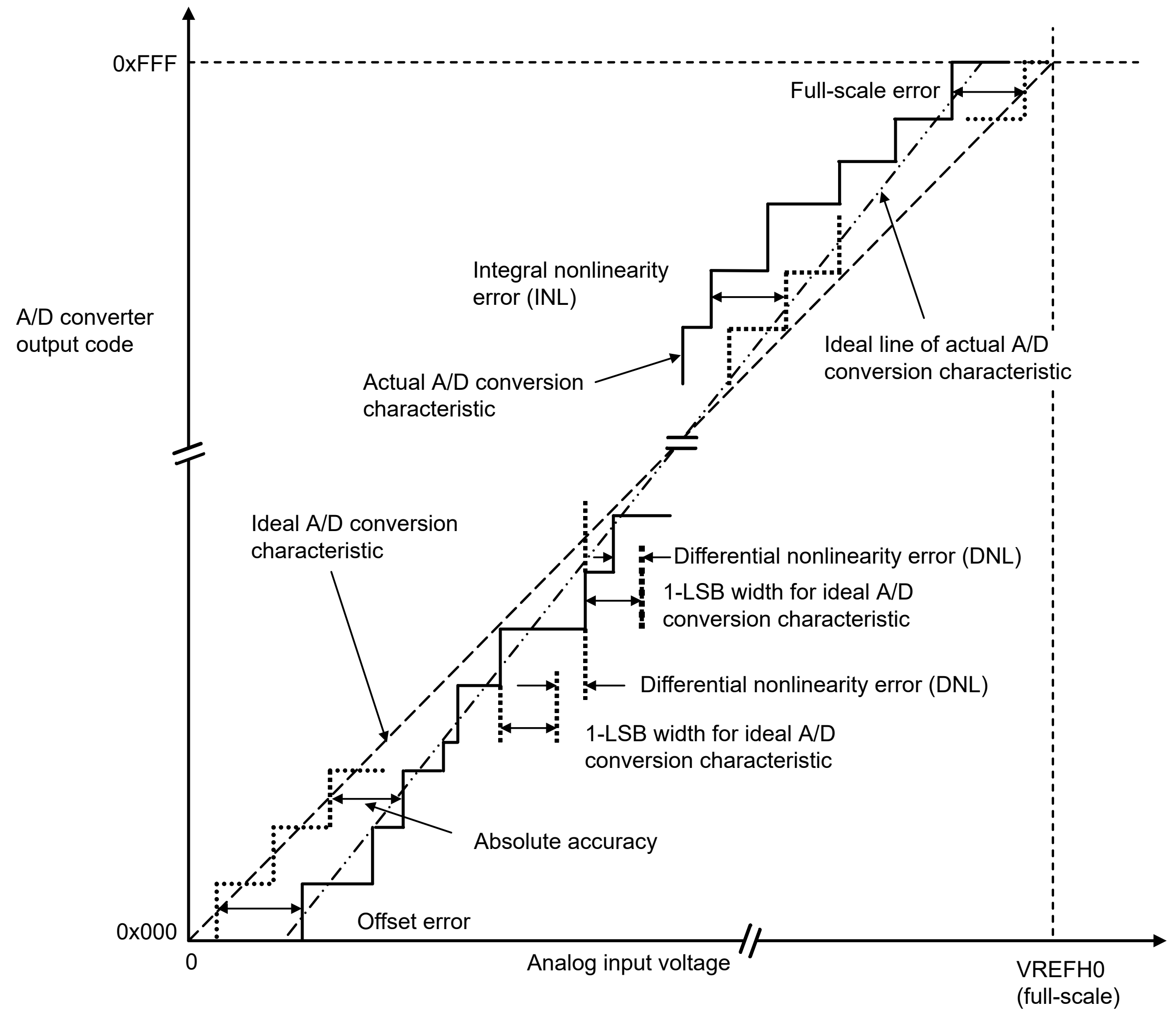


Figure 2.33 Illustration of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6.2 Temperature Sensor/Internal Reference Voltage Characteristics

Table 2.43 Temperature sensor/internal reference voltage characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Temperature sensor output voltage	V_{TMPS25}	—	1.05	—	V	—
Internal reference voltage	V_{BGR}	1.40	1.48	1.56	V	—
Temperature coefficient	F_{VTMPS}	—	-3.3	—	mV/°C	—
Operation stabilization wait time	t_{AMP}	5	—	—	µs	—

2.6.3 POR Characteristics

Table 2.44 POR characteristics

Conditions: VSS = 0 V, Ta = -40 to +105°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Detection voltage	VPOR VPDR	1.43	1.50	1.57	V	—
Minimum pulse width[*1]	TPW	300	—	—	µs	—

Note 1. This width is the minimum time required for a POR reset when VCC falls below VPDR. This width is also the minimum time required for a POR reset from when VCC falls below 0.7 V to when VCC exceeds VPOR in the Software standby mode or while the main system clock is stopped through setting HOCOCR.HCSTOP bit and MOSCCR.MOSTP bit.

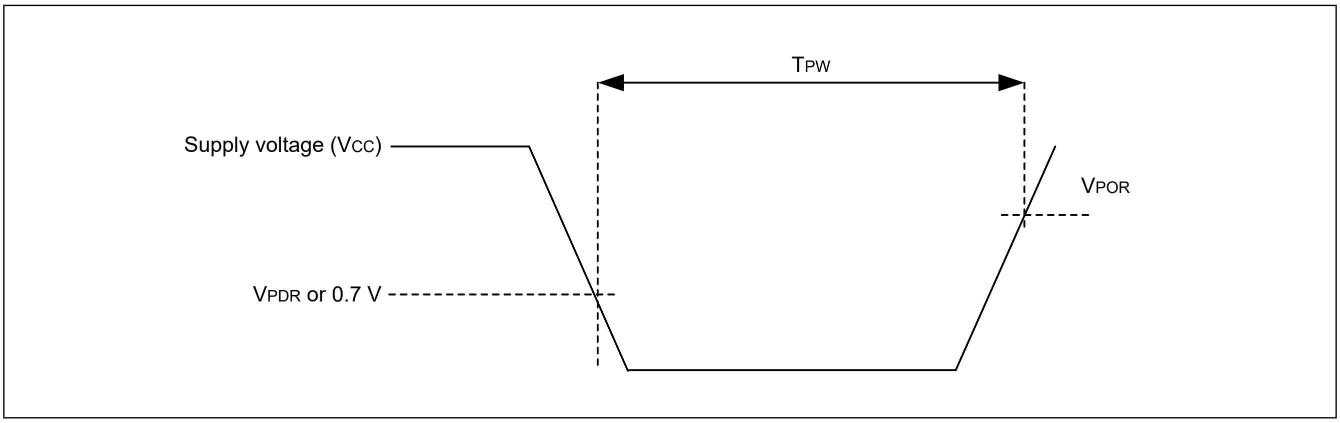


Figure 2.34 Minimum VCC pulse width

2.6.4 LVD Characteristics

Table 2.45 LVD0 characteristics

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det0_0}	3.84	3.96	4.08	V	The power supply voltage is rising.
			3.76	3.88	4.00	V	The power supply voltage is falling.
		V_{det0_1}	2.88	2.97	3.06	V	The power supply voltage is rising.
			2.82	2.91	3.00	V	The power supply voltage is falling.
		V_{det0_2}	2.59	2.67	2.75	V	The power supply voltage is rising.
			2.54	2.62	2.70	V	The power supply voltage is falling.
		V_{det0_3}	2.31	2.38	2.45	V	The power supply voltage is rising.
			2.26	2.33	2.40	V	The power supply voltage is falling.
		V_{det0_4}	1.84	1.90	1.95	V	The power supply voltage is rising.
			1.80	1.86	1.91	V	The power supply voltage is falling.
		V_{det0_5}	1.64	1.69	1.74	V	The power supply voltage is rising.
			1.60	1.65	1.70	V	The power supply voltage is falling.
Minimum pulse width		t_{LW}	500	—	—	μs	—
Detection delay time		—	—	—	500	μs	—

Table 2.46 LVD1 characteristics (1 of 2)

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det1_0}	4.08	4.16	4.24	V	The power supply voltage is rising.
			4.00	4.08	4.16	V	The power supply voltage is falling.
		V_{det1_1}	3.88	3.96	4.04	V	The power supply voltage is rising.
			3.80	3.88	3.96	V	The power supply voltage is falling.
		V_{det1_2}	3.68	3.75	3.82	V	The power supply voltage is rising.
			3.60	3.67	3.74	V	The power supply voltage is falling.
		V_{det1_3}	3.48	3.55	3.62	V	The power supply voltage is rising.
			3.40	3.47	3.54	V	The power supply voltage is falling.
		V_{det1_4}	3.28	3.35	3.42	V	The power supply voltage is rising.
			3.20	3.27	3.34	V	The power supply voltage is falling.
		V_{det1_5}	3.07	3.13	3.19	V	The power supply voltage is rising.
			3.00	3.06	3.12	V	The power supply voltage is falling.
		V_{det1_6}	2.91	2.97	3.03	V	The power supply voltage is rising.
			2.85	2.91	2.97	V	The power supply voltage is falling.
		V_{det1_7}	2.76	2.82	2.87	V	The power supply voltage is rising.
			2.70	2.76	2.81	V	The power supply voltage is falling.
		V_{det1_8}	2.61	2.66	2.71	V	The power supply voltage is rising.
			2.55	2.60	2.65	V	The power supply voltage is falling.
		V_{det1_9}	2.45	2.50	2.55	V	The power supply voltage is rising.
			2.40	2.45	2.50	V	The power supply voltage is falling.
		V_{det1_A}	2.35	2.40	2.45	V	The power supply voltage is rising.
			2.30	2.35	2.40	V	The power supply voltage is falling.

Table 2.46 LVD1 characteristics (2 of 2)

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det1_B}	2.25	2.30	2.34	V	The power supply voltage is rising.
			2.20	2.25	2.29	V	The power supply voltage is falling.
		V_{det1_C}	2.15	2.20	2.24	V	The power supply voltage is rising.
			2.10	2.15	2.19	V	The power supply voltage is falling.
		V_{det1_D}	2.05	2.09	2.13	V	The power supply voltage is rising.
			2.00	2.04	2.08	V	The power supply voltage is falling.
		V_{det1_E}	1.94	1.98	2.02	V	The power supply voltage is rising.
			1.90	1.94	1.98	V	The power supply voltage is falling.
		V_{det1_F}	1.84	1.88	1.91	V	The power supply voltage is rising.
			1.80	1.84	1.87	V	The power supply voltage is falling.
		V_{det1_10}	1.74	1.78	1.81	V	The power supply voltage is rising.
			1.70	1.74	1.77	V	The power supply voltage is falling.
		V_{det1_11}	1.64	1.67	1.70	V	The power supply voltage is rising.
			1.60	1.63	1.66	V	The power supply voltage is falling.
Minimum pulse width		t_{LW}	500	—	—	μs	—
Detection delay time		—	—	—	500	μs	—

2.6.5 Power Supply Voltage Rising Slope Characteristics

Table 2.47 Power supply voltage rising slope characteristics

Conditions: VSS = 0 V, Ta = -40 to +105°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Power supply voltage rising slope	S_{VCC}	—	—	54	V/ms	—

Note: Make sure to keep the internal reset state by the LVD0 circuit or an external reset until VCC reaches the operating voltage range shown in AC characteristics.

2.7 RAM Data Retention Characteristics

Table 2.48 RAM data retention characteristics

Conditions: VSS = 0 V, Ta = -40 to +105°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	1.43[*1]	—	5.5	V	—

Note 1. This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.

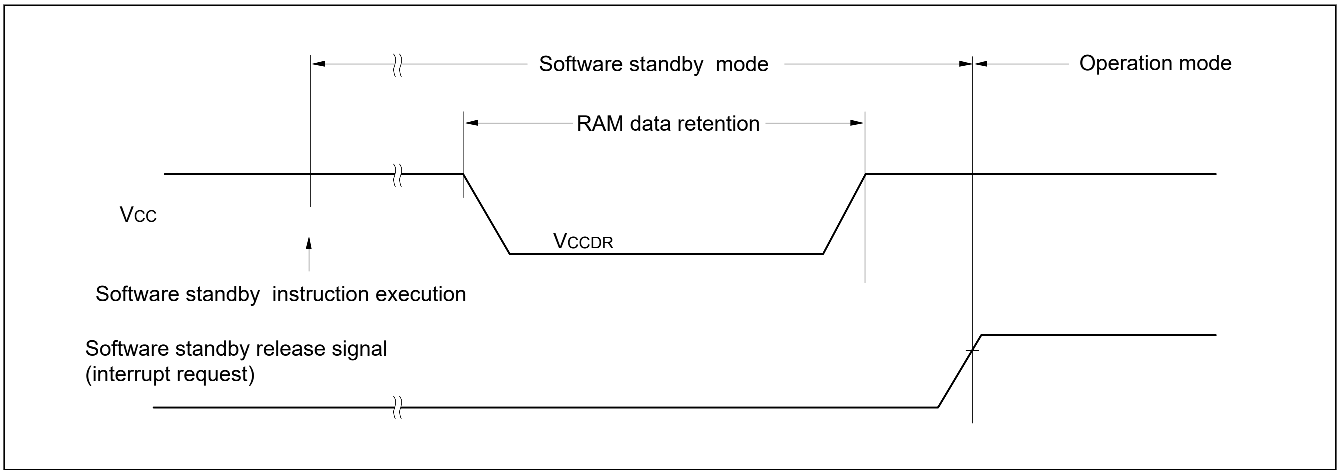


Figure 2.35 RAM data retention

2.8 Flash Memory Programming Characteristics

Table 2.49 Flash memory programming characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
CPU/peripheral hardware clock frequency	I_{CLK}	1	—	32	MHz	—
Number of code flash rewrites[*1 *2 *3]	Cerwr	10000	—	—	Times	Retained for 10 years Ta = 85°C
		1000	—	—		Retained for 20 years Ta = 85°C
Number of data flash rewrites[*1 *2 *3]		—	1000000	—		Retained for 1 year Ta = 25°C
		100000	—	—		Retained for 5 years Ta = 85°C
		10000	—	—		Retained for 20 years Ta = 85°C

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. The listed numbers of times apply when using the flash memory programmer and the Renesas Electronics self-programming library.

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Table 2.50 Code flash memory characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz, 3 MHz			4 MHz ≤ ICLK < 8 MHz			8 MHz ≤ ICLK < 32 MHz			ICLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programming time	4 bytes	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	μs
Erasure time	2 Kbytes	t_{E2K}	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	ms
Blank checking time	4 bytes	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	μs
	2 Kbytes	t_{BC2K}	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	μs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	μs
Security setting time		t_{AWSSAS}	—	18.0	525.5	—	14.3	468.7	—	12.5	440.7	—	11.6	426.7	—	11.3	422.3	ms
Time until programming starts following cancellation of the Software standby instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	2	—	—	2	—	—	2	—	—	μs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	15	—	—	15	—	—	15	—	—	μs

Note: The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

Table 2.51 Data flash memory characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz, 3 MHz			4 MHz ≤ ICLK < 8 MHz			8 MHz ≤ ICLK < 32 MHz			ICLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programming time	1 byte	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	256 bytes	t_{E2K}	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	ms
Blank checking time	1 byte	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	256 bytes	t_{BC2K}	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Time until programming starts following cancellation of the Software standby instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs
Time until reading starts following setting DFLEN to 1		t_{DSTOP}	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	µs
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	2	—	—	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	15	—	—	15	—	—	15	—	—	µs

Note: The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2.9 Serial Wire Debug (SWD)

Table 2.52 SWD characteristics (1)

Conditions: VCC = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 2.36
SWCLK clock high pulse width	t_{SWCKH}	35	—	—	ns	
SWCLK clock low pulse width	t_{SECKL}	35	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	16	—	—	ns	Figure 2.37
SWDIO hold time	t_{SWDH}	16	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	70	ns	

Table 2.53 SWD characteristics (2)

Conditions: VCC = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	—	—	ns	Figure 2.36
SWCLK clock high pulse width	t_{SWCKH}	120	—	—	ns	
SWCLK clock low pulse width	t_{SECKL}	120	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	50	—	—	ns	Figure 2.37
SWDIO hold time	t_{SWDH}	50	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	170	ns	

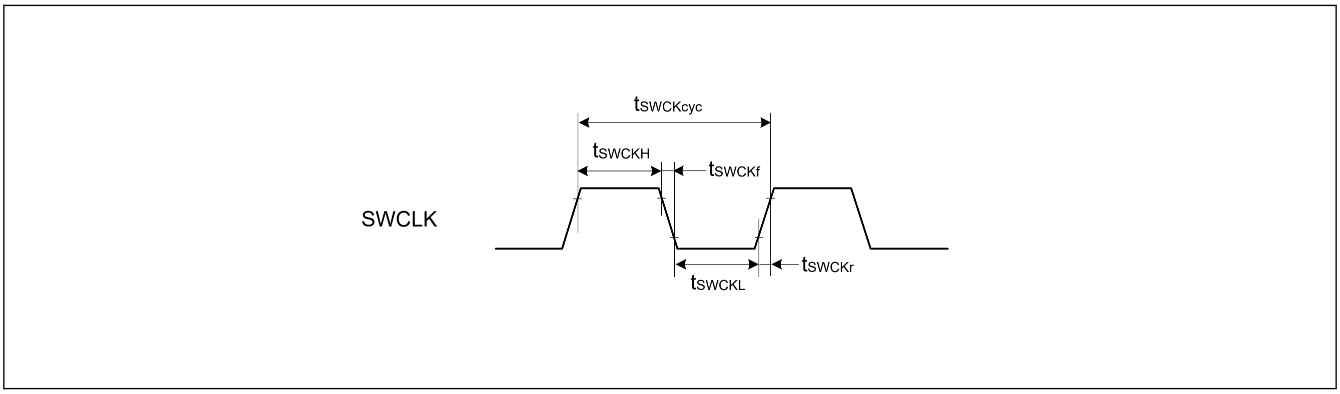


Figure 2.36 SWD SWCLK timing

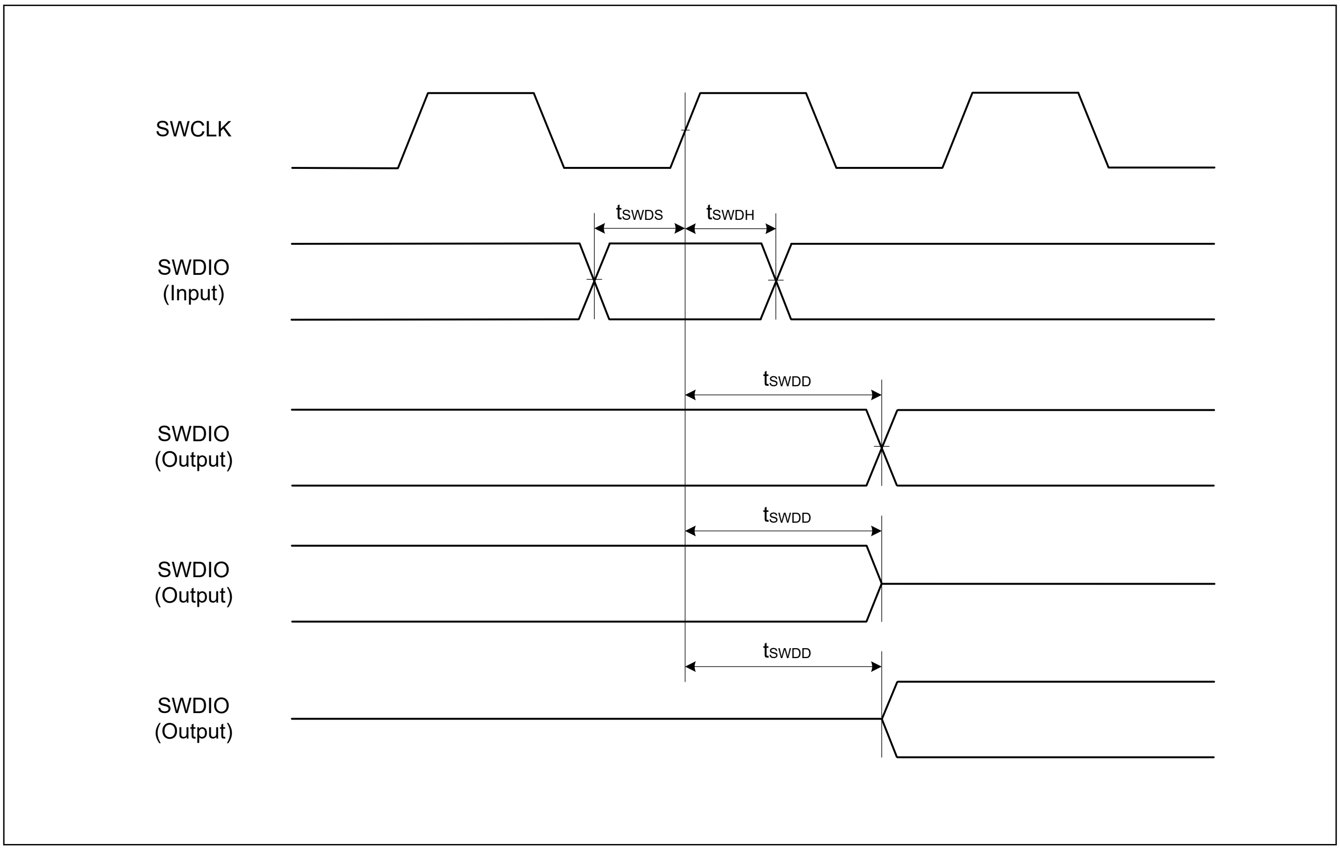


Figure 2.37 SWD input/output timing

Revision 1.00 — January 31, 2024

Initial release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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