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April 1st, 2010
Renesas Electronics Corporation

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7546 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0160-0122

Rev.1.22

Mar 13, 2009

DESCRIPTION

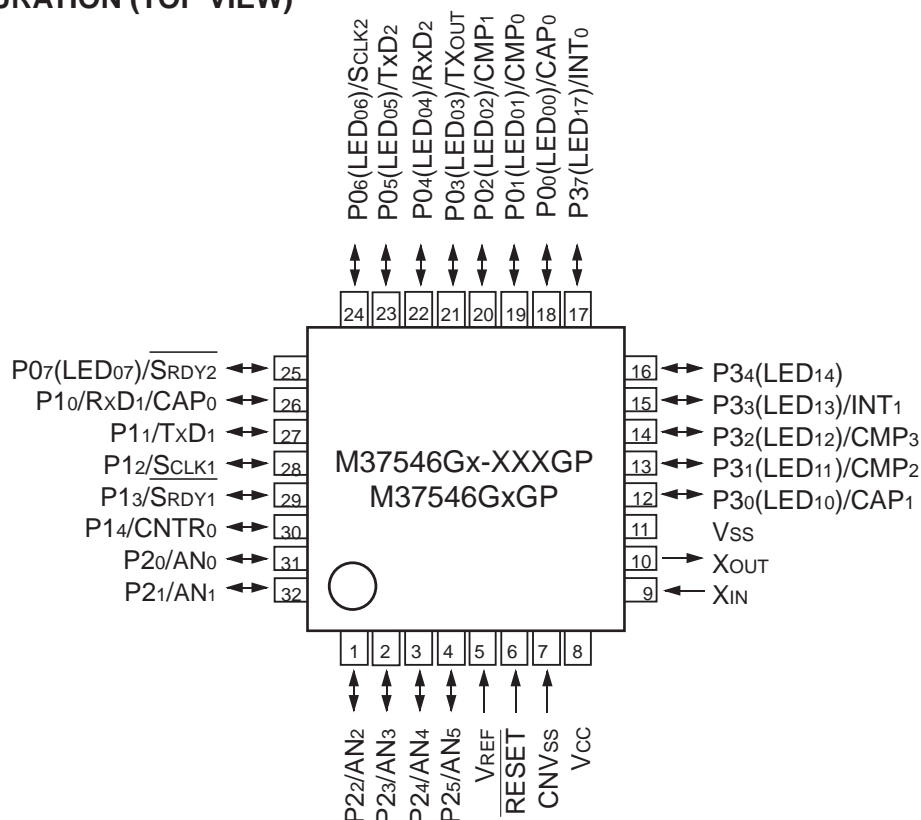
The 7546 Group is the QzROM version of 7542 Group.

The 7546 Group has the pin-compatibility with the 7542 Group. As new functions, the power-on reset, the low voltage detection circuit, and the function set ROM are added.

FEATURES

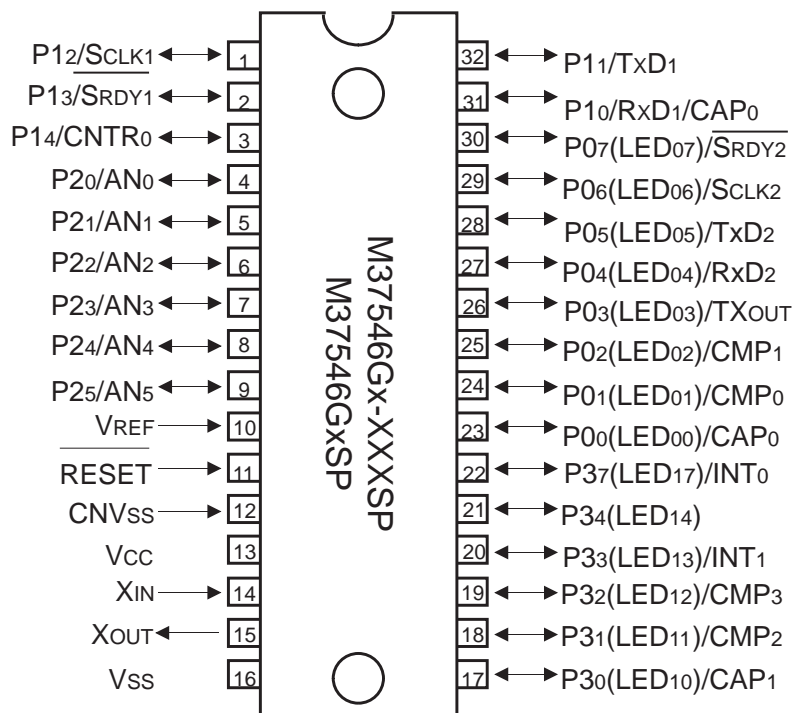
- Basic machine-language instructions 71
- The minimum instruction execution time 0.25 μ s
(at 8 MHz oscillation frequency, double-speed mode for the shortest instruction)
- Memory size
 - ROM 8K, 16K bytes
 - RAM 384, 512 bytes
- Programmable I/O ports 25
- Interrupts 18 sources, 16 vectors
- Timers 8-bit \times 2
..... 16-bit \times 2
- Output compare 4-channel
- Input capture 2-channel
- Serial interface 8-bit \times 2 (UART or Clock-synchronized)
- A/D converter 10-bit \times 6 channels
- Clock generating circuit Built-in type
(low-power dissipation by an on-chip oscillator)
(connected to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)

- Watchdog timer 16-bit \times 1
- Power-on reset circuit Built-in type
- Low voltage detection circuit Built-in type
- Power source voltage
 - XIN oscillation frequency at ceramic oscillation, in double-speed mode
 - At 8 MHz 4.5 to 5.5 V
 - At 6.5 MHz 4.0 to 5.5 V
 - At 2 MHz 2.4 to 5.5 V
 - At 1 MHz 2.2 to 5.5 V
 - XIN oscillation frequency at ceramic oscillation, in high-speed mode or middle-speed mode
 - At 8 MHz 4.0 to 5.5 V
 - At 4 MHz 2.4 to 5.5 V
 - At 2 MHz 2.2 to 5.5 V
 - XIN oscillation frequency at RC oscillation in high-speed mode or middle-speed mode
 - At 4 MHz 4.0 to 5.5 V
 - At 2 MHz 2.4 to 5.5 V
 - At 1 MHz 2.2 to 5.5 V
 - XIN oscillation frequency at on-chip oscillation 1.8 to 5.5 V
- Power dissipation 29.5 mW (Typ.)
- Operating temperature range -20 to 85 $^{\circ}$ C

PIN CONFIGURATION (TOP VIEW)

Package type: PLQP0032GB-A (32P6U-A)

Fig. 1 Pin configuration (Package type: PLQP0032GB-A)



Package type: PRDP0032BA-A (32P4B)

Fig. 2 Pin configuration (Package type: PRDP0032BA-A)

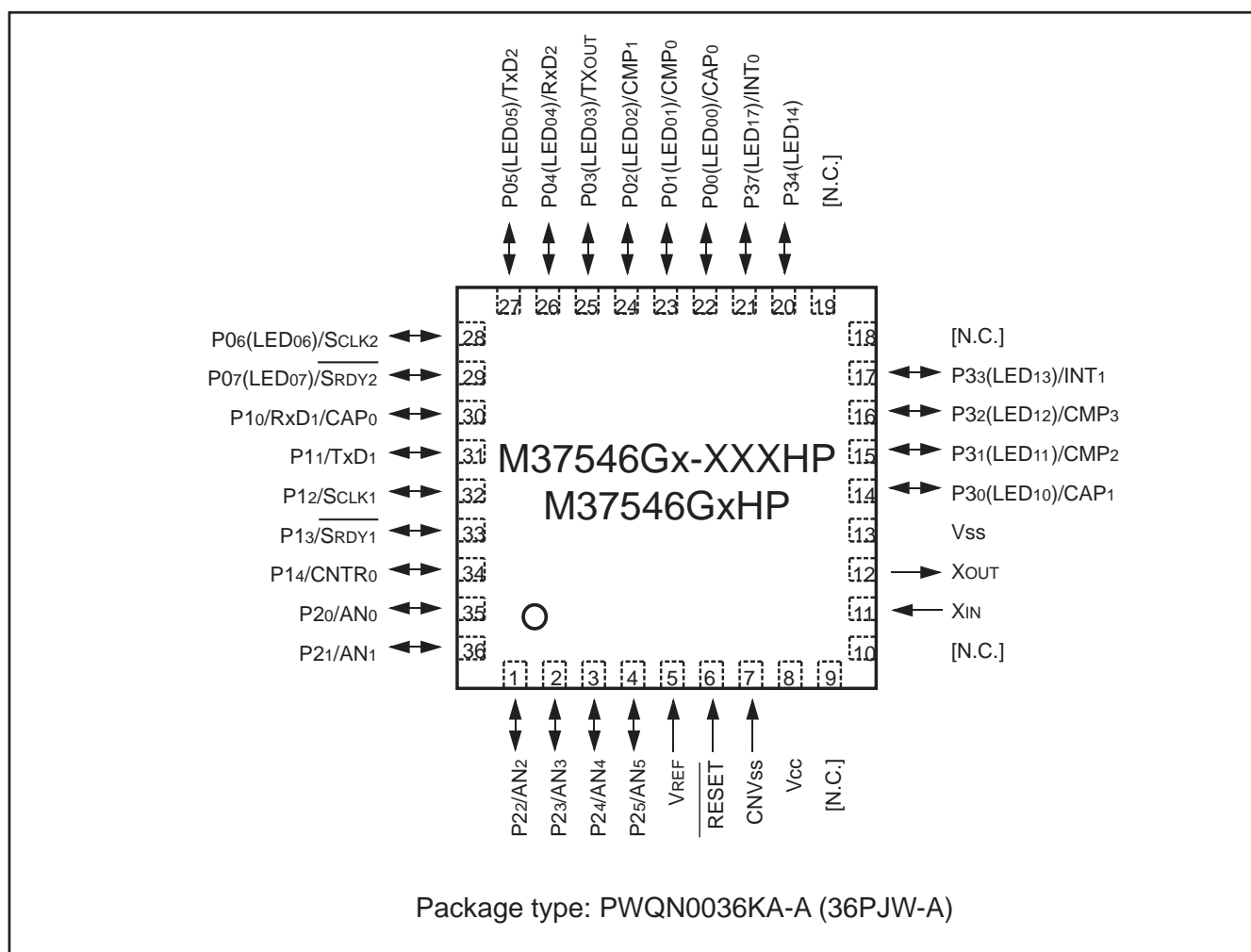


Fig. 3 Pin configuration (Package type: PWQN0036KA-A)

Table 1 Performance overview

| Parameter | | | Function |
|--|-------------------|-----------------------|--|
| Number of basic instructions | | | 71 |
| Instruction execution time | | | 0.25 μs (Minimum instruction, oscillation frequency 8 MHz: double-speed mode) |
| Oscillation frequency | | | 8 MHz (max.) |
| Memory sizes | ROM | | 8 K to 16 K bytes |
| | RAM | | 384 to 512 bytes |
| I/O port | P0, P1, P2, P3 | | •8-bit X 1, 6-bit X 2, 5-bit X 1 |
| Interrupts | | | 18 sources, 16 vectors |
| Timer | | | •8-bit X 2, 16-bit X 2 |
| Output compare | | | 4 channel |
| Input capture | | | 2 channel |
| Serial interface | | | 8-bit X 2 (UART or clock synchronous) |
| A/D converter | | | 10-bit X 6 channel |
| Watchdog timer | | | 16-bit X 1 |
| Clock generating circuit | | | Built-in (external ceramic resonator or quartz-crystal oscillator, RC oscillation available) (Low consumption current by on-chip oscillator available) |
| Power source voltage (at ceramic resonance) | Double-speed mode | At 8MHz oscillation | 4.5 to 5.5 V |
| | | At 6.5MHz oscillation | 4.0 to 5.5 V |
| | | At 2MHz oscillation | 2.4 to 5.5 V |
| | | At 1MHz oscillation | 2.2 to 5.5 V |
| | High-speed mode | At 8MHz oscillation | 4.0 to 5.5 V |
| | Middle-speed mode | At 4MHz oscillation | 2.4 to 5.5 V |
| | | At 2MHz oscillation | 2.2 to 5.5 V |
| Power source voltage (at RC oscillation) | High-speed mode | At 4MHz oscillation | 4.0 to 5.5 V |
| | Middle-speed mode | At 2MHz oscillation | 2.4 to 5.5 V |
| | | At 1MHz oscillation | 2.2 to 5.5 V |
| Power source voltage (at on-chip oscillation) | | | 1.8 to 5.5 V |
| Power dissipation | | | 29.5 mW (Typ.) |
| Operating temperature range | | | -20 to 85 °C |
| Device structure | | | CMOS silicon gate |
| Package | | | 32-pin plastic molded SDIP/LQFP |
| | | | 36-pin plastic molded WQFN |

FUNCTIONAL BLOCK

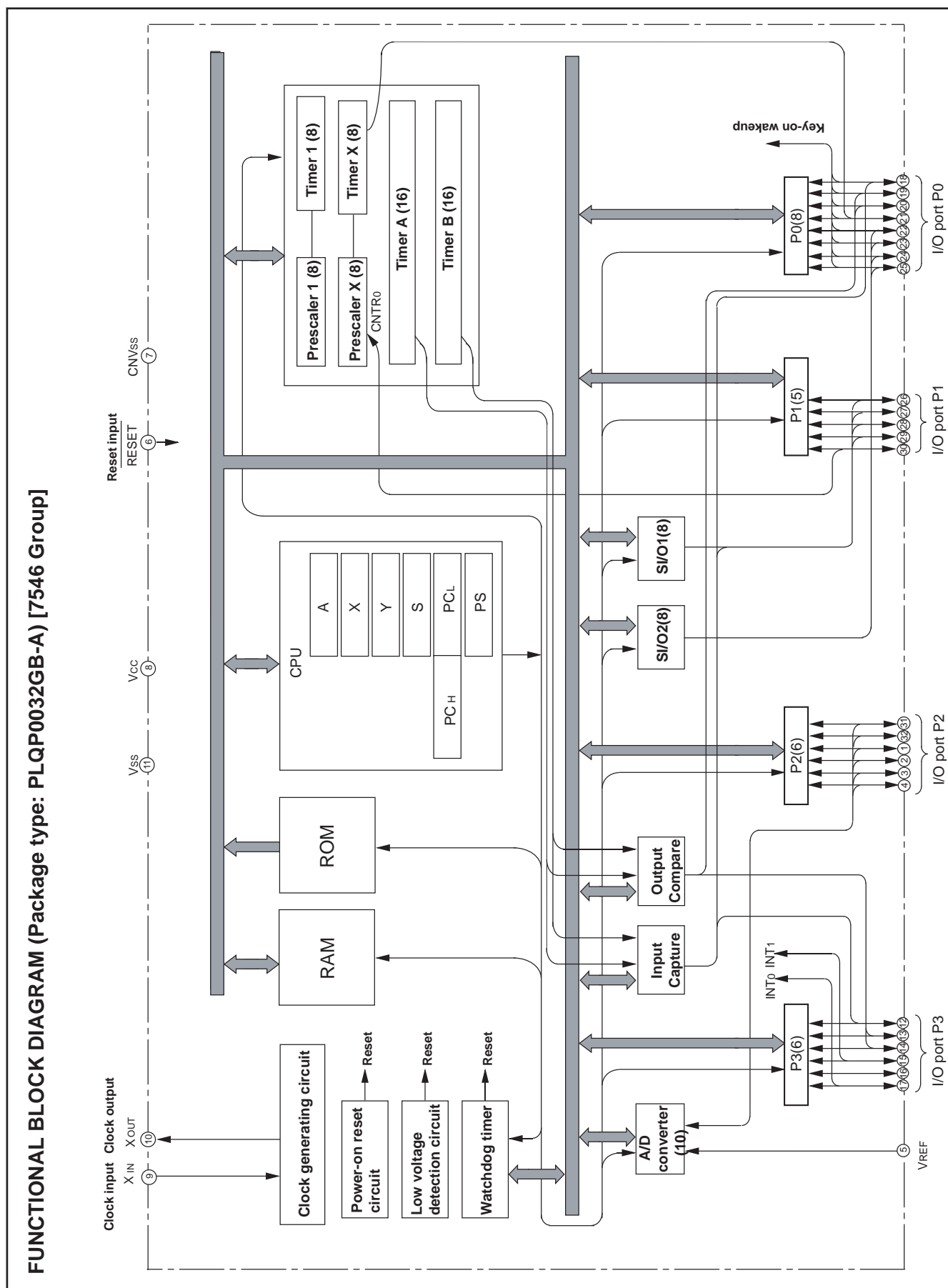


Fig. 4 Functional block diagram (Package type: PLQP0032GB-A)

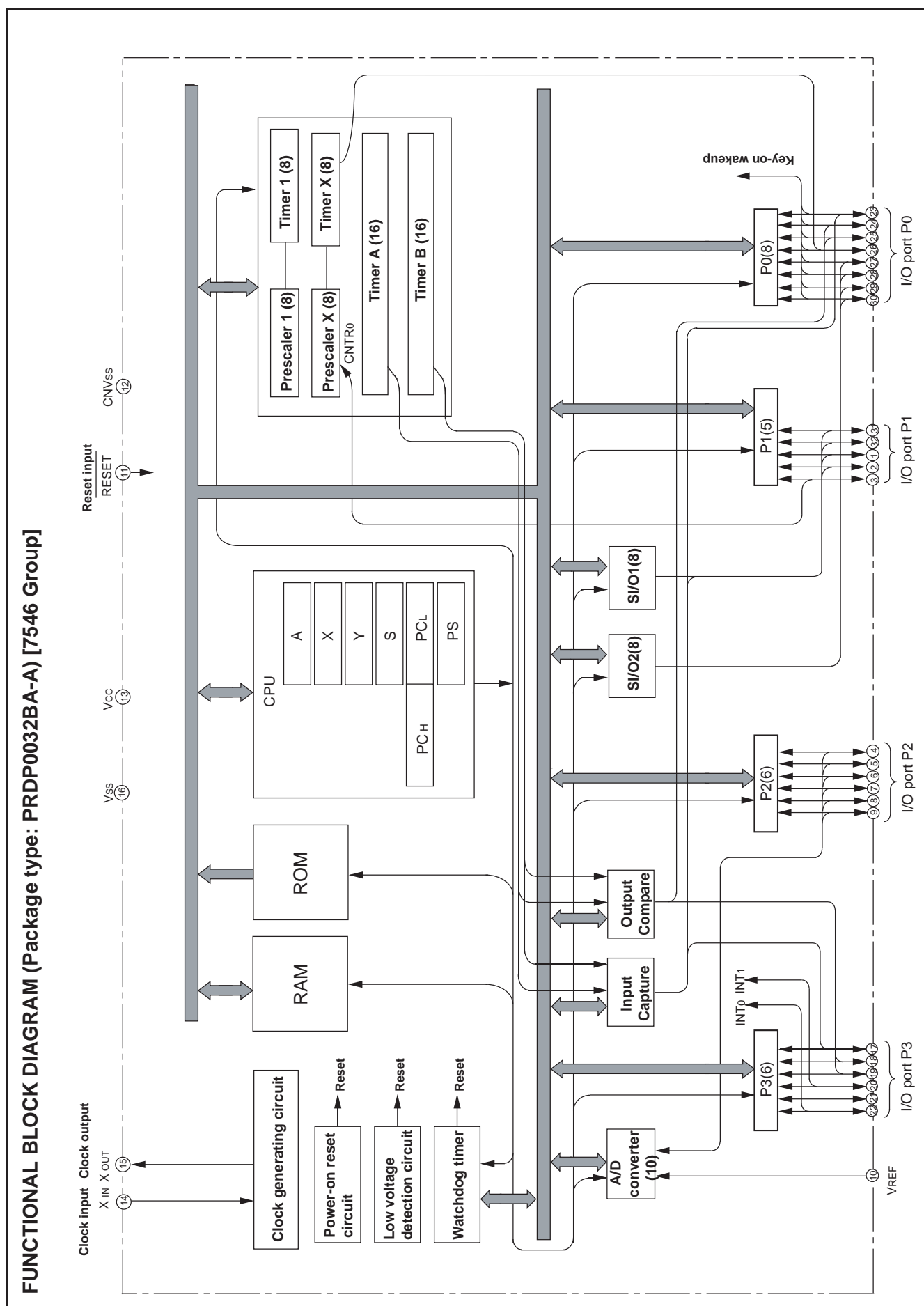
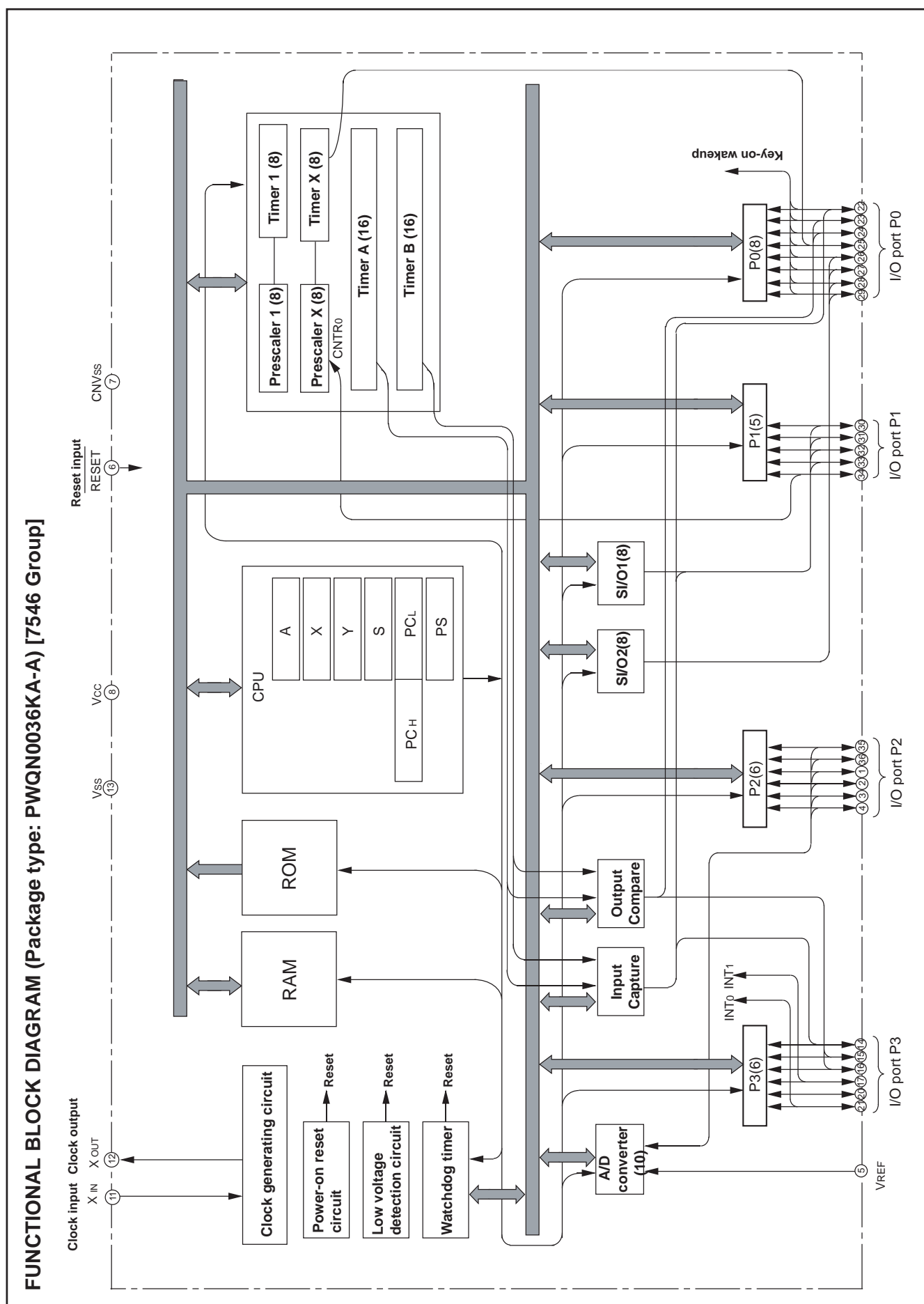


Fig. 5 Functional block diagram (Package type: PRDP0032BA-A)



PIN DESCRIPTION

Table 2 Pin description

| Pin | Name | Function | Function expect a port function | |
|---|--------------------------|--|--|--|
| Vcc, Vss | Power source | Apply voltage of 1.8 to 5.5 V to Vcc, and 0 V to Vss. | | |
| VREF | Analog reference voltage | •Reference voltage input pin for A/D converter. | | |
| CNVss | CNVss | •Chip operating mode control pin, which is always connected to Vss. | | |
| RESET | Reset input | •Reset input pin for active "L" | | |
| XIN | Clock input | •Input and output pins for main clock generating circuit. •Connect a ceramic resonator or quartz crystal oscillator between the XIN and XOUT pins. | | |
| XOUT | Clock output | •For using RC oscillator, short between the XIN and XOUT pins, and connect the capacitor and resistor. •If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. •When the on-chip oscillator is selected as the main clock, connect XIN pin to Vcc and leave XOUT open. | | |
| P00(LED00)/CAP0 P01(LED01)/CMP0 P02(LED02)/CMP1 P03(LED03)/TXOUT P04(LED04)/RxD2 P05(LED05)/TxD2 P06(LED06)/SCLK2 P07(LED07)/SRDY2 | I/O port P0 | •8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program. • High drive capacity for LED drive port can be selected by program. | • Capture function pin • Compare function pin • Timer X function pin • Serial I/O2 function pin | • Key-input (key-on wake up interrupt input) pin |
| P10/RxD1/CAP0 P11/TxD1 P12/SCLK1 P13/SRDY1 P14/CNTR0 | I/O port P1 | •5-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for P10, P12 and P13 | • Serial I/O1 function pin • Capture function pin • Serial I/O1 function pin • Timer X function pin | |
| P20/AN0–P25/AN5 | I/O port P2 | •6-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure | • Input pins for A/D converter | |
| P30(LED10)/CAP1 P31(LED11)/CMP2 P32(LED12)/CMP3 P33(LED13)/INT1 P34(LED14) P37(LED17)/INT0 | I/O port P3 | •6-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for P37). •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program. • High drive capacity for LED drive port can be selected by program. | • Capture function pin • Compare function pin • Interrupt input pin • Interrupt input pin | |

GROUP EXPANSION

Renesas plans to expand the 7546 Group as follow:

Memory type

Support for QzROM

Memory size

ROM size 8 K to 16 K bytes

RAM size 384 to 512 bytes

Package

PRDP0032BA-A 32-pin plastic molded SDIP

PLQP0032GB-A 0.8 mm-pitch 32-pin plastic molded LQFP

PWQN0036KA-A 0.5 mm-pitch 36-pin plastic molded WQFN

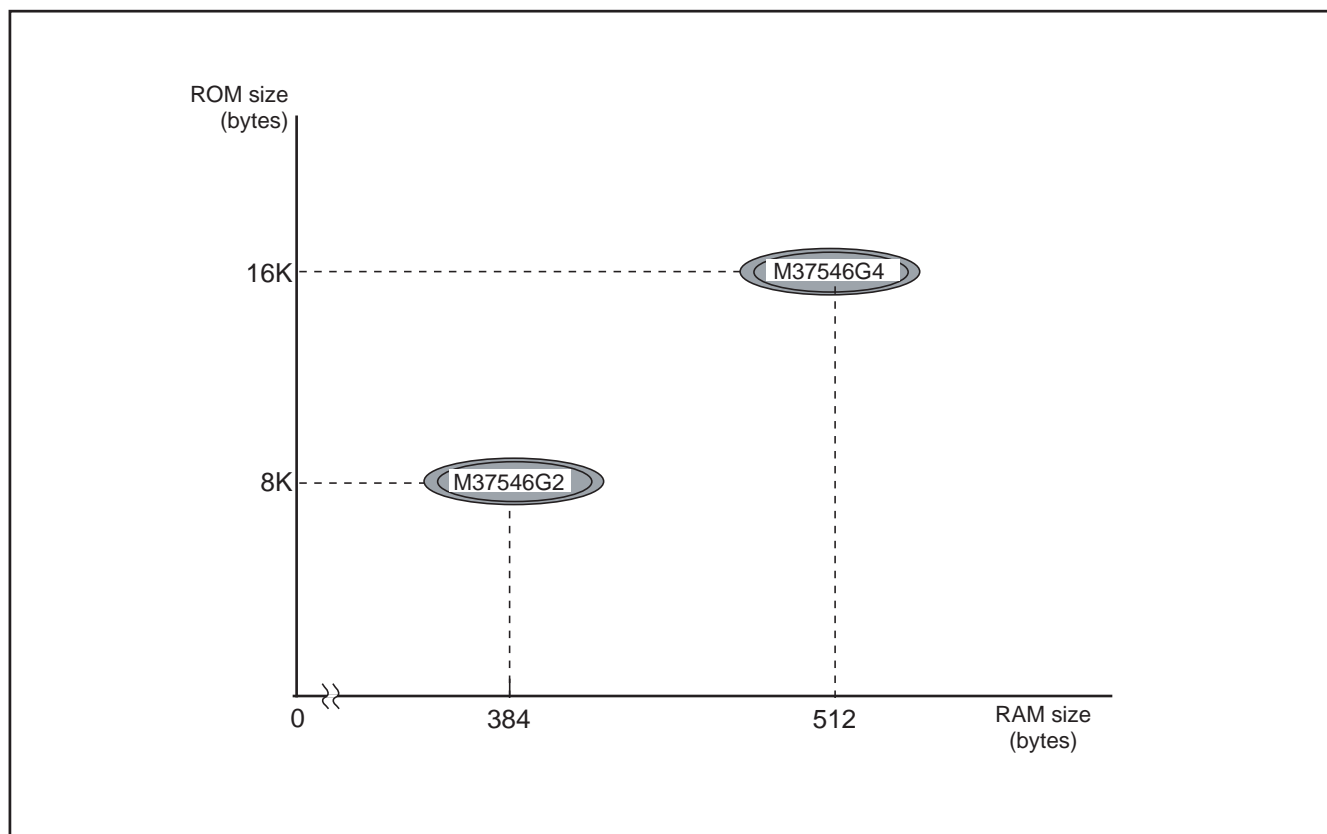


Fig. 7 Memory expansion plan

Currently supported products are listed below.

Table 3 List of supported products

| Product | ROM size (bytes) ROM size for User () | RAM size (bytes) | Package | Remarks |
|----------------|---|---------------------|--------------|-----------------------|
| M37546G2-XXXGP | 8192 (8062) | 384 | PLQP0032GB-A | Shipped after writing |
| M37546G2-XXXHP | | | PWQN0036KA-A | |
| M37546G2-XXXSP | | | PRDP0032BA-A | |
| M37546G2GP | | | PLQP0032GB-A | Shipped in blank |
| M37546G2HP | | | PWQN0036KA-A | |
| M37546G2SP | | | PRDP0032BA-A | |
| M37546G4-XXXGP | 16384 (16254) | 512 | PLQP0032GB-A | Shipped after writing |
| M37546G4-XXXHP | | | PWQN0036KA-A | |
| M37546G4-XXXSP | | | PRDP0032BA-A | |
| M37546G4GP | | | PLQP0032GB-A | Shipped in blank |
| M37546G4HP | | | PWQN0036KA-A | |
| M37546G4SP | | | PRDP0032BA-A | |

Note : ROM size includes the function set ROM.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The MCU uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the SERIES 740 <SOFTWARE> USER'S MANUAL for details on each instruction set.

Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions can be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

Accumulator (A)

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

Index register X (X), Index register Y (Y)

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.

When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

Stack pointer (S)

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.

The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.

The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed. The operations of pushing register contents onto the stack and popping them from the stack are shown in Fig. 9.

Program counter (PC)

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

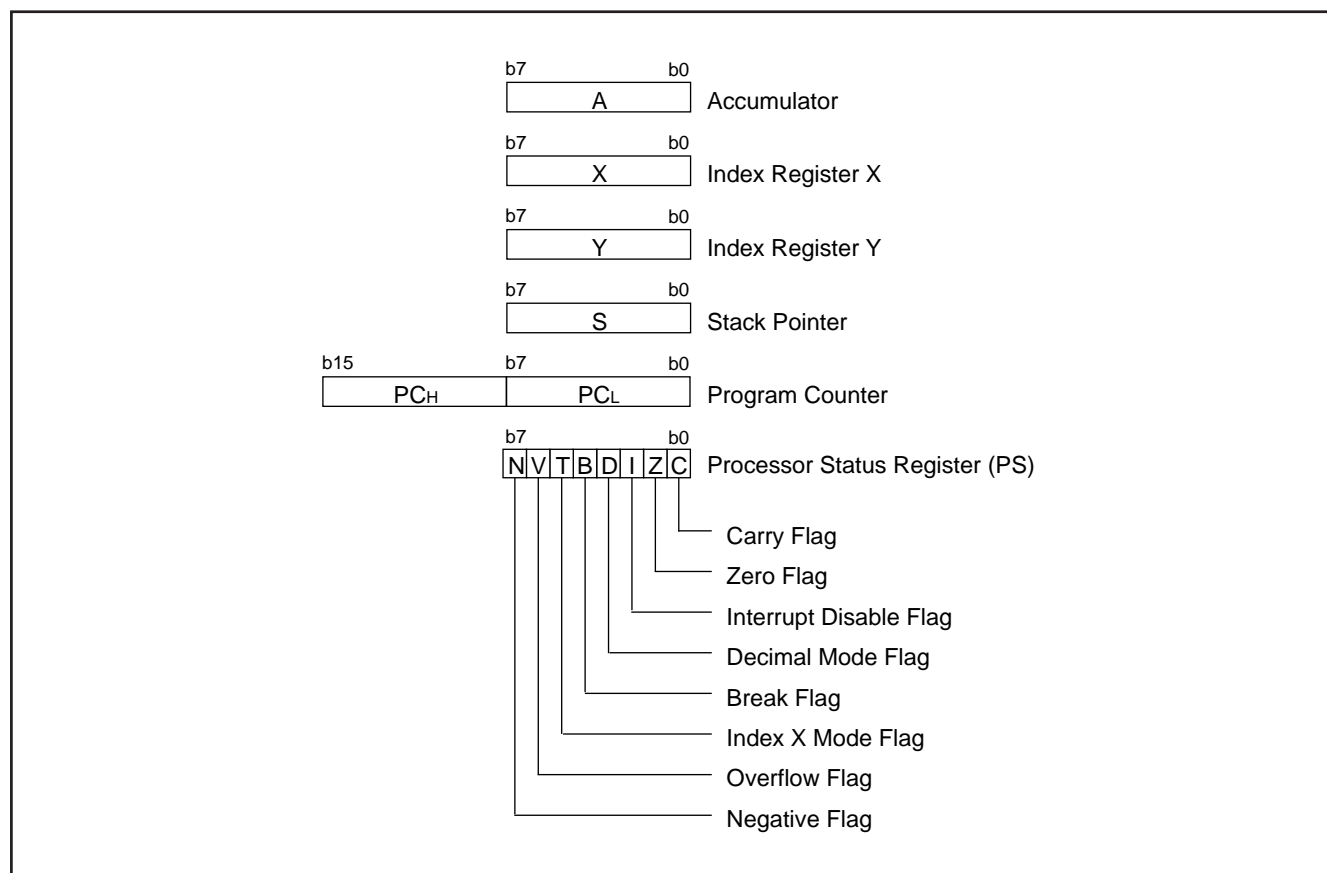


Fig. 8 740 Family CPU register structure

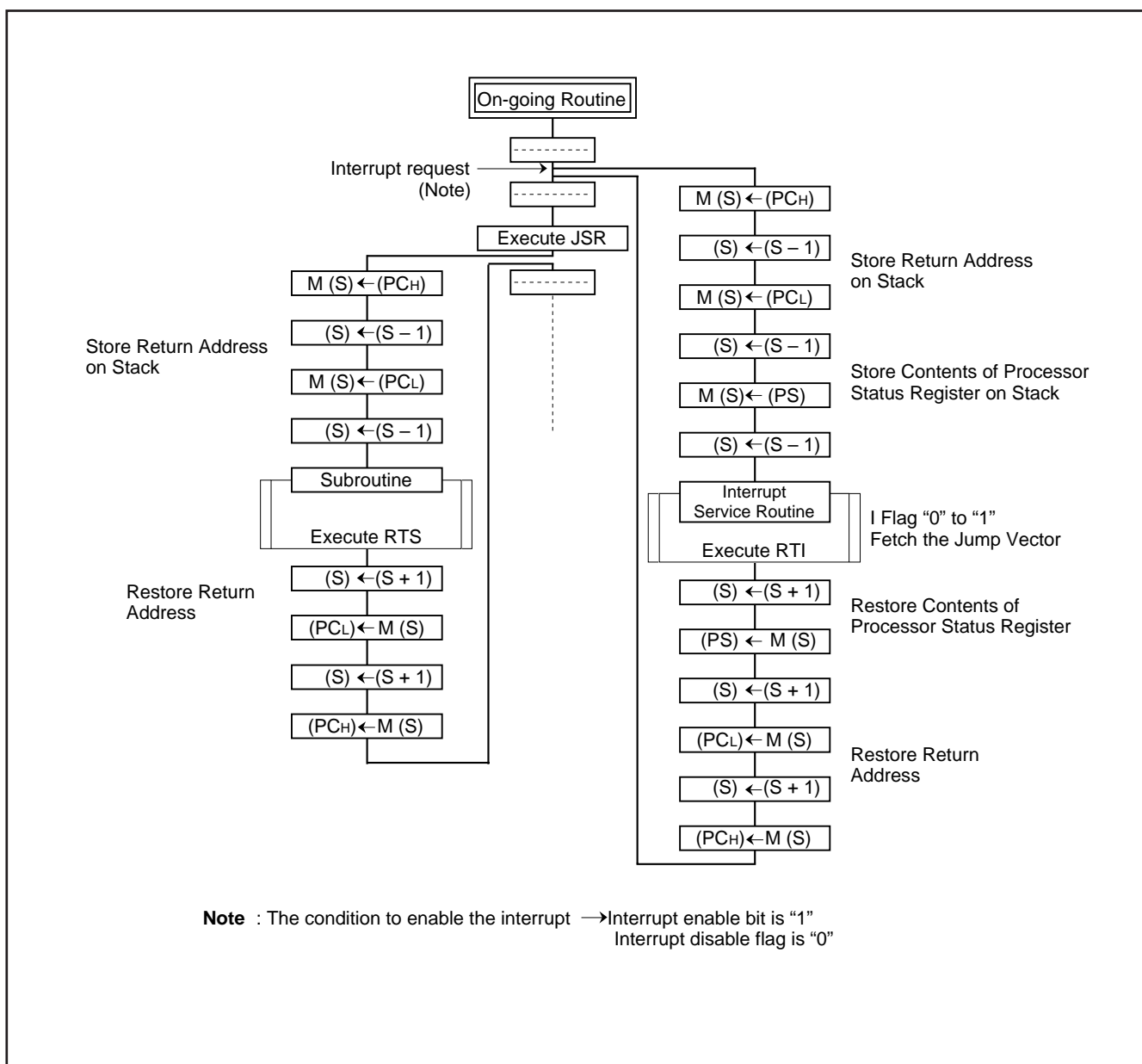


Fig. 9 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

| | Push instruction to stack | Pop instruction from stack |
|---------------------------|---------------------------|----------------------------|
| Accumulator | PHA | PLA |
| Processor status register | PHP | PLP |

Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

After reset, the Interrupt disable (I) flag is set to "1", but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

(1) Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

(2) Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

(3) Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1".

When an interrupt occurs, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is serviced.

(4) Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".

Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

(5) Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1". The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

(7) Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

(8) Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

| | C flag | Z flag | I flag | D flag | B flag | T flag | V flag | N flag |
|-------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| Set instruction | SEC | – | SEI | SED | – | SET | – | – |
| Clear instruction | CLC | – | CLI | CLD | – | CLT | CLV | – |

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

ROM Code Protect Address (address FFDB₁₆)

Address FFDB₁₆, which is the reserved ROM area of QzROM, is the ROM code protect address. "00₁₆" is written into this address when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp.. When "00₁₆" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.

As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.

As for the QzROM product shipped after writing, "00₁₆" (protect enabled) or "FF₁₆" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing. The writing of "00₁₆" or "FF₁₆" can be selected as the ROM option setup (referred to as "Mask option setup" in MM) when ordering.

■ Notes

Because the contents of RAM are indefinite at reset, set initial values before using.

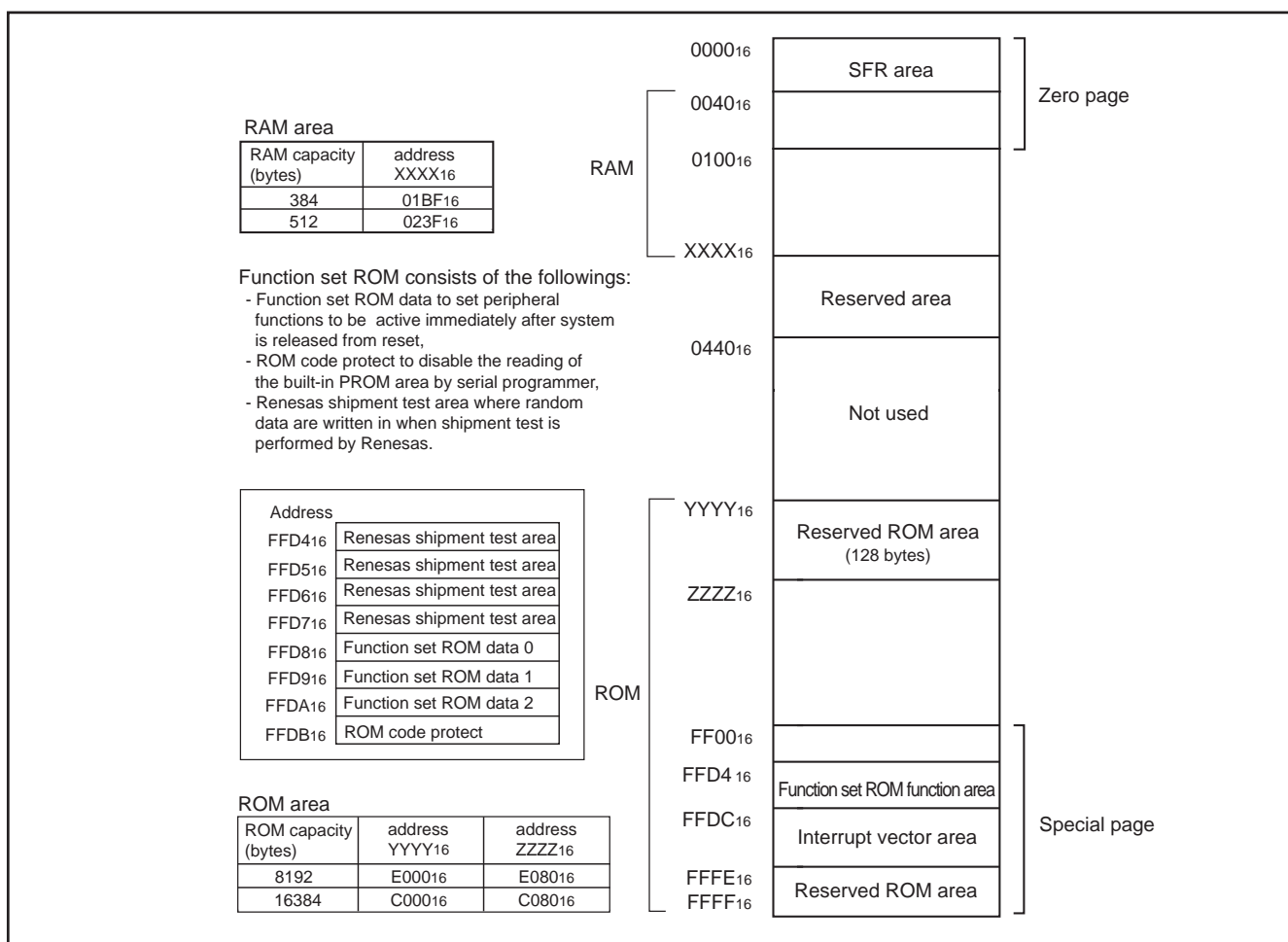


Fig. 10 Memory map diagram

[CPU mode register] CPUM

The CPU mode register contains the stack page selection bit, etc..
 This register is allocated at address 003B16.
 Some function of the CPU mode register can be controlled by the function set ROM data 2.

Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.

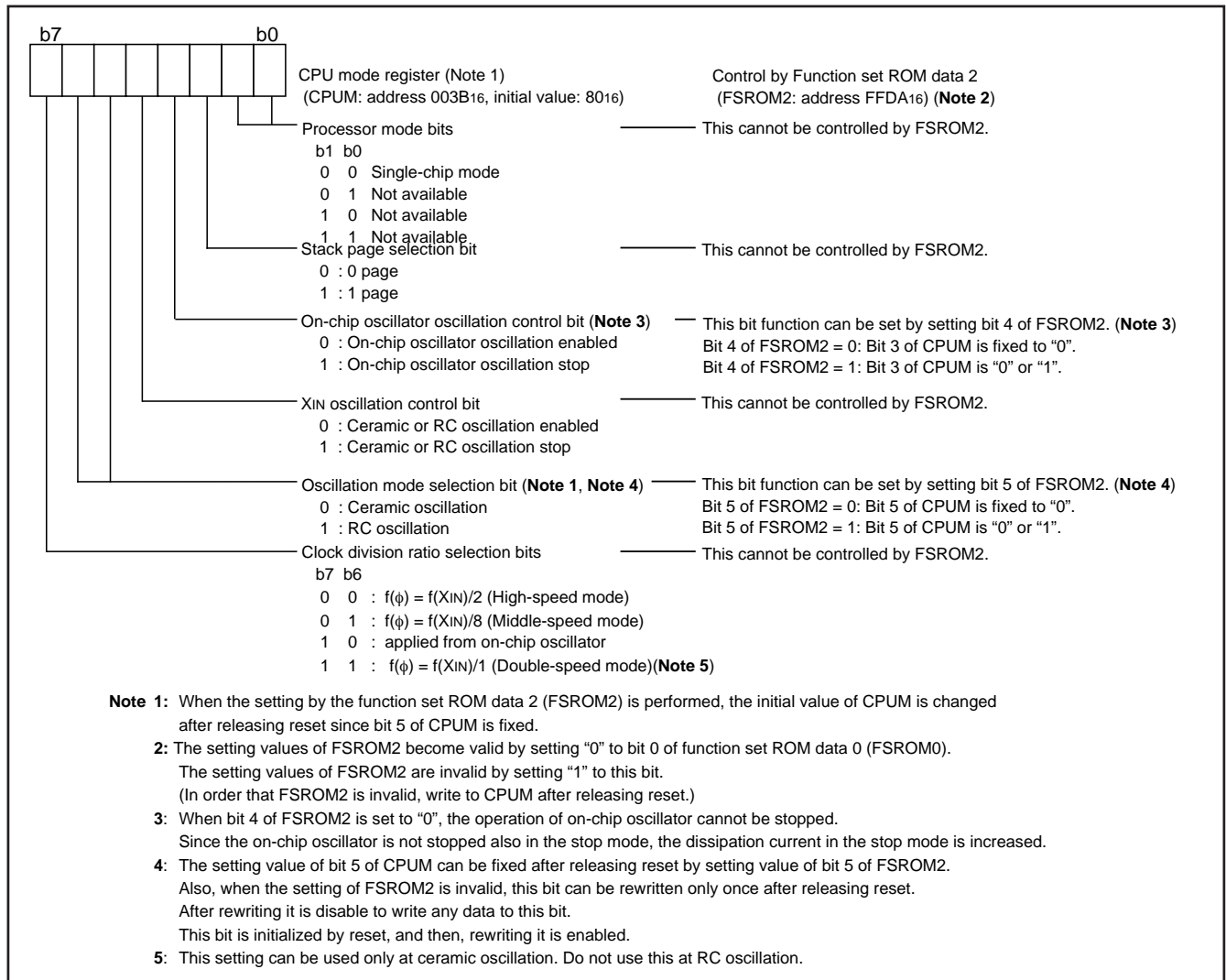


Fig. 11 Structure of CPU mode register

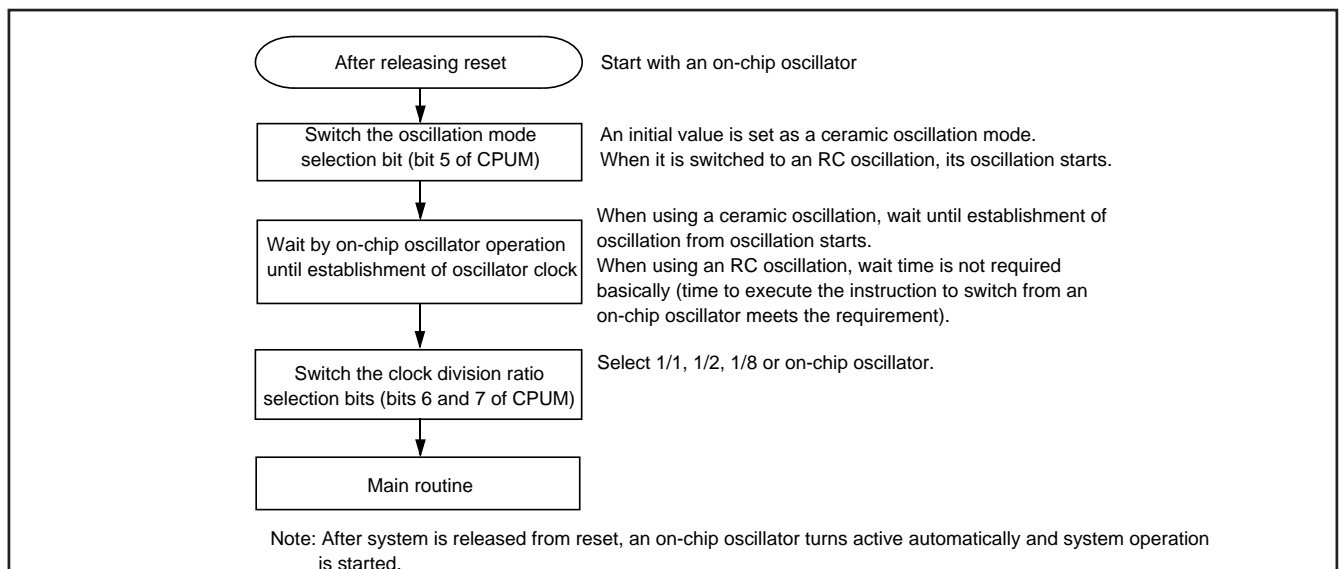


Fig. 12 Switching method of CPU mode register

| | | | |
|--------------------|---|--------------------|--|
| 0000 ₁₆ | Port P0 (P0) | 0020 ₁₆ | Capture mode register (CAPM) |
| 0001 ₁₆ | Port P0 direction register (P0D) | 0021 ₁₆ | Compare output mode register (CMOM) |
| 0002 ₁₆ | Port P1 (P1) | 0022 ₁₆ | Capture/compare status register (CCSR) |
| 0003 ₁₆ | Port P1 direction register (P1D) | 0023 ₁₆ | Compare interrupt source set register (CISR) |
| 0004 ₁₆ | Port P2 (P2) | 0024 ₁₆ | Timer A (low-order) (TAL) |
| 0005 ₁₆ | Port P2 direction register (P2D) | 0025 ₁₆ | Timer A (high-order) (TAH) |
| 0006 ₁₆ | Port P3 (P3) | 0026 ₁₆ | Timer B (low-order) (TBL) |
| 0007 ₁₆ | Port P3 direction register (P3D) | 0027 ₁₆ | Timer B (high-order) (TBH) |
| 0008 ₁₆ | Reserved | 0028 ₁₆ | Prescaler 1 (PRE1) |
| 0009 ₁₆ | Reserved | 0029 ₁₆ | Timer 1 (T1) |
| 000A ₁₆ | Interrupt source set register (INTSET) | 002A ₁₆ | Timer count source set register (TCSS) |
| 000B ₁₆ | Interrupt source discrimination register (INTDIS) | 002B ₁₆ | Timer X mode register (TXM) |
| 000C ₁₆ | Capture register 0 (low-order) (CAP0L) | 002C ₁₆ | Prescaler X (PREX) |
| 000D ₁₆ | Capture register 0 (high-order) (CAP0H) | 002D ₁₆ | Timer X (TX) |
| 000E ₁₆ | Capture register 1 (low-order) (CAP1L) | 002E ₁₆ | Transmit 2 / Receive 2 buffer register (TB2/RB2) |
| 000F ₁₆ | Capture register 1 (high-order) (CAP1H) | 002F ₁₆ | Serial I/O2 status register (SIO2STS) |
| 0010 ₁₆ | Compare register (low-order) (CMPL) | 0030 ₁₆ | Serial I/O2 control register (SIO2CON) |
| 0011 ₁₆ | Compare register (high-order) (CMPH) | 0031 ₁₆ | UART2 control register (UART2CON) |
| 0012 ₁₆ | Capture/compare register R/W pointer (CCRP) | 0032 ₁₆ | Baud rate generator 2 (BRG2) |
| 0013 ₁₆ | Capture software trigger register (CSTR) | 0033 ₁₆ | Reserved |
| 0014 ₁₆ | Compare register re-load register (CMPR) | 0034 ₁₆ | A/D control register (ADCON) |
| 0015 ₁₆ | Port POP3 drive capacity control register (DCCR) | 0035 ₁₆ | A/D conversion register (low-order) (ADL) |
| 0016 ₁₆ | Pull-up control register (PULL) | 0036 ₁₆ | A/D conversion register (high-order) (ADH) |
| 0017 ₁₆ | Port P1P3 control register (P1P3C) | 0037 ₁₆ | On-chip oscillation division ratio selection register (RODR) |
| 0018 ₁₆ | Transmit 1 /Receive 1 buffer register (TB1/RB1) | 0038 ₁₆ | MISRG |
| 0019 ₁₆ | Serial I/O1 status register (SIO1STS) | 0039 ₁₆ | Watchdog timer control register (WDTCN) |
| 001A ₁₆ | Serial I/O1 control register (SIO1CON) | 003A ₁₆ | Interrupt edge selection register (INTEDGE) |
| 001B ₁₆ | UART1 control register (UART1CON) | 003B ₁₆ | CPU mode register (CPUM) |
| 001C ₁₆ | Baud rate generator 1 (BRG1) | 003C ₁₆ | Interrupt request register 1 (IREQ1) |
| 001D ₁₆ | Timer A, B mode register (TABM) | 003D ₁₆ | Interrupt request register 2 (IREQ2) |
| 001E ₁₆ | Capture/compare port register (CCPR) | 003E ₁₆ | Interrupt control register 1 (ICON1) |
| 001F ₁₆ | Timer source selection register (TMSR) | 003F ₁₆ | Interrupt control register 2 (ICON2) |

Notes 1: Do not access to the SFR area including nothing.

Fig. 13 Memory map of special function register (SFR)

I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output. When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port.

When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

If a pin set to input is written to, only the port latch is written to and the pin remains floating.

- Set bits 6 and 7 of port P2 direction register to "1".
- Set bits 5 and 6 of port P3 direction register to "1".

[Port P0P3 drive capacity control register] DCCR

By setting the Port P0P3 drive capacity control register (address 001516), the drive capacity of the N-channel output transistor for the port P0 and port P3 can be selected.

[Pull-up control register] PULL

By setting the pull-up control register (address 001616), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

[Port P1P3 control register] P1P3C

By setting the port P1P3 control register (address 001716), a CMOS input level or a TTL input level can be selected for ports P10, P12, P13, and P37 by program.

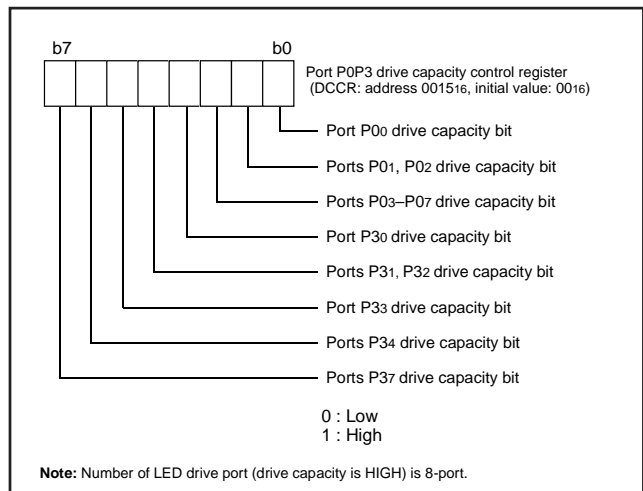


Fig. 14 Structure of port P0P3 drive capacity control register

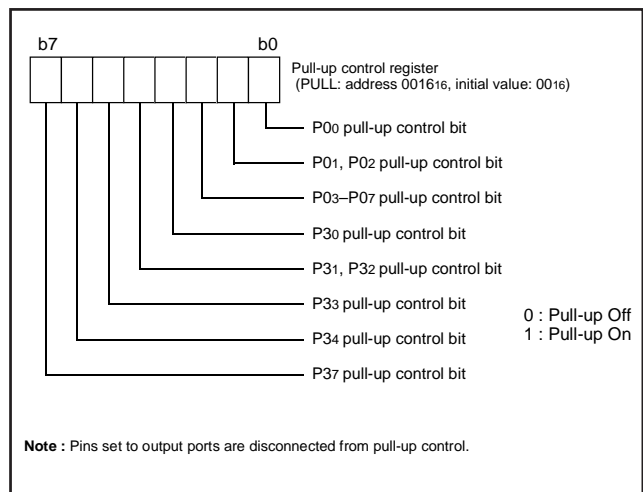


Fig. 15 Structure of pull-up control register

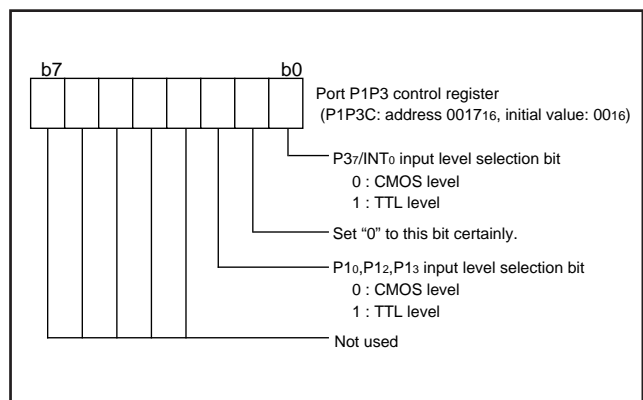


Fig. 16 Structure of port P1P3 control register

Table 6 I/O port function table

| Pin | Name | I/O format | Non-port function | SFRs related each pin | Diagram No. |
|------------------------------------|-------------|--|---|---|--------------|
| P00(LED00)/CAP0 | I/O port P0 | •CMOS compatible input level (Note 1) •CMOS 3-state output | • Capture function input • Key input interrupt | Capture/Compare port register Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register | (1) |
| P01(LED01)/CMP0 P02(LED02)/CMP1 | | | • Compare function output • Key input interrupt | Capture/Compare port register Pull-up control register Port P0P3 drive capacity control register | (2) |
| P03(LED03)/TXOUT | | | • Timer X function output • Key input interrupt | Timer X mode register Pull-up control register Port P0P3 drive capacity control register | (3) |
| P04(LED04)/RxD2 | | | • Serial I/O2 function input/output • Key input interrupt | Serial I/O2 control register Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register | (4) |
| P05(LED05)/TxD2 | | | | Serial I/O2 control register Pull-up control register Port P0P3 drive capacity control register | (5) |
| P06(LED06)/SCLK2 | | | | Serial I/O2 control register Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register | (6) |
| P07(LED07)/SRDY2 | | | | Serial I/O2 control register Pull-up control register Port P0P3 drive capacity control register | (7) |
| P10/RxD1/CAP0 | I/O port P1 | | • Serial I/O1 function input • Capture function input | Serial I/O1 control register Capture/Compare port register Port P1P3 control register | (8) |
| P11/TxD1 | | | • Serial I/O1 function input/output | Serial I/O1 control register | (9) |
| P12/SCLK1 | | | | Serial I/O1 control register Port P1P3 control register | (10) |
| P13/ $\overline{\text{SRDY1}}$ | | | | Serial I/O1 control register Port P1P3 control register | (11) |
| P14/CNTR0 | | | • Timer X function input/output • External interrupt input | Timer X mode register | (12) |
| P20/AN0–P25/AN5 | I/O port P2 | | • A/D conversion input | A/D control register | (13) |
| P30(LED10)/CAP1 | I/O port P3 | | • Capture function input | Capture/Compare port register Pull-up control register Port P0P3 drive capacity control register | (14) |
| P31(LED11)/CMP2 P32(LED12)/CMP3 | | | • Compare function output | Capture/Compare port register Pull-up control register Port P0P3 drive capacity control register | (15) |
| P33(LED13)/INT1 | | | • External interrupt input | Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register | (16) |
| P34(LED14) | | | | Pull-up control register Port P0P3 drive capacity control register | (17) |
| P37(LED17)/INT0 | | | • External interrupt input | Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register Port P1P3 control register | (18) (19) |

Notes 1: Ports P10, P12, P13, P37 are CMOS/TTL level.

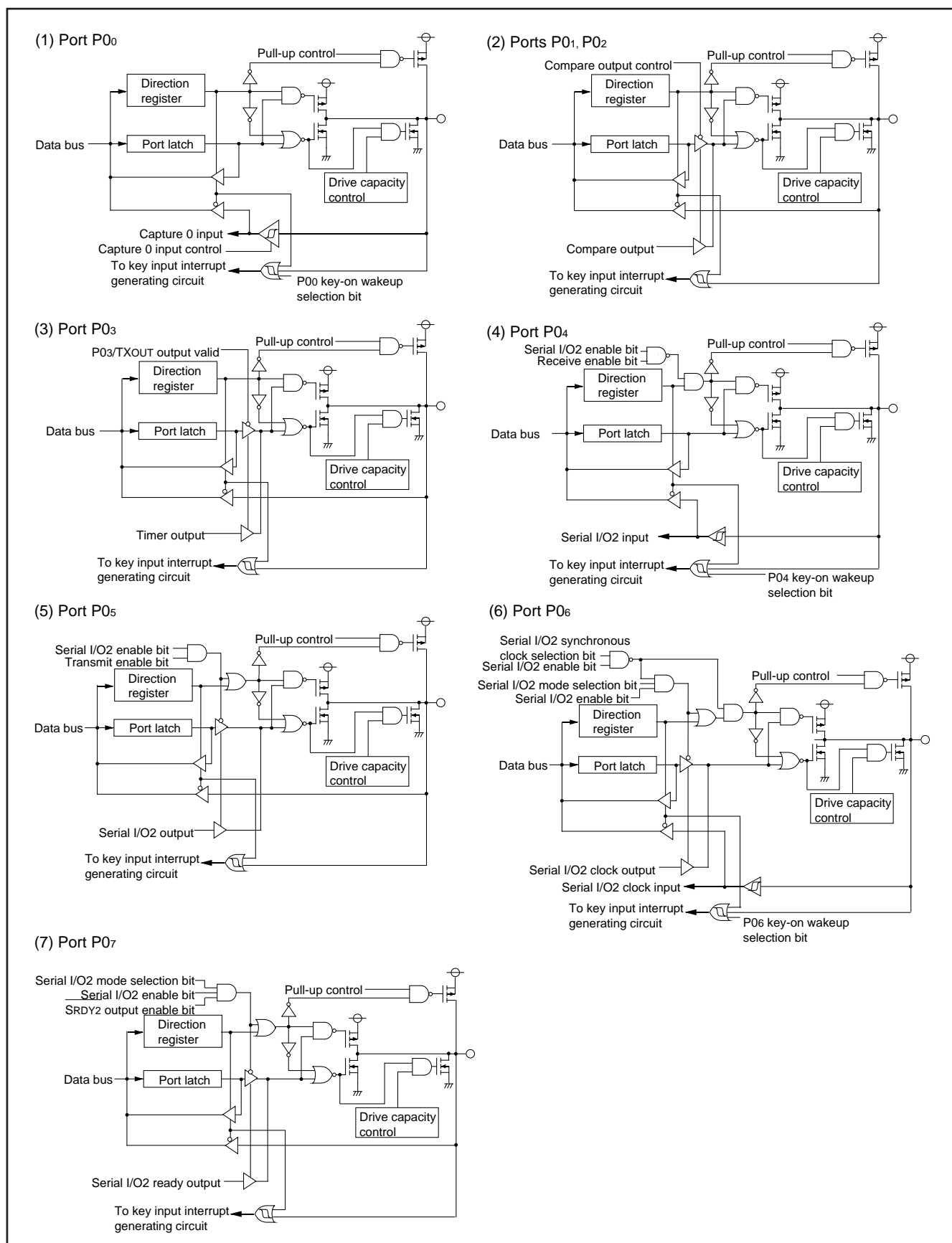
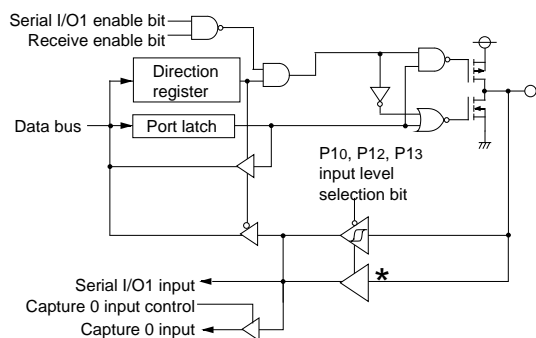
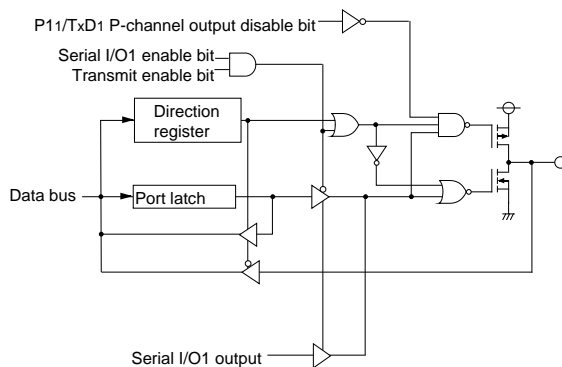


Fig. 17 Block diagram of ports (1)

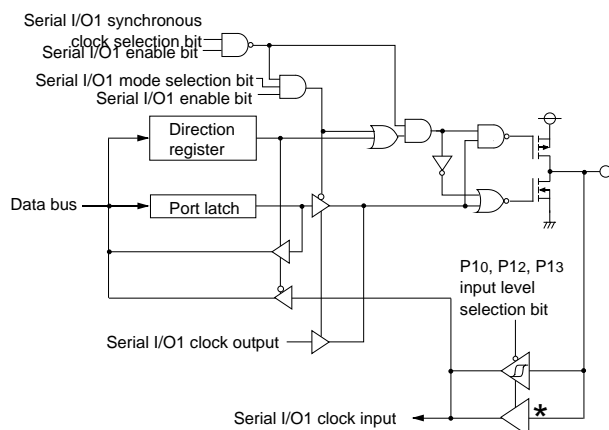
(8) Port P10



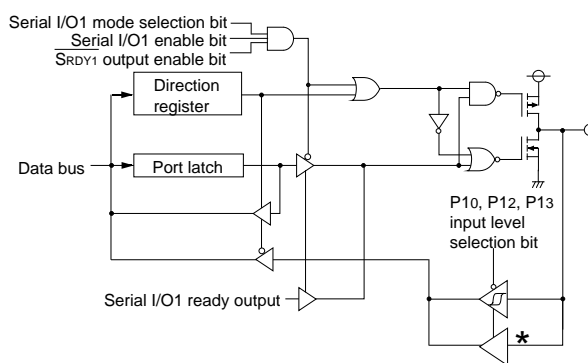
(9) Port P11



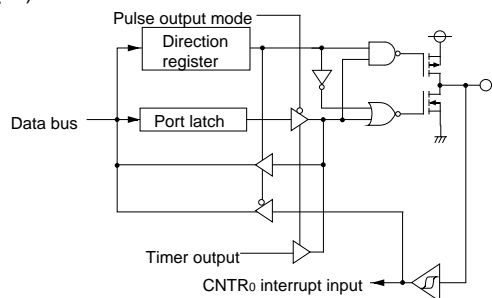
(10) Port P12



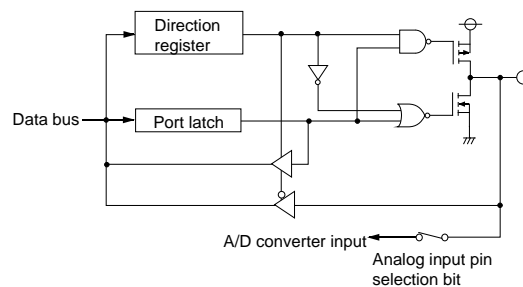
(11) Port P13



(12) Port P14

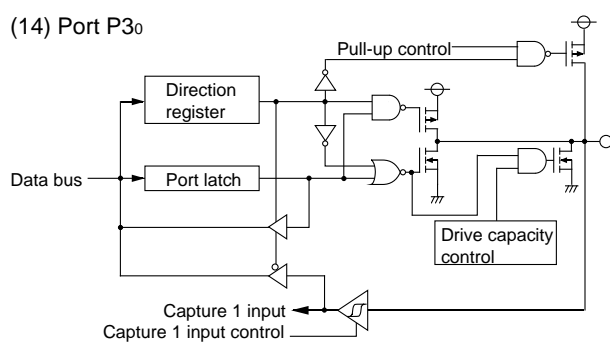
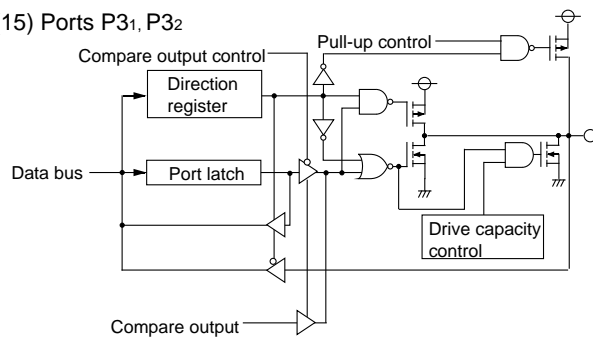
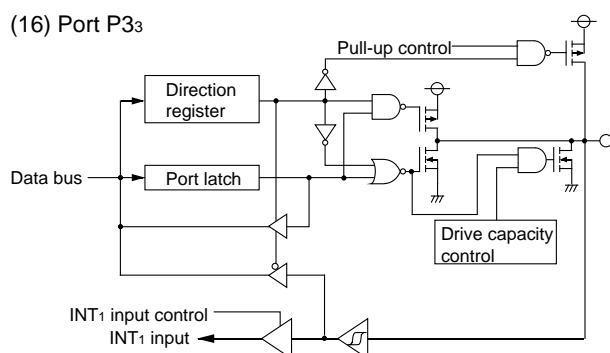
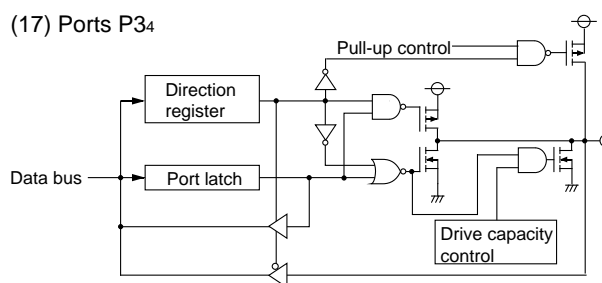
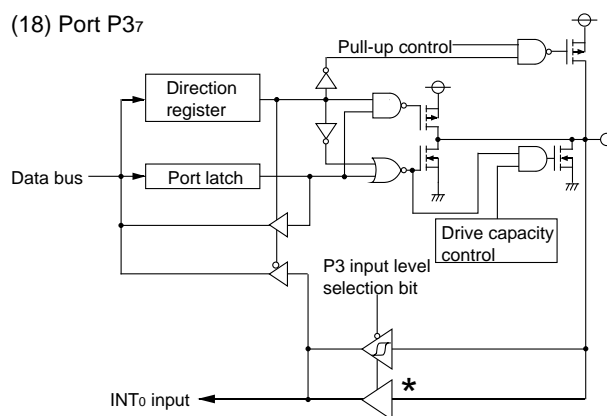


(13) Ports P20–P25



* P10, P12, P13, and P37 input level are switched to the CMOS/TTL level by the port P1P3 control register. When the TTL level is selected, there is no hysteresis characteristics.

Fig. 18 Block diagram of ports (2)

(14) Port P3₀(15) Ports P3₁, P3₂(16) Port P3₃(17) Ports P3₄(18) Port P3₇

★ P10, P12, P13, and P37 input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 19 Block diagram of ports (3)

Termination of unused pins

- Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.

Output ports: Open.

Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase. Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used).

We recommend processing unused pins through a resistor which can secure $I_{OH(avg)}$ or $I_{OL(avg)}$.

Because, when an I/O port or a pin which have an output function is selected as an input port, it may operate as an output port by incorrect operation etc.

Table 7 Termination of unused pins

| Pin | Termination 1 (recommend) | Termination 2 | Termination 3 | Termination 4 |
|-----------------|------------------------------|--|---|---|
| P00/CAP0 | I/O port | When selecting CAP function, perform termination of input port. | - | When selecting key-on wakeup function, perform termination of input port. |
| P01/CMP0 | | When selecting CMP0 function, perform termination of output port. | - | |
| P02/CMP1 | | When selecting CMP1 function, perform termination of output port. | - | |
| P03/TXOUT | | When selecting TXOUT function, perform termination of output port. | - | |
| P04/RxD2 | | When selecting RxD2 function, perform termination of input port. | - | |
| P05/TxD2 | | When selecting TxD2 function, perform termination of output port. | - | |
| P06/SCLK2 | | When selecting external clock input, perform termination of output port. | When selecting internal clock output, perform termination of output port. | |
| P07/SRDY2 | | When selecting SRDY2 function, perform termination of output port. | - | |
| P10/RxD1/CAP0 | | When selecting RxD1 function, perform termination of input port. | When selecting CAP function, perform termination of input port. | - |
| P11/TxD1 | | When selecting TxD1 function, perform termination of output port. | - | - |
| P12/SCLK1 | | When selecting external clock input, perform termination of input port. | When selecting internal clock output, perform termination of output port. | - |
| P13/SRDY1 | | When selecting SRDY1 function, perform termination of output port. | - | - |
| P14/CNTR0 | | When selecting CNTR input function, perform termination of input port. | When selecting CNTR output function, perform termination of output port. | - |
| P20/AN0–P25/AN5 | | When selecting AN function, perform termination of input port. | - | - |
| P30/CAP1 | Connect to Vss. | When selecting CAP function, perform termination of input port. | - | - |
| P31/CMP2 | | When selecting CMP2 function, perform termination of output port. | - | - |
| P32/CMP3 | | When selecting CMP3 function, perform termination of output port. | - | - |
| P33/INT1 | | When selecting INT function, perform termination of input port. | - | - |
| P34 | | - | - | - |
| P37/INT0 | | When selecting INT function, perform termination of input port. | - | - |
| VREF | | - | - | - |
| XIN | | - | - | - |
| XOUT | | - | - | - |
| | | - | - | - |

Interrupts

The 7546 Group interrupts are vector interrupts with a fixed priority scheme, and generated by 16 sources among 18 sources: 6 external, 11 internal, and 1 software.

The interrupt sources, vector addresses⁽¹⁾, and interrupt priority are shown in Table 8.

Each interrupt except the BRK instruction interrupt has the interrupt request bit and the interrupt enable bit. These bits and the interrupt disable flag (I flag) control the acceptance of interrupt requests. Fig. 20 shows an interrupt control diagram.

An interrupt request is accepted when all of the following conditions are satisfied:

- Interrupt disable flag.....“0”
- Interrupt request bit.....“1”
- Interrupt enable bit.....“1”

Though the interrupt priority is determined by hardware, priority processing can be performed by software using the above bits and flag.

Table 8 Interrupt vector addresses and priority

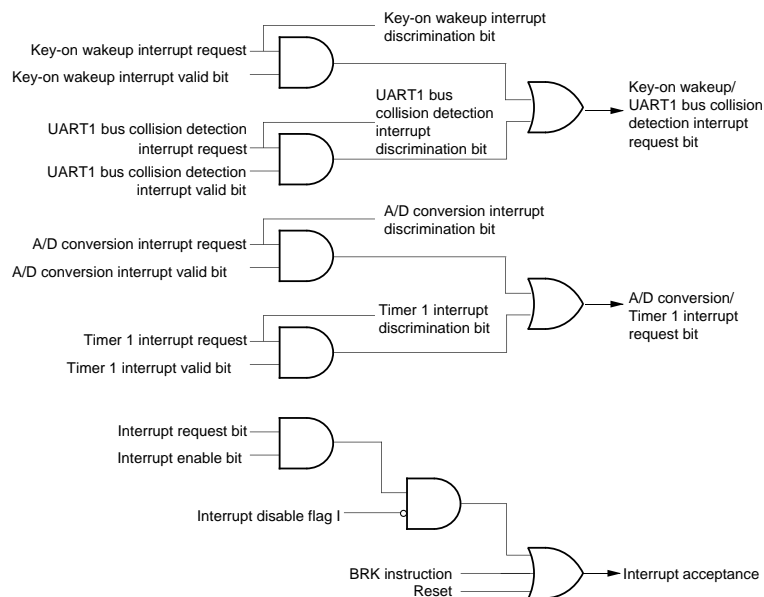
| Interrupt source | Priority | Vector addresses (Note 1) | | Interrupt request generating conditions | Remarks |
|---|----------|---------------------------|--------------------|--|--|
| | | High-order | Low-order | | |
| Reset (Note 2) | 1 | FFFD ₁₆ | FFFC ₁₆ | At reset input | Non-maskable |
| Serial I/O1 receive | 2 | FFFB ₁₆ | FFFA ₁₆ | At completion of serial I/O1 data receive | Valid only when serial I/O1 is selected |
| Serial I/O1 transmit | 3 | FFF9 ₁₆ | FFF8 ₁₆ | At completion of serial I/O1 transmit shift or when transmit buffer is empty | Valid only when serial I/O1 is selected |
| Serial I/O2 receive | 4 | FFF7 ₁₆ | FFF6 ₁₆ | At completion of serial I/O2 data receive | Valid only when serial I/O2 is selected |
| Serial I/O2 transmit | 5 | FFF5 ₁₆ | FFF4 ₁₆ | At completion of serial I/O2 transmit shift or when transmit buffer is empty | Valid only when serial I/O2 is selected |
| INT ₀ | 6 | FFF3 ₁₆ | FFF2 ₁₆ | At detection of either rising or falling edge of INT ₀ input | External interrupt (active edge selectable) |
| INT ₁ | 7 | FFF1 ₁₆ | FFF0 ₁₆ | At detection of either rising or falling edge of INT ₁ input | External interrupt (active edge selectable) |
| Key-on wake-up/ UART1 bus collision detection (Note 3) | 8 | FFEF ₁₆ | FFEE ₁₆ | At falling of conjunction of input logical level for port P0 (at input) At detection of UART1 bus collision detection | External interrupt (valid at falling edge) When UART1 bus collision detection interrupt is enabled. |
| CNTR ₀ | 9 | FFED ₁₆ | FFEC ₁₆ | At detection of either rising or falling edge of CNTR ₀ input | External interrupt (active edge selectable) |
| Capture 0 | 10 | FFEB ₁₆ | FFEA ₁₆ | At detection of either rising or falling edge of Capture 0 input | External interrupt (active edge selectable) |
| Capture 1 | 11 | FFE9 ₁₆ | FFE8 ₁₆ | At detection of either rising or falling edge of Capture 1 input | External interrupt (active edge selectable) |
| Compare | 12 | FFE7 ₁₆ | FFE6 ₁₆ | At compare matched | Compare interrupt source is selected. |
| Timer X | 13 | FFE5 ₁₆ | FFE4 ₁₆ | At timer X underflow | |
| Timer A | 14 | FFE3 ₁₆ | FFE2 ₁₆ | At timer A underflow | |
| Timer B | 15 | FFE1 ₁₆ | FFE0 ₁₆ | At timer B underflow | |
| A/D conversion/ Timer 1 (Note 4) | 16 | FFDF ₁₆ | FFDE ₁₆ | At completion of A/D conversion At timer 1 underflow | STP release timer underflow |
| BRK instruction | 17 | FFDD ₁₆ | FFDC ₁₆ | At BRK instruction execution | Non-maskable software interrupt |

Notes1: Vector addresses contain internal jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

3: Key-on wakeup interrupt and UART1 bus collision detection interrupt can be enabled by setting of interrupt source set register. The occurrence of these interrupts are discriminated by interrupt source discrimination register.

4: A/D conversion interrupt and Timer 1 interrupt can be enabled by setting of interrupt source set register. The occurrence of these interrupts are discriminated by interrupt source discrimination register.



Note: For key-on wakeup, UART1 bus collision detection, A/D conversion and Timer 1 interrupt, even if interrupt valid bit (000A16) is set "0: Invalid", interrupt discrimination bit (000B16) is set to "1: interrupt occurs" when corresponding interrupt request occurs. But corresponding interrupt request bit (003C16, 003D16) is not set to "1".

Fig. 20 Interrupt control

• Interrupt Disable Flag

The interrupt disable flag is assigned to bit 2 of the processor status register. This flag controls the acceptance of all interrupt requests except for the BRK instruction. When this flag is set to "1", the acceptance of interrupt requests is disabled. When it is set to "0", the acceptance of interrupt requests is enabled. This flag is set to "1" with the SEI instruction and set to "0" with the CLI instruction.

When an interrupt request is accepted, the contents of the processor status register are pushed onto the stack while the interrupt disable flag remains set to "0". Subsequently, this flag is automatically set to "1" and multiple interrupts are disabled.

To use multiple interrupts, set this flag to "0" with the CLI instruction within the interrupt processing routine.

The contents of the processor status register are popped off the stack with the RTI instruction.

• Interrupt Request Bits

Once an interrupt request is generated, the corresponding interrupt request bit is set to "1" and remains "1" until the request is accepted. When the request is accepted, this bit is automatically set to "0".

Each interrupt request bit can be set to "0", but cannot be set to "1", by software.

• Interrupt Enable Bits

The interrupt enable bits control the acceptance of the corresponding interrupt requests. When an interrupt enable bit is set to "0", the acceptance of the corresponding interrupt request is disabled. If an interrupt request occurs in this condition, the corresponding interrupt request bit is set to "1", but the interrupt request is not accepted. When an interrupt enable bit is set to "1", the acceptance of the corresponding interrupt request is enabled. Each interrupt enable bit can be set to "0" or "1" by software. The interrupt enable bit for an unused interrupt should be set to "0".

• Interrupt Enable Setting

The following interrupt sources can be set to valid or invalid by the interrupt source set register (000A16).

- Key-on wakeup
- UART1 bus collision detection interrupt
- A/D conversion
- Timer 1 interrupt

• Interrupt edge selection

The valid edge of external interrupt INT0 and INT1 can be selected by the interrupt edge selection bit of the interrupt edge selection register (003A16), respectively.

Set bit 2 of interrupt edge selection register to "1".

• Key-on wakeup

Enable/disable of a key-on wakeup of pins P00, P04, and P06 can be selected by the key-on wakeup enable bit of the interrupt edge selection register (003A16), respectively.

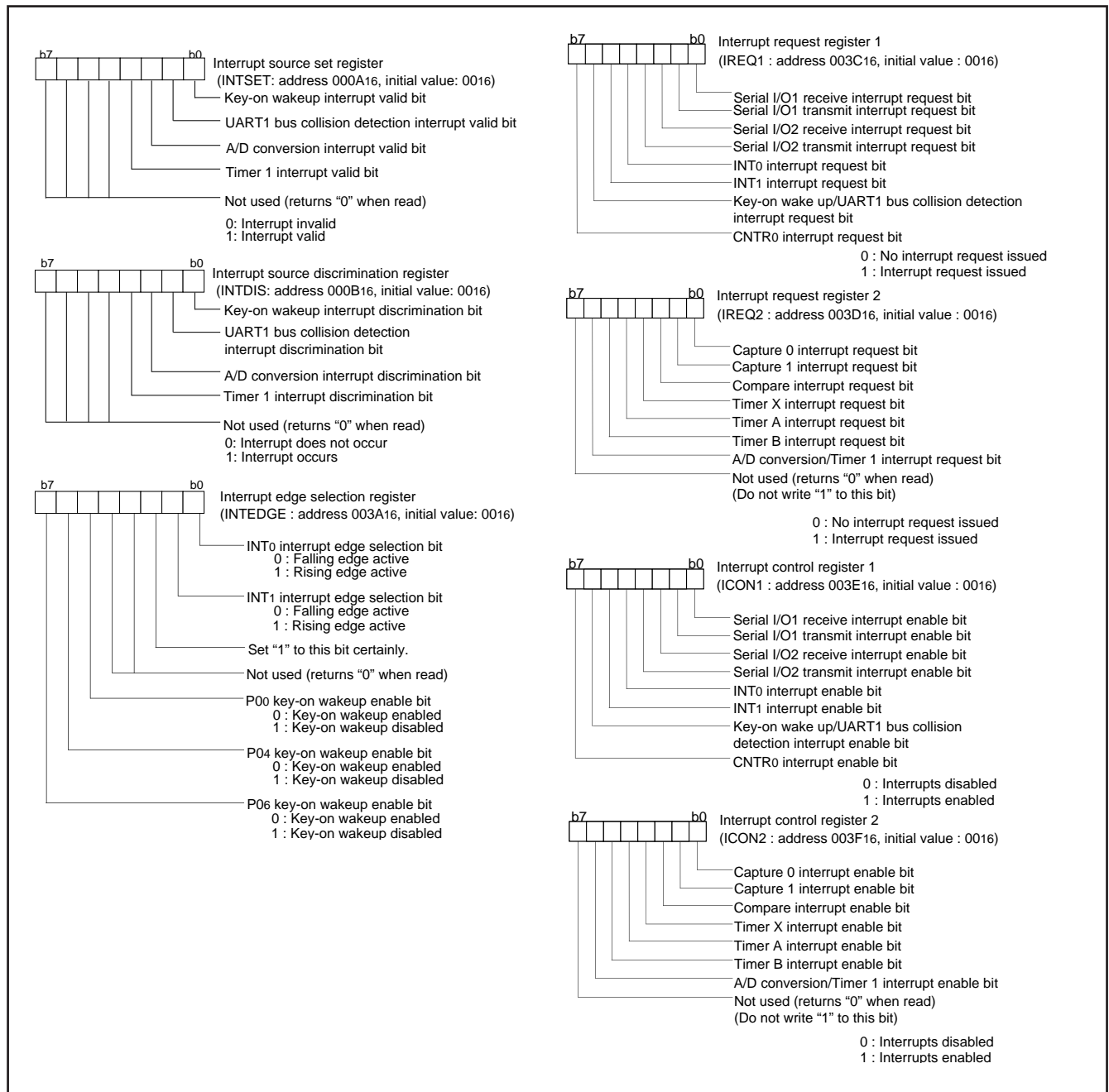


Fig. 21 Structure of Interrupt-related registers

• Interrupt Request Generation, Acceptance, and Handling

Interrupts have the following three phases.

(i) Interrupt Request Generation

An interrupt request is generated by an interrupt source (external interrupt signal input, timer underflow, etc.) and the corresponding request bit is set to "1".

(ii) Interrupt Request Acceptance

Based on the interrupt acceptance timing in each instruction cycle, the interrupt control circuit determines acceptance conditions (interrupt request bit, interrupt enable bit, and interrupt disable flag) and interrupt priority levels for accepting interrupt requests. When two or more interrupt requests are generated simultaneously, the highest priority interrupt is accepted. The value of the interrupt request bit for an unaccepted interrupt remains the same and acceptance is determined at the next interrupt acceptance timing point.

(iii) Handling of Accepted Interrupt Request

The accepted interrupt request is processed.

Fig. 22 shows the time up to execution in the interrupt processing routine, and Fig. 23 shows the interrupt sequence.

Fig. 24 shows the timing of interrupt request generation, interrupt request bit, and interrupt request acceptance.

• Interrupt Handling Execution

When interrupt handling is executed, the following operations are performed automatically.

- (1) Once the currently executing instruction is completed, an interrupt request is accepted.
- (2) The contents of the program counters and the processor status register at this point are pushed onto the stack area in order from 1 to 3.
 - 1.High-order bits of program counter (PCH)
 - 2.Low-order bits of program counter (PCL)
 - 3.Processor status register (PS)
- (3) Concurrently with the push operation, the jump address of the corresponding interrupt (the start address of the interrupt processing routine) is transferred from the interrupt vector to the program counter.
- (4) The interrupt request bit for the corresponding interrupt is set to "0". Also, the interrupt disable flag is set to "1" and multiple interrupts are disabled.
- (5) The interrupt routine is executed.
- (6) When the RTI instruction is executed, the contents of the registers pushed onto the stack area are popped off in the order from 3 to 1. Then, the routine that was before running interrupt processing resumes.

As described above, it is necessary to set the stack pointer and the jump address in the vector area corresponding to each interrupt to execute the interrupt processing routine.

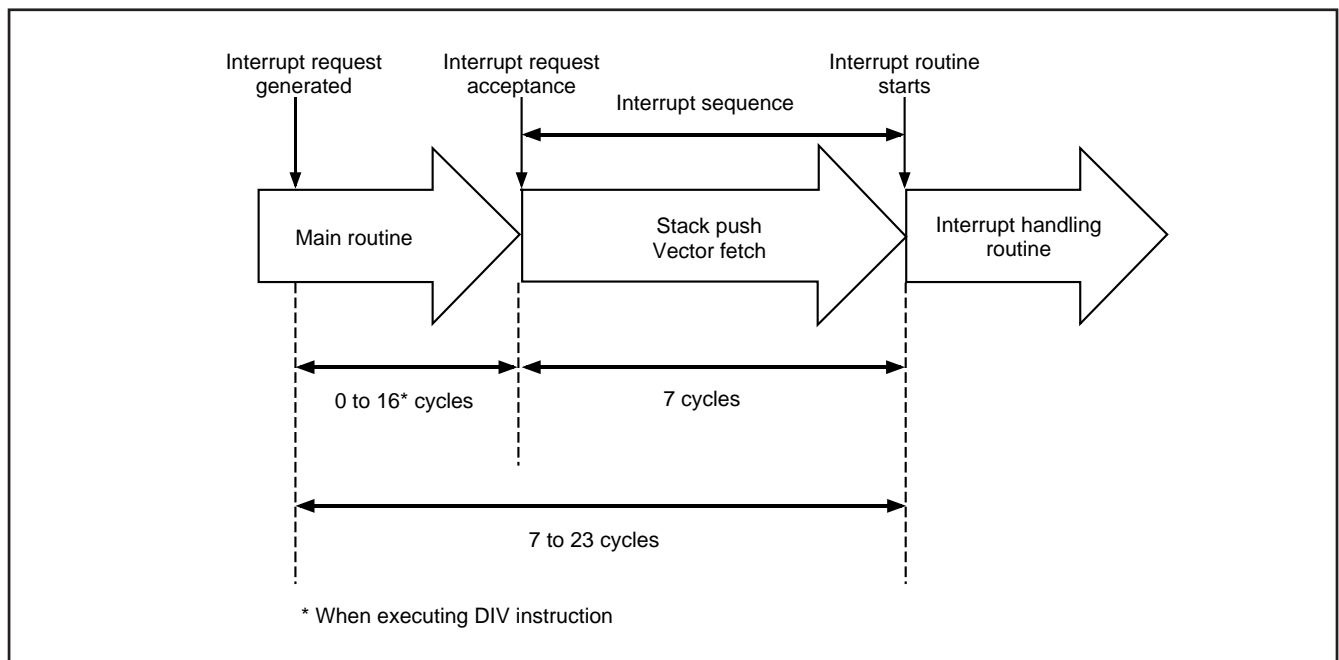


Fig. 22 Time up to execution in interrupt routine

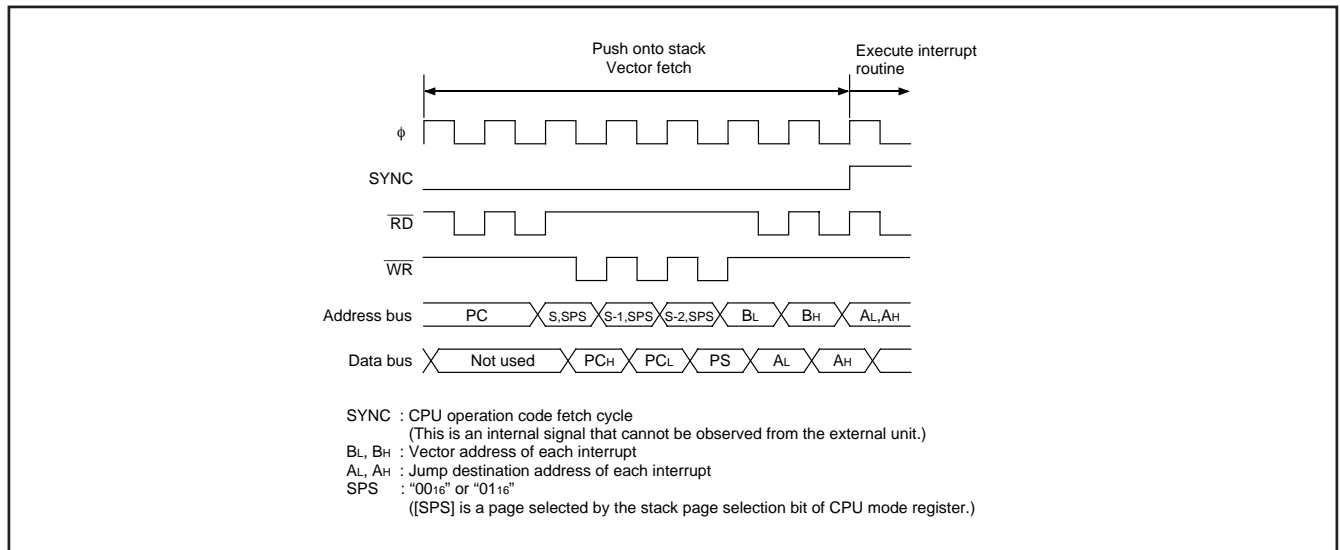


Fig. 23 Interrupt sequence

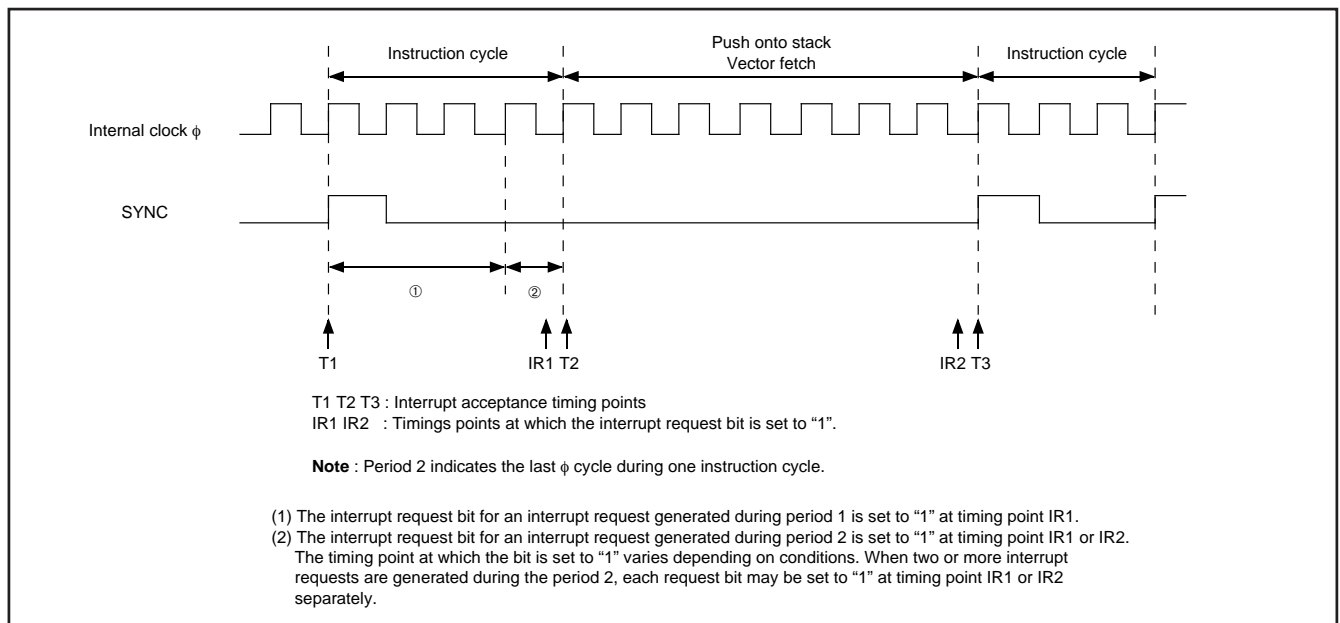


Fig. 24 Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

■ Notes on Interrupts

When setting the followings, the interrupt request bit may be set to "1".

<When switching external interrupt active edge>

- INT0 interrupt edge selection bit
(bit 0 of Interrupt edge selection register (address 3A₁₆))
- INT1 interrupt edge selection bit
(bit 1 of Interrupt edge selection register)
- CNTR0 active edge switch bit
(bit 2 of timer X mode register (address 2B₁₆))
- Capture 0 interrupt edge selection bit
(bits 1 and 0 of capture mode register (address 20₁₆))
- Capture 1 interrupt edge selection bit
(bits 3 and 2 of capture mode register)

If it is not necessary to generate an interrupt synchronized with these settings, take the following sequence.

- (1) Set the corresponding enable bit to "0" (disabled).
- (2) Set the interrupt edge selection bit (the active edge switch bit) or the interrupt source bit.
- (3) Set the corresponding interrupt request bit to "0" after one or more instructions have been executed.
- (4) Set the corresponding interrupt enable bit to "1" (enabled).

Timers

The 7546 Group has 4 timers: timer 1, timer X, timer A and timer B.

The division ratio of every timer and prescaler is $1/(n+1)$ provided that the value of the timer latch or prescaler is n .

All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

• Frequency divider for timer

According to the clock division selection bits (b7 and b6) of CPU mode register (003B16), the count source of frequency divider is set as follows;

b7b6 = "00"(high-speed), "01"(middle-speed), "11"(double-speed): XIN

b7b6 = "10"(On-chip oscillator): On-chip oscillator

●Timer 1

Timer 1 is an 8-bit timer and counts the prescaler output.

When Timer 1 underflows, the timer 1 interrupt request bit is set to "1".

Prescaler 1 is an 8-bit prescaler and counts the signal which is the oscillation frequency divided by 16.

Prescaler 1 and Timer 1 have the prescaler 1 latch and the timer 1 latch to retain the reload value, respectively. The value of prescaler 1 latch is set to Prescaler 1 when Prescaler 1 underflows. The value of timer 1 latch is set to Timer 1 when Timer 1 underflows.

When writing to Prescaler 1 (PRE1) is executed, the value is written to both the prescaler 1 latch and Prescaler 1.

When writing to Timer 1 (T1) is executed, the value is written to both the timer 1 latch and Timer 1.

When reading from Prescaler 1 (PRE1) and Timer 1 (T1) is executed, each count value is read out.

Timer 1 always operates in the timer mode.

Prescaler 1 counts the signal which is the oscillation frequency divided by 16. Each time the count clock is input, the contents of Prescaler 1 is decremented by 1. When the contents of Prescaler 1 reach "0016", an underflow occurs at the next count clock, and the prescaler 1 latch is reloaded into Prescaler 1 and count continues. The division ratio of Prescaler 1 is $1/(n+1)$ provided that the value of Prescaler 1 is n .

The contents of Timer 1 is decremented by 1 each time the underflow signal of Prescaler 1 is input. When the contents of Timer 1 reach "0016", an underflow occurs at the next count clock, and the timer 1 latch is reloaded into Timer 1 and count continues. The division ratio of Timer 1 is $1/(m+1)$ provided that the value of Timer 1 is m . Accordingly, the division ratio of Prescaler 1 and Timer 1 is $1/((n+1) \times (m+1))$ provided that the value of Prescaler 1 is n and the value of Timer 1 is m .

Timer 1 cannot stop counting by software.

●Timer X

Timer X is an 8-bit timer and counts the prescaler X output.

When Timer X underflows, the timer X interrupt request bit is set to "1".

Prescaler X is an 8-bit prescaler and counts the signal selected by the timer X count source selection bit.

Prescaler X and Timer X have the prescaler X latch and the timer X latch to retain the reload value, respectively. The value of prescaler X latch is set to Prescaler X when Prescaler X underflows. The value of timer X latch is set to Timer X when Timer X underflows.

When writing to Prescaler X (PREX) is executed, the value is written to both the prescaler X latch and Prescaler X.

When writing to Timer X (TX) is executed, the value is written to both the timer X latch and Timer X.

When reading from Prescaler X (PREX) and Timer X (TX) is executed, each count value is read out.

Timer X can be selected in one of 4 operating modes by setting the timer X operating mode bits of the timer X mode register.

(1) Timer mode

Prescaler X counts the count source selected by the timer X count source selection bits. Each time the count clock is input, the contents of Prescaler X is decremented by 1. When the contents of Prescaler X reach "0016", an underflow occurs at the next count clock, and the prescaler X latch is reloaded into Prescaler X and count continues. The division ratio of Prescaler X is $1/(n+1)$ provided that the value of Prescaler X is n .

The contents of Timer X is decremented by 1 each time the underflow signal of Prescaler X is input. When the contents of Timer X reach "0016", an underflow occurs at the next count clock, and the timer X latch is reloaded into Timer X and count continues. The division ratio of Timer X is $1/(m+1)$ provided that the value of Timer X is m . Accordingly, the division ratio of Prescaler X and Timer X is $1/((n+1) \times (m+1))$ provided that the value of Prescaler X is n and the value of Timer X is m .

(2) Pulse output mode

In the pulse output mode, the waveform whose polarity is inverted each time timer X underflows is output from the CNTR0 pin.

The output level of CNTR0 pin can be selected by the CNTR0 active edge switch bit. When the CNTR0 active edge switch bit is "0", the output of CNTR0 pin is started at "H" level. When this bit is "1", the output is started at "L" level.

Also, the inverted waveform of pulse output from CNTR0 pin can be output from TXOUT pin by setting "1" to the P03/TXOUT output valid bit.

When using a timer in this mode, set the port P14 and P03 direction registers to output mode.

(3) Event counter mode

The timer A counts signals input from the P14/CNTR0 pin.

Except for this, the operation in event counter mode is the same as in timer mode.

The active edge of CNTR0 pin input signal can be selected from rising or falling by the CNTR0 active edge switch bit.

(4) Pulse width measurement mode

In the pulse width measurement mode, the pulse width of the signal input to P14/CNTR0 pin is measured.

The operation of Timer X can be controlled by the level of the signal input from the CNTR0 pin.

When the CNTR0 active edge switch bit is “0”, the signal selected by the timer X count source selection bit is counted while the input signal level of CNTR0 pin is “H”. The count is stopped while the pin is “L”. Also, when the CNTR0 active edge switch bit is “1”, the signal selected by the timer X count source selection bit is counted while the input signal level of CNTR0 pin is “L”. The count is stopped while the pin is “H”.

Timer X can stop counting by setting “1” to the timer X count stop bit in any mode.

Also, when Timer X underflows, the timer X interrupt request bit is set to “1”.

Note on Timer X is described below:

■ Note on Timer X

(1) CNTR0 interrupt active edge selection-1

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

When this bit is “0”, the CNTR0 interrupt request bit is set to “1” at the falling edge of CNTR0 pin input signal. When this bit is “1”, the CNTR0 interrupt request bit is set to “1” at the rising edge of CNTR0 pin input signal.

(2) CNTR0 interrupt active edge selection-2

According to the setting value of CNTR0 active edge switch bit, the interrupt request bit may be set to "1".

When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- ① Set the corresponding interrupt enable bit to "0" (disabled).
- ② Set the active edge switch bit.
- ③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④ Set the corresponding interrupt enable bit to "1" (enabled).

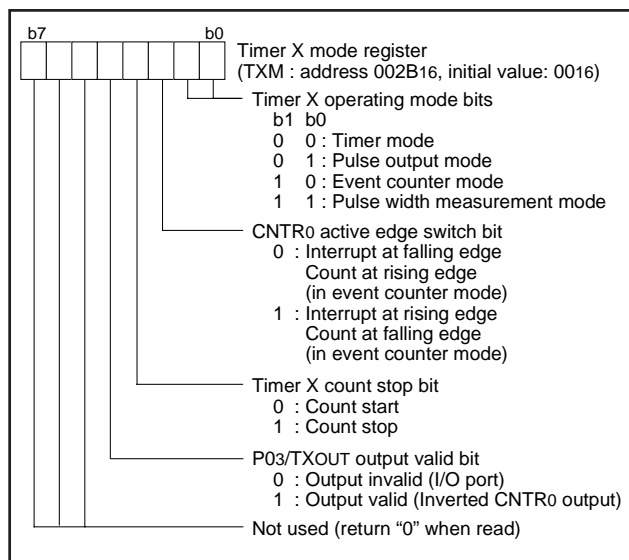


Fig. 26 Structure of timer X mode register

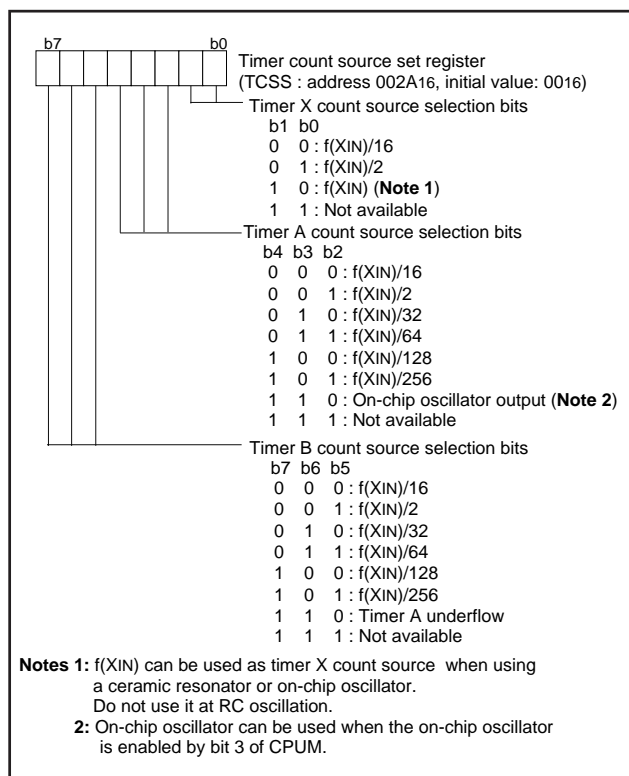


Fig. 27 Timer count source set register

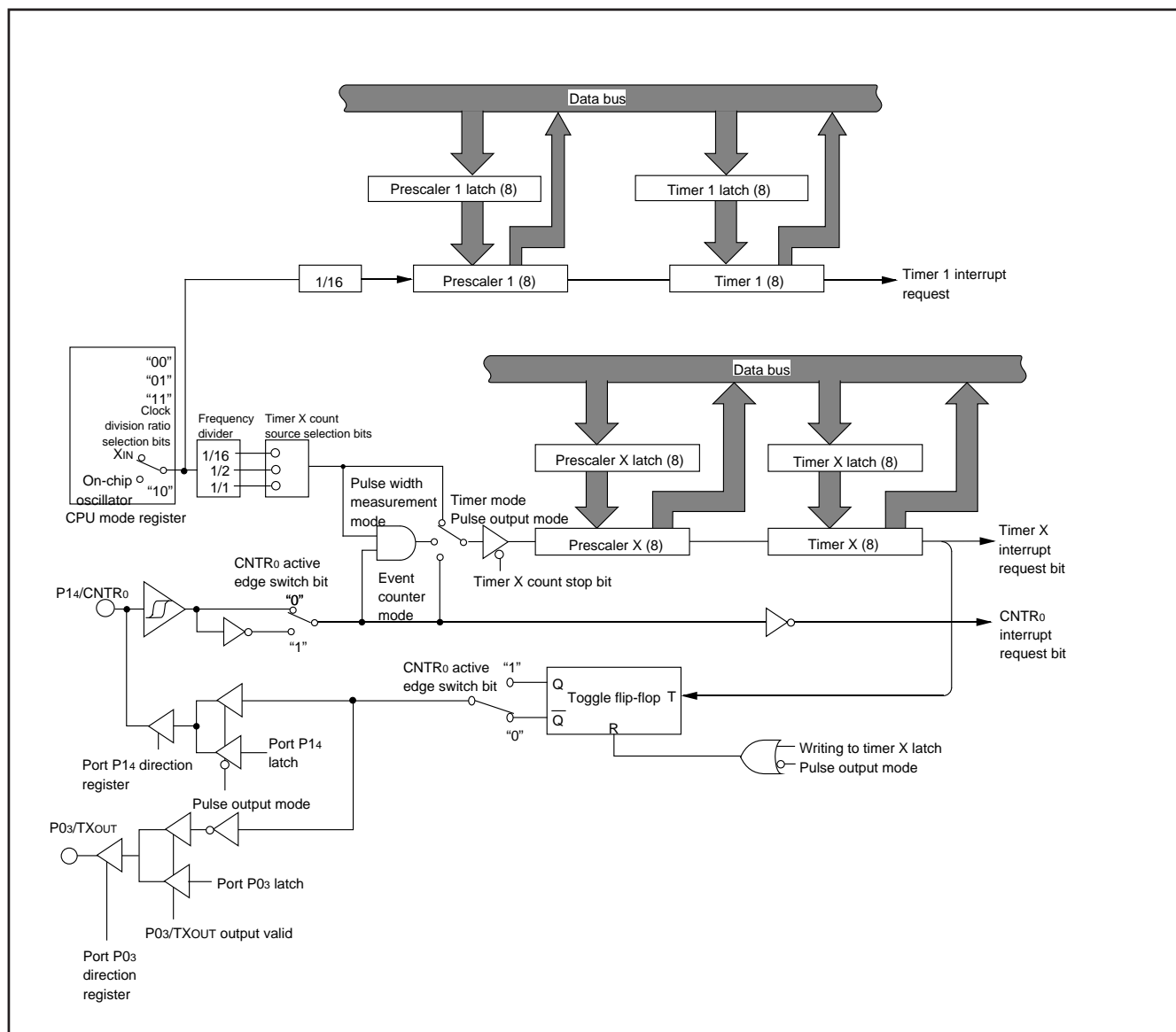


Fig. 28 Block diagram of timer 1 and timer X

●Timer A,B

Timer A and Timer B are 16-bit timers and counts the signal which is the oscillation frequency selected by setting of the timer count source set register (TCSS). Timer A and Timer B have the same function except of the count source clock selection.

The count source clock of Timer A is selected from among 1/2, 1/16, 1/32, 1/64, 1/128, 1/256 of f(XIN) clock and on-chip oscillator clock.

The count source clock of Timer B is selected from among 1/2, 1/16, 1/32, 1/64, 1/128, 1/256 of f(XIN) clock and Timer A underflow.

Timer A (B) consists of the low-order of Timer A: TAL (Timer B: TBL) and the high-order of Timer A: TAH (Timer B: TBH). Timer A (B) is decremented by 1 when each time of the count clock is input. When the contents of Timer A (B) reach "000016", an underflow occurs at the next count clock, and the timer latch is reloaded into timer. When Timer A (B) underflows, the Timer A (B) interrupt request bit is set to "1".

Timer A (B) has the Timer A (B) latch to retain the load value. The value of timer A (B) latch is set to Timer A (B) at the timing of Timer A (B) underflow. The division ratio of Timer A (B) is 1/(n+1) provided that the value of Timer A (B) is n.

When writing to both the low-order of Timer A (B) and the high order of Timer A (B) is executed, writing to "latch only" or "latch and timer" can be selected by the setting value of the timer A (B) write control bit.

When reading from Timer A (B) register is executed, the count value of Timer A (B) is read out.

Be sure to write to/read out the low-order of Timer A (B) and the high-order of Timer A (B) in the following order;

- Read

Read the high-order of Timer A (B) first, and the low-order of Timer A (B) next and be sure to read both high-order and low-order.

- Write

Write to the low-order of Timer A (B) first, and the high-order of Timer A (B) next and be sure to write both low-order and high order.

Timer A and Timer B can be used for the timing timer of Input capture and Output compare function.

■ Notes on Timer A, B

(1) Setting of timer value

When "1: Write to only latch" is set to the timer A (B) write control bit, written data to timer register is set to only latch even if timer is stopped. Accordingly, in order to set the initial value for timer when it is stopped, set "0: Write to latch and timer simultaneously" to timer A (B) write control bit.

(2) Read/write of timer A

Stop timer A to read/write its data when the system is in the following state;

- CPU operation clock source: XIN oscillation
- Timer A count source: On-chip oscillator output

(3) Read/write of timer B

Stop timer B to read/write its data when the system is in the following state;

- CPU operation clock source: XIN oscillation
- Timer B count source: Timer A underflow
- Timer A count source: On-chip oscillator output

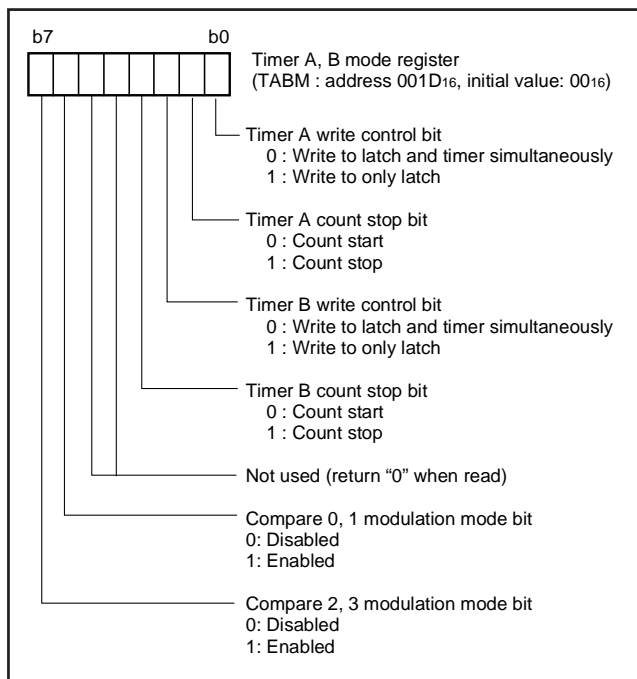


Fig. 29 Structure of timer A, B mode register

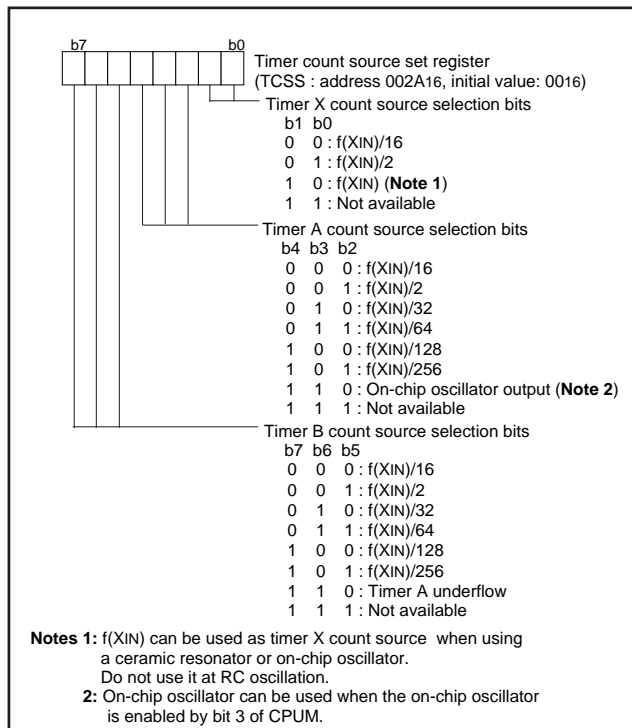


Fig. 30 Timer count source set register

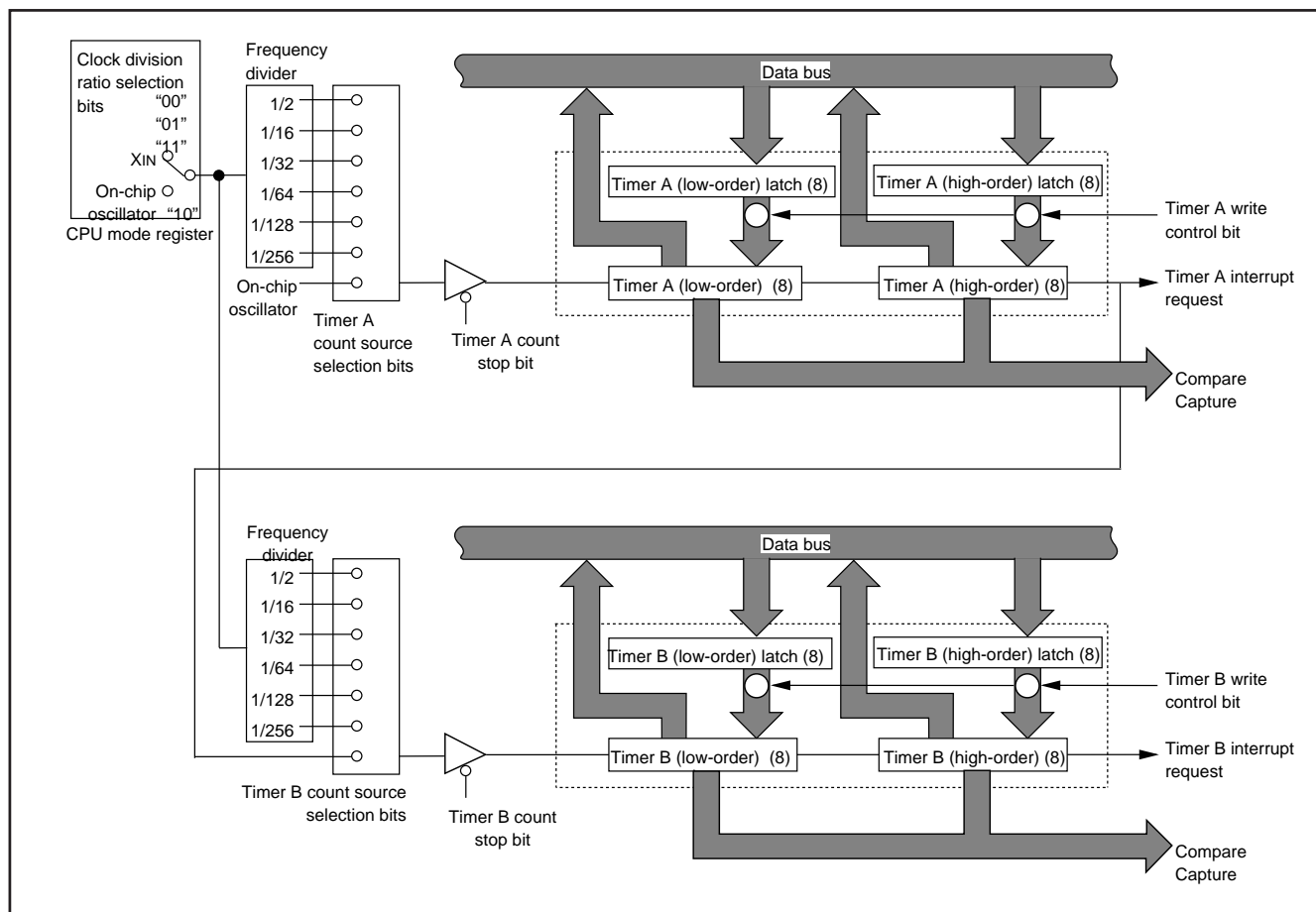


Fig. 31 Block diagram of timer A and timer B

Output compare

7546 group has 4-output compare channels. Each channel (0 to 3) has the same function and can be used to output waveform by using count value of either Timer A or Timer B.

The source timer for each channel is selected by setting value of the compare x ($x = 0, 1, 2, 3$) timer source bit. Timer A and Timer B can be selected for the source timer to each channel, respectively.

To use each compare channel, set "1" to the compare x output port bit and set the port direction register corresponding to compare channel to output mode.

The compare value for each channel is set to the compare register (low-order) and compare register (high-order).

Writing to the register for each channel is controlled by setting value of compare register write pointer. Writing to each register is in the following order;

1. Set the value of corresponded output compare channel to the compare register write pointer.
2. Write a value to the compare register (low-order) and compare register (high-order).
3. Set "1" to the compare latch y ($y = 00, 01, 10, 11, 20, 21, 30, 31$) re-load bit.

When "1" is set to the compare latch y re-load bit, the value set to the compare register is loaded to compare latch when the next timer underflow.

When count value of timer and setting value of compare latch is matched, compare output trigger occurs.

When "1: Enabled" is set to the compare trigger x enable bit, the output waveform from port is inverted by compare trigger.

When "0: Disabled" is set to the compare trigger x enable bit, the output waveform is not inverted, so port output can be fixed to "H" or "L".

When "0: Positive" is set to the compare x output level latch, the compare output waveform is turned to "H level" at compare latch $x0$'s match and turned to "L level" at compare latch $x1$'s match.

When "1: Negative" is set to the compare x output level latch, the compare output waveform is turned to "L level" at compare latch $x0$'s match and turned to "H level" at compare latch $x1$'s match.

The compare output level of each channel can be confirmed by reading the compare x output status bit.

Compare output interrupt is available when match of each compare channel and timer count value. The interrupt request from each channel can be disabled or enabled by setting value of compare latch y interrupt source bit.

Compare 0,1 (2,3) modulation mode

In compare modulation mode, modulation waveform can be generated by using compare channel 0 and 1, or compare channel 2 and 3. To use this mode,

- Set "1: Enabled" to the compare 0,1 (2, 3) modulation mode bit.
- Set Timer A underflow for Timer B count source.
- Set Timer A for the timer source of compare channel 0 (2).
- Set Timer B for the timer source of compare channel 1 (3).

In this mode, AND waveform of compare 0 (1) and compare 2 (3) is generated from Port P01 and P31, respectively. Accordingly, in order to use this mode, set "1" to the compare 0 output port bit or compare 2 output port bit.

■ Notes on Output Compare

- When the selected source timer of each compare channel is stopped, written data to compare register is loaded to the compare latch simultaneously.
- Do not write the same data to both of compare latch $x0$ and $x1$.
- When setting value of the compare latch is larger than timer setting value, compare match signal is not generated. Accordingly, the output waveform is fixed to "L" or "H" level.
However, when setting value of another compare latch is smaller than timer setting value, this compare match signal is generated. Accordingly, compare match interrupt occurs.
- When the compare x trigger enable bit is cleared to "0" (disabled), the match trigger to the waveform output circuit is disabled, and the output waveform can be fixed to "L" or "H" level.

However, in this case, the compare match signal is generated. Accordingly, compare match interrupt occurs.

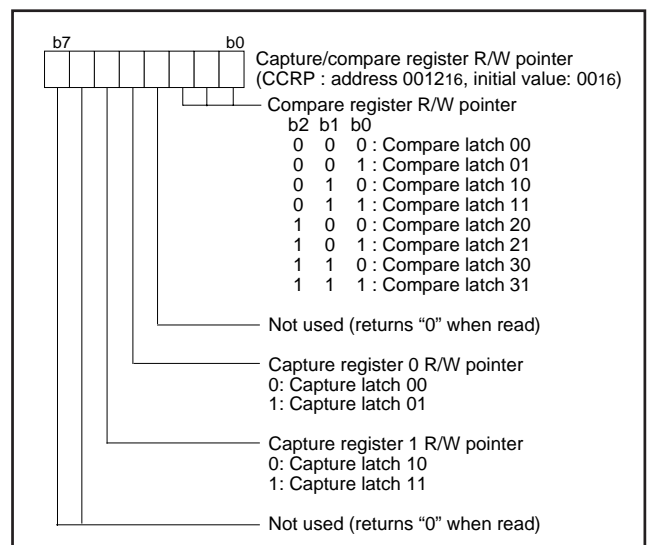


Fig. 32 Structure of capture/compare register R/W pointer

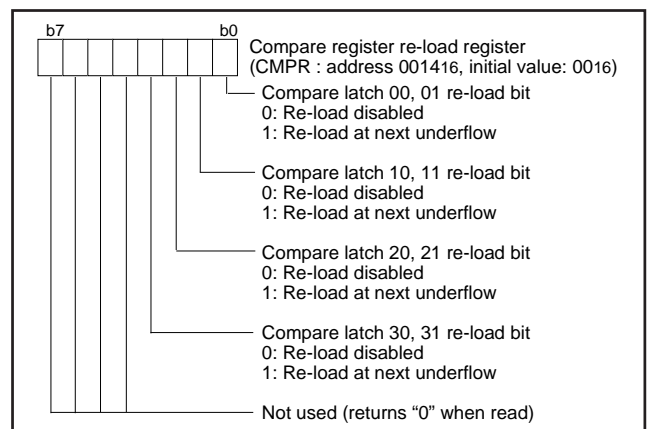


Fig. 33 Structure of compare register re-load register

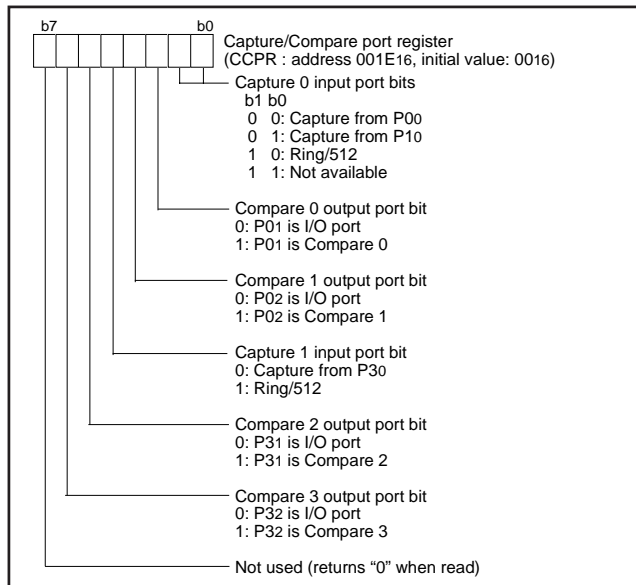


Fig. 34 Structure of capture/compare port register

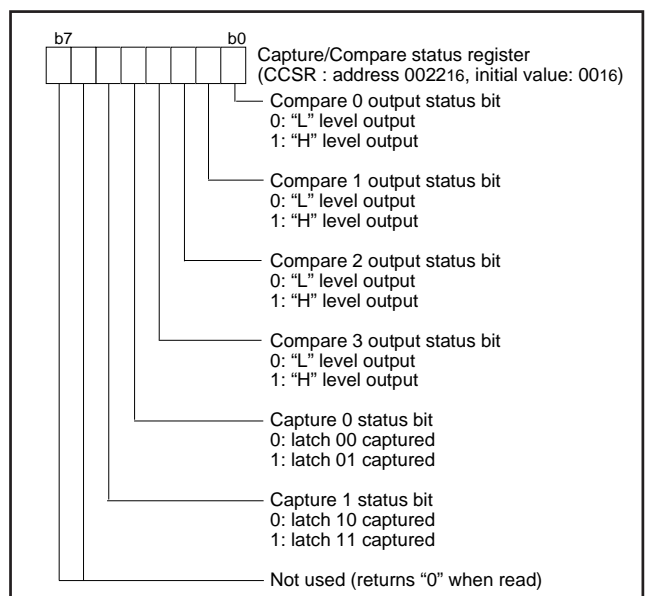


Fig. 37 Structure of capture/compare status register

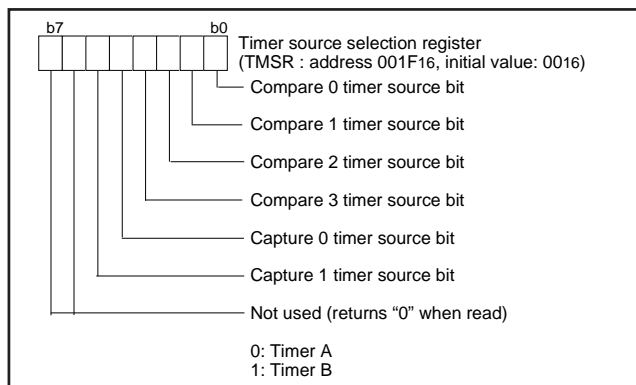


Fig. 35 Structure of timer source selection register

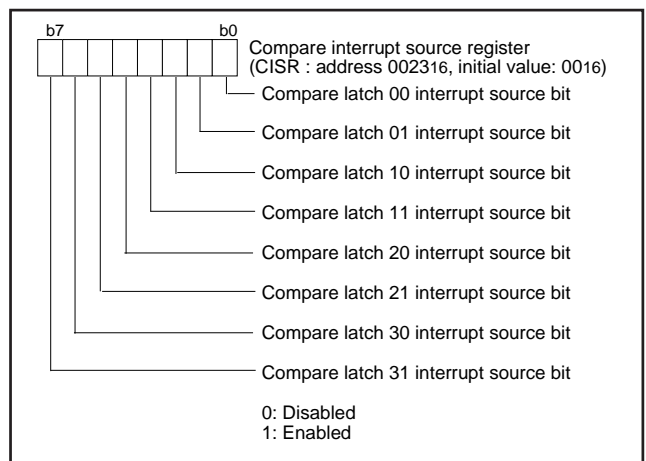


Fig. 38 Structure of compare interrupt source register

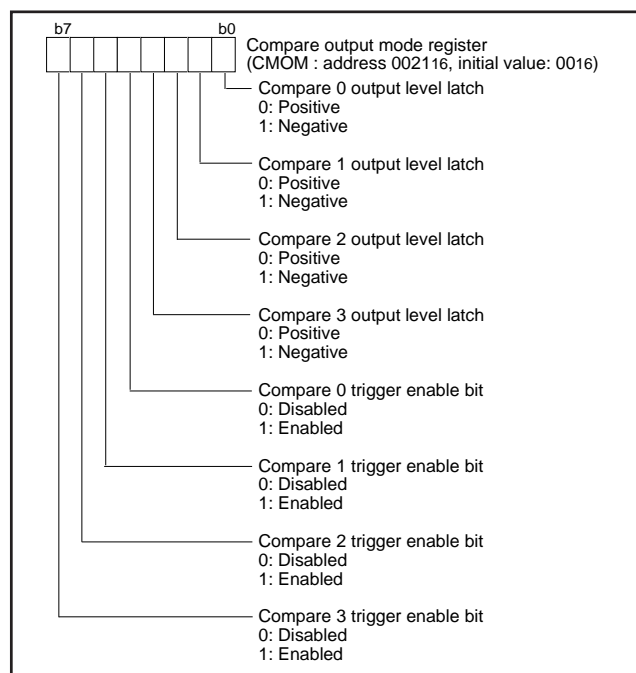


Fig. 36 Structure of compare output mode register

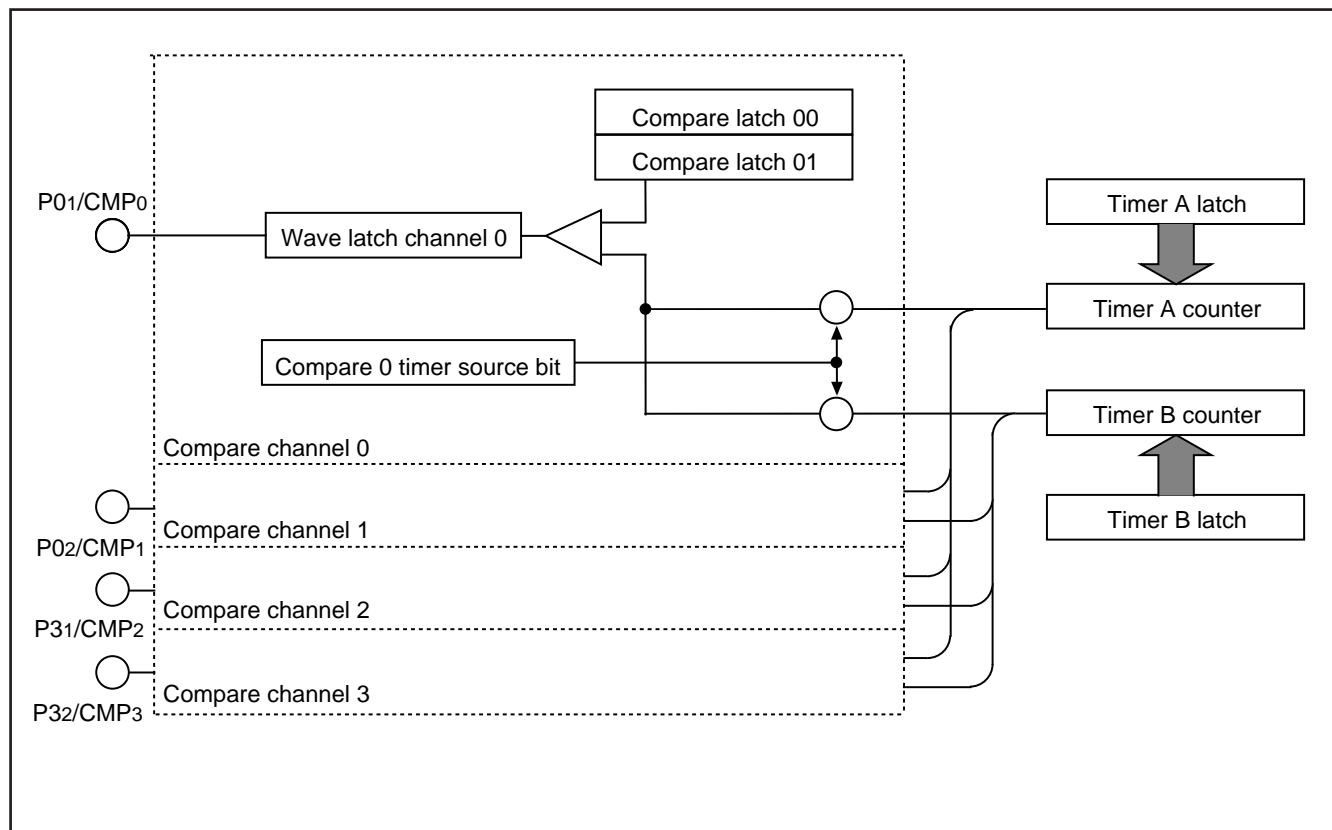


Fig. 39 Block diagram of output compare

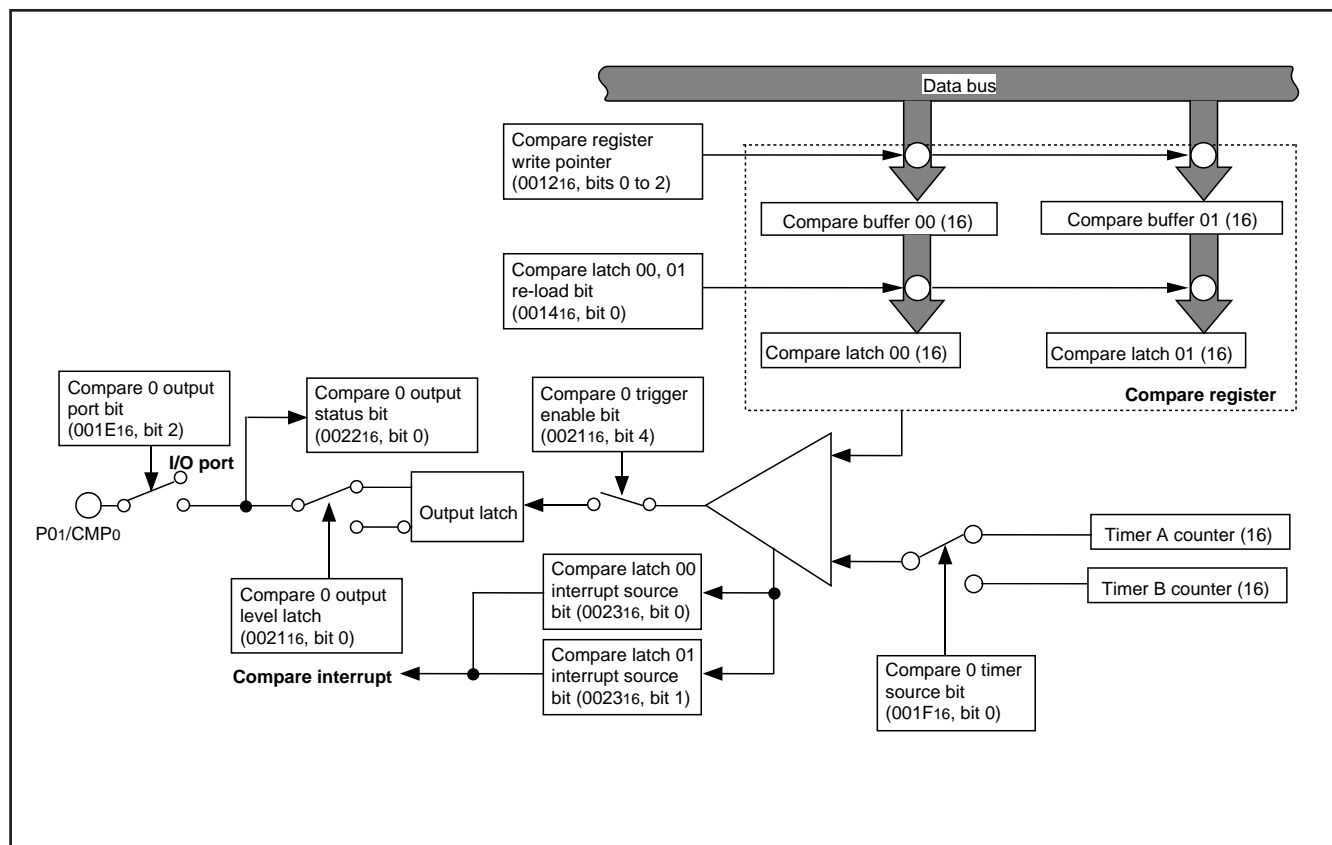


Fig. 40 Block diagram of compare channel 0

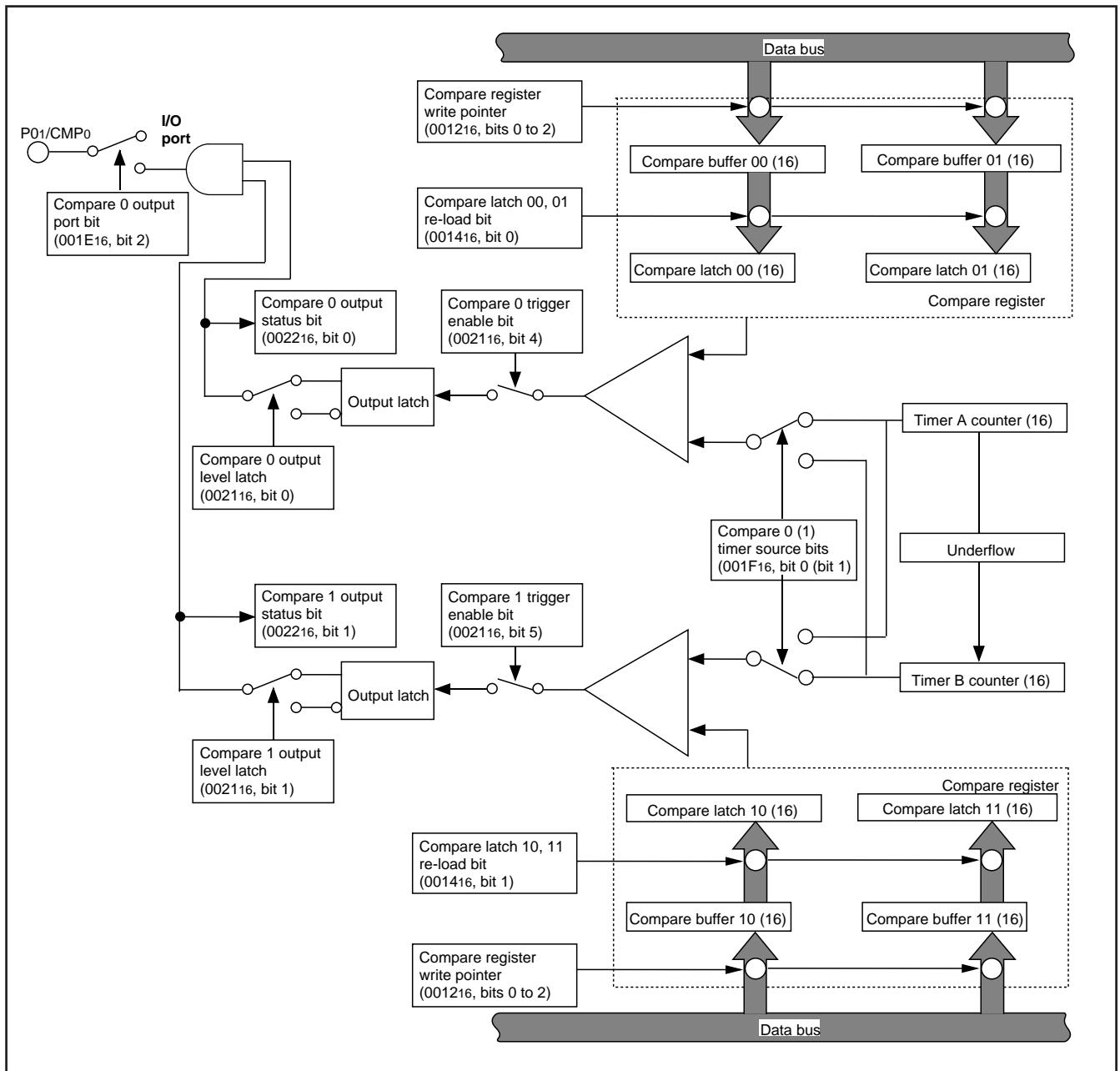


Fig. 41 Block diagram at modulation mode

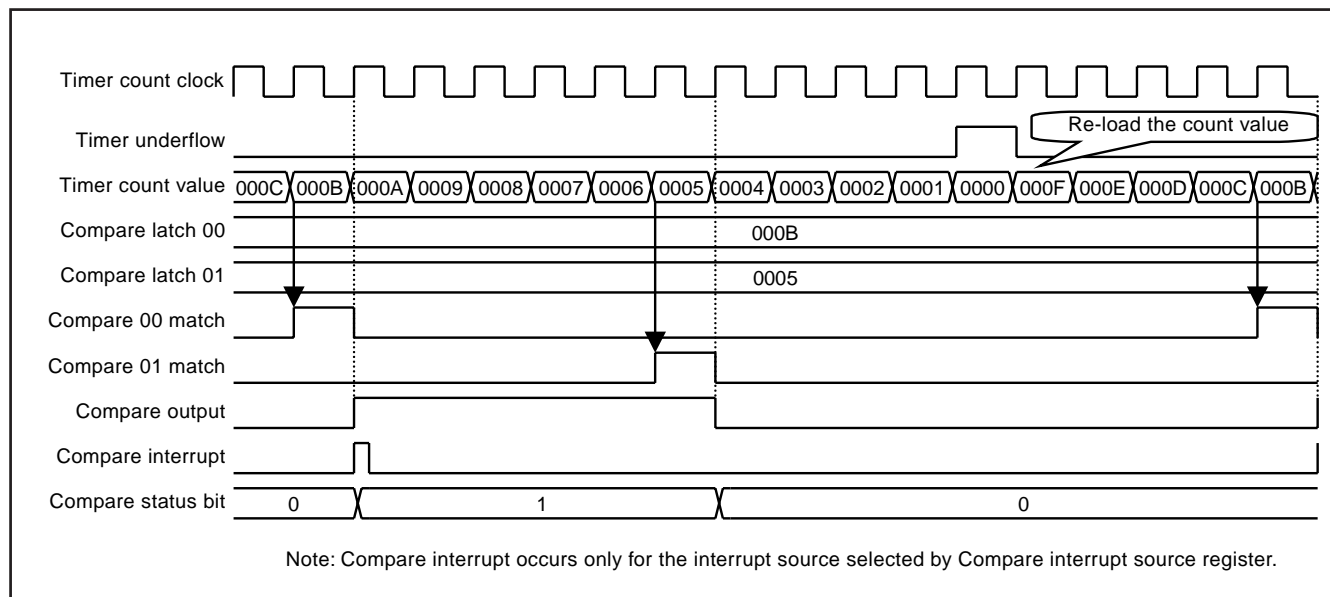


Fig. 42 Output compare mode (general waveform)

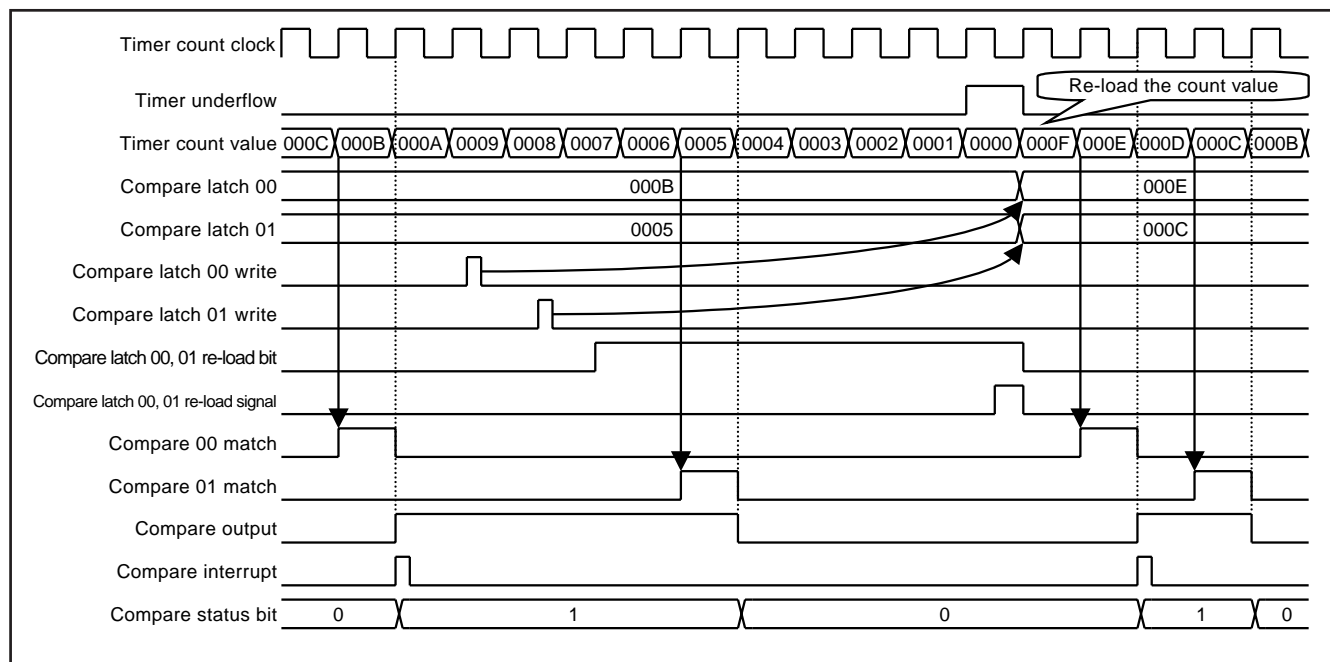


Fig. 43 Output compare mode (compare register write timing)

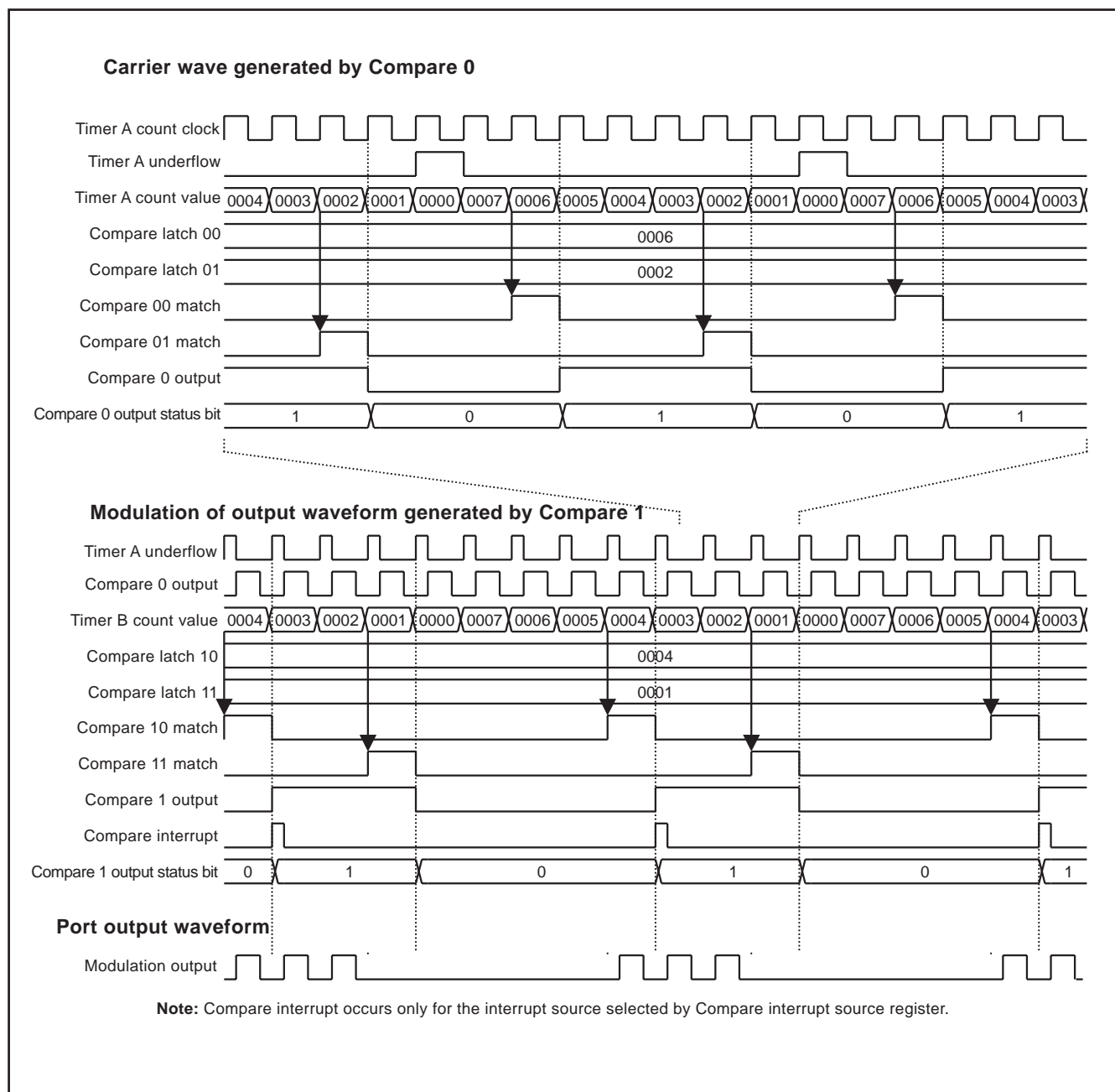


Fig. 44 Output compare mode (compare 0, 1 modulation mode)

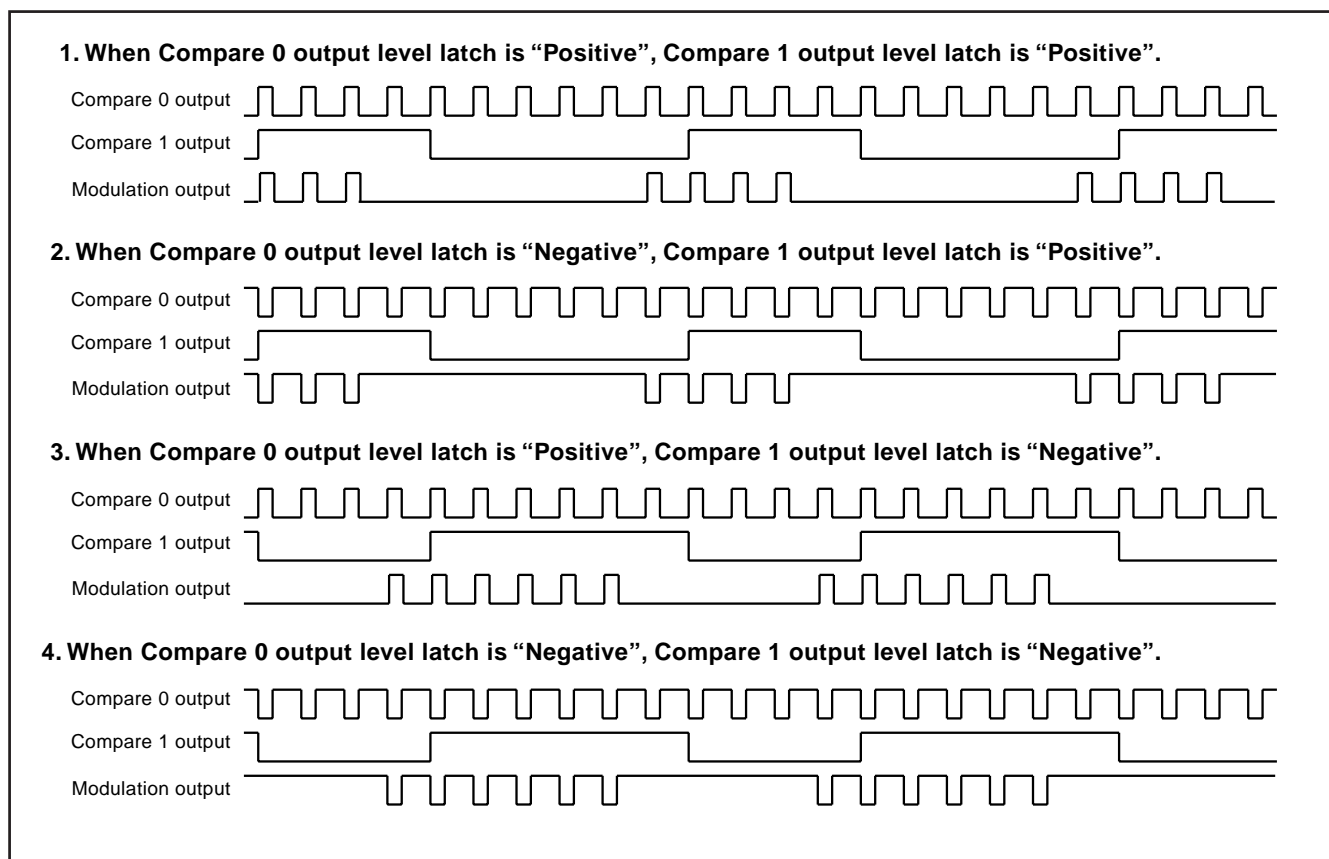


Fig. 45 Output compare mode (compare 0, 1 modulation mode: effect of output level latch)

Input capture

7546 group has 2-input capture channels. Each channel (0 and 1) has the same function and can be used to capture count value of either Timer A or Timer B.

The source timer for each channel is selected by setting value of the capture x (x = 0, 1) timer source bit. Timer A and Timer B can be selected for the source timer to each channel, respectively.

To use each capture channel, set the capture x input port bits and set the port direction register corresponding to capture channel to input mode.

The input capture circuit retains the count value of selected timer when external trigger is input. The timer count value is retained to the capture latch x0 when rising edge is input and is retained to the capture latch x1 when falling edge is input.

The count value of timer can be retained by software by capture y (y = 00, 01, 10, 11) software trigger bit too. When "1" is set to this bit, count value of timer is retained to the corresponded capture latch.

When reading from the capture y software trigger bit is executed, "0" is read out.

The latest status of capture latch can be confirmed by reading of the capture x status bit. This bit indicates the capture latch which latest data is in.

The valid trigger edge for capture interrupt is set by the capture x interrupt edge selection bits. (Regardless of the setting value of capture x interrupt edge selection bits, timer count values for both edges are retained to the capture latch.)

Each capture input has the noise filter circuit that judges continuous 4-time same level with sampling clock to be valid. The sampling clock of noise filter is set by the capture x noise filter clock selection bits.

Reading from the register for each channel is controlled by setting value of the capture register read pointer. Reading from each register is in the following order;

1. Set the value of the corresponded input capture channel to the capture register read pointer.
2. Read from the capture register (low-order) and capture register (high-order).

■ Notes on Input Capture

- If the capture trigger is input while the capture register (low-order and high-order) is in read, captured value is changed between high-order reading and low-order reading. Accordingly, some countermeasure by program is recommended, for example comparing the values that twice of read.
- When CPU operation clock source is XIN oscillation and the on-chip-oscillator is selected for Timer A count source, Timer A cannot be used for the capture source timer. Timer B cannot be used for the capture source timer when the system is in the following state;
 - CPU operation clock source: XIN oscillation
 - Timer B count source: Timer A underflow
 - Timer A count source: On-chip oscillator output
- When writing "1" to capture latch x0 (x1) software trigger bit of capture latch x0 and x1 at the same time, or external trigger and software trigger occur simultaneously, the set value of capture x status bit is undefined.
- When setting the interrupt active edge selection bit and noise filter clock selection bit of external interrupt CAP0, CAP1, the interrupt request bit may be set to "1". When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.
 - ① Set the corresponding interrupt enable bit to "0" (disabled).
 - ② Set the interrupt edge selection bit or noise filter clock selection bit.
 - ③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
 - ④ Set the corresponding interrupt enable bit to "1" (enabled).
- When the capture interrupt is used as the interrupt for return from stop mode, set the capture x noise filter clock selection bits to "00 (Filter stop)".

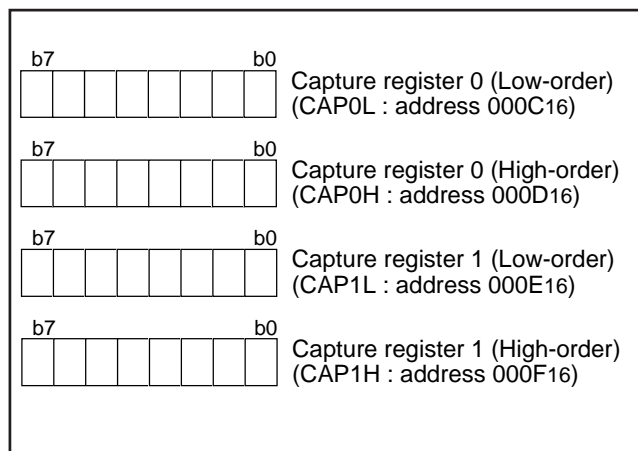


Fig. 46 Structure of capture software trigger register

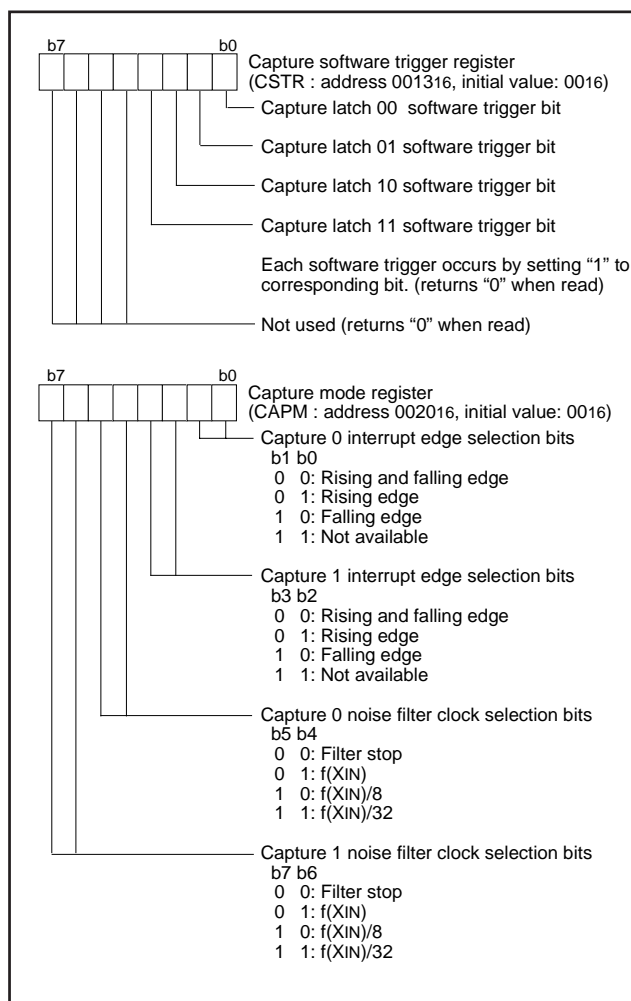


Fig. 47 Structure of capture software trigger register/capture mode register

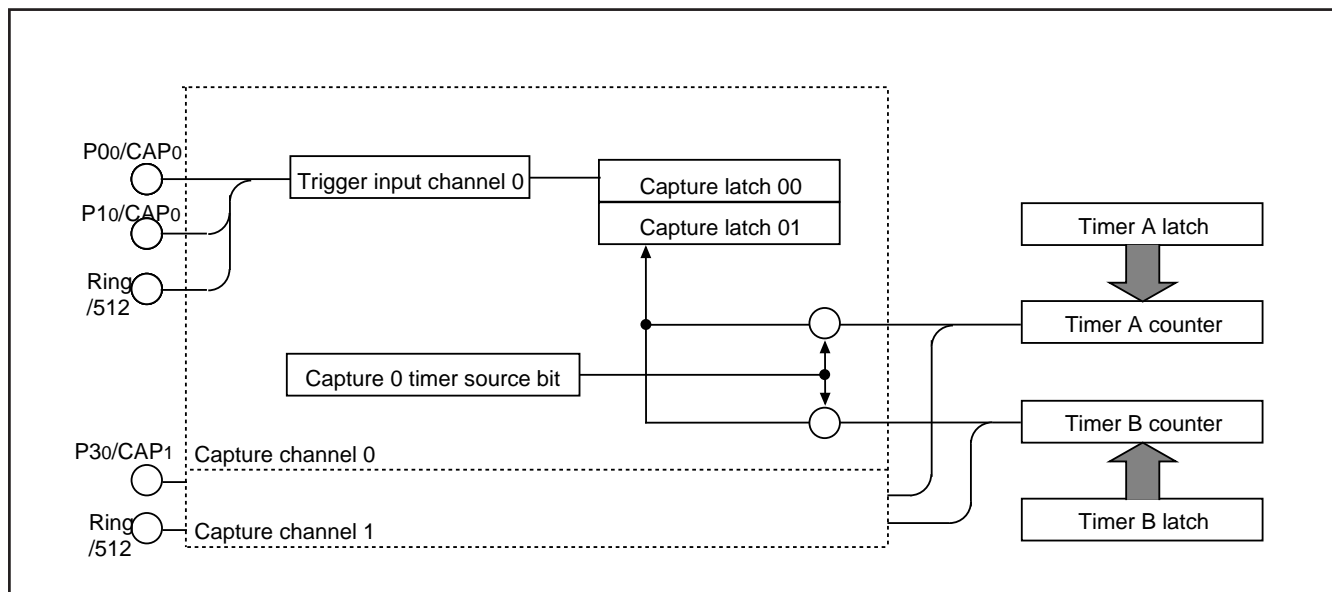


Fig. 48 Block diagram of input capture

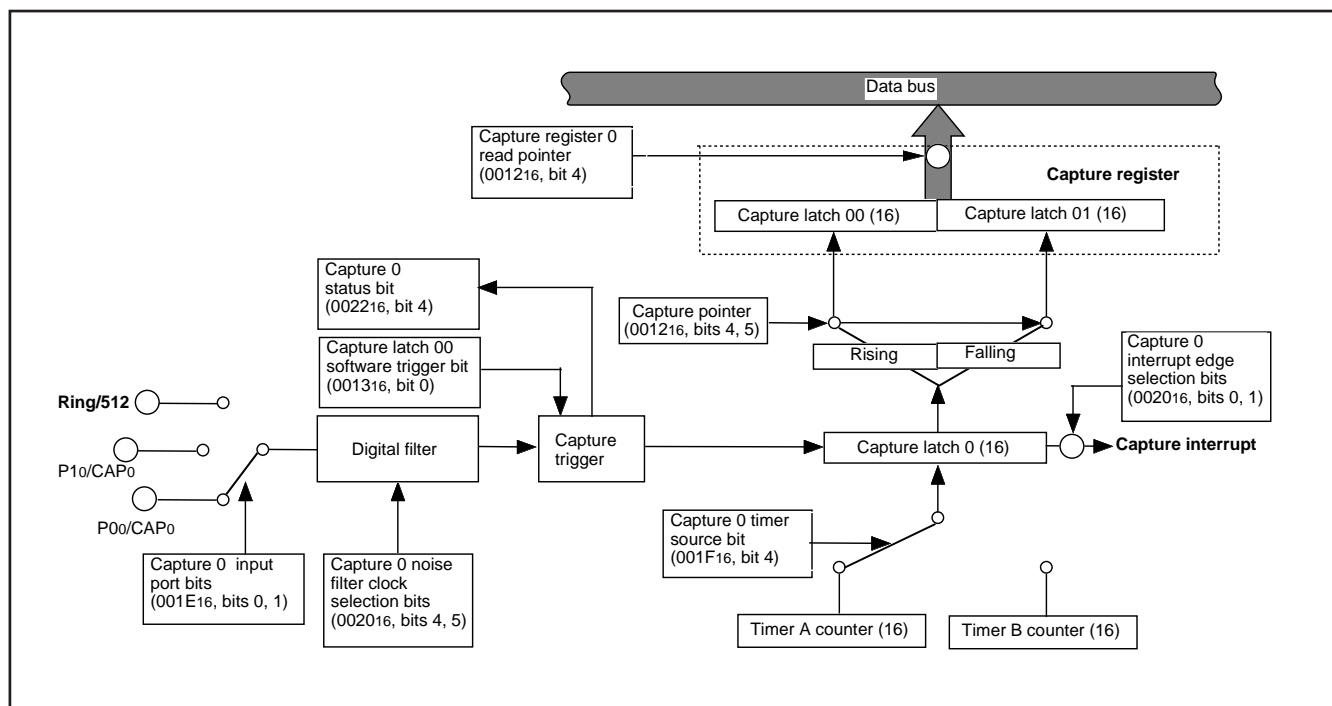


Fig. 49 Block diagram of capture channel 0

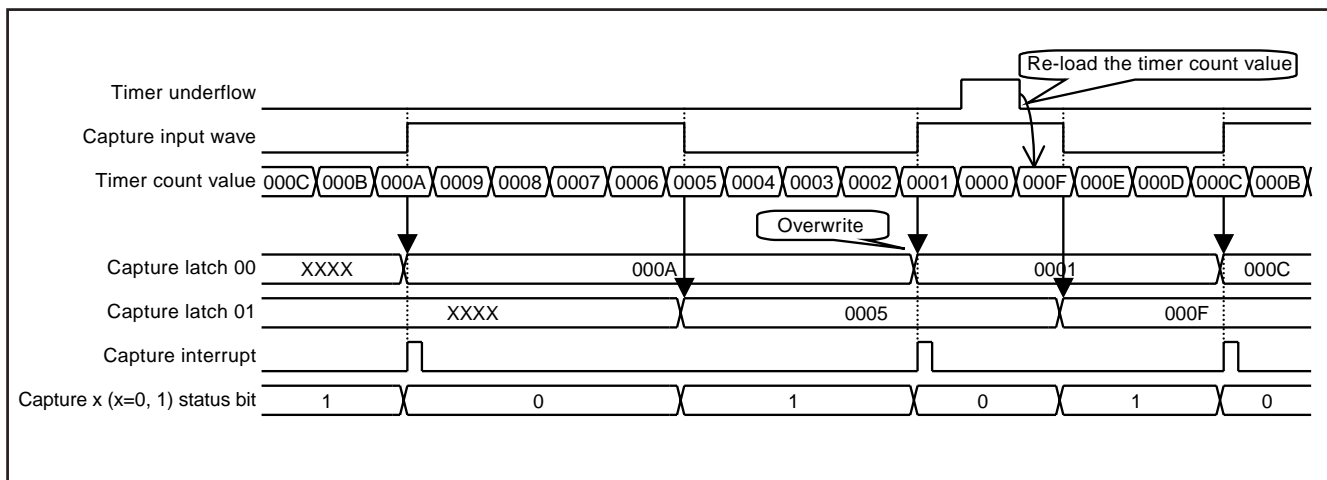


Fig. 50 Capture interrupt edge selection = "rising edge"

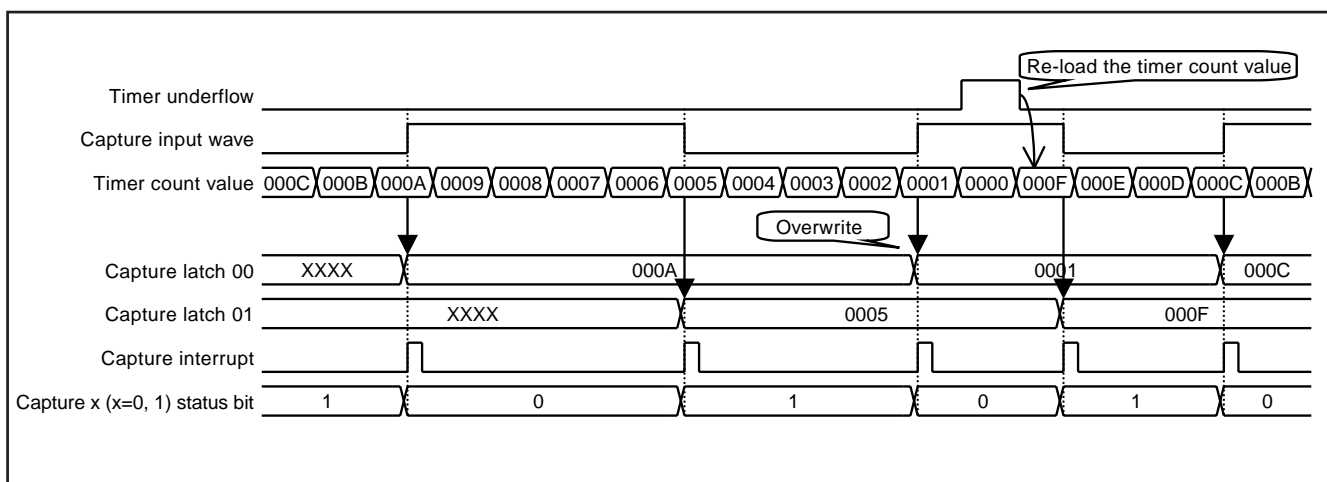


Fig. 51 Capture interrupt edge selection = "rising and falling edge"

Serial Interface

The 7546 Group has Serial I/O1 and Serial I/O2. Except that Serial I/O1 has the bus collision detection function and the Tx/D2 output structure for Serial I/O2 is CMOS only, they have the same function.

●Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O1 Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6) to “1”.

For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

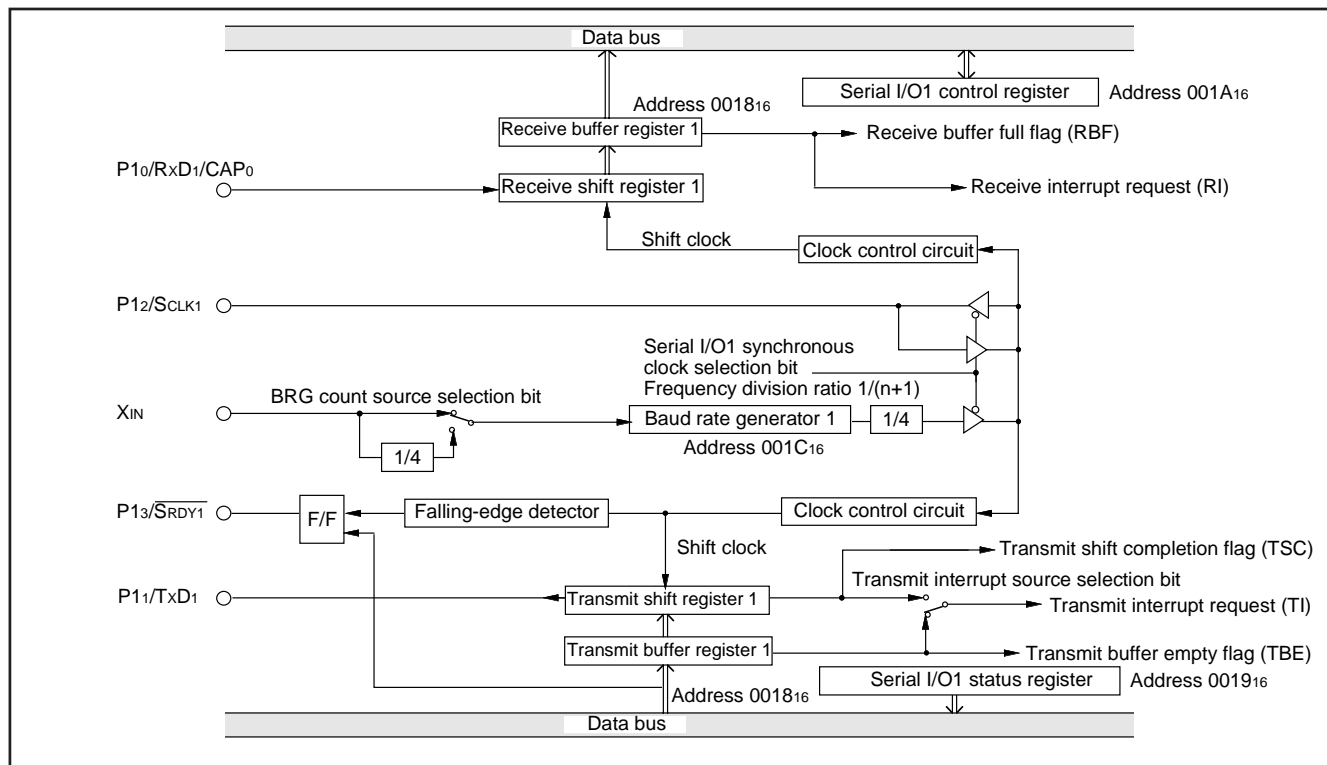


Fig. 52 Block diagram of clock synchronous serial I/O1

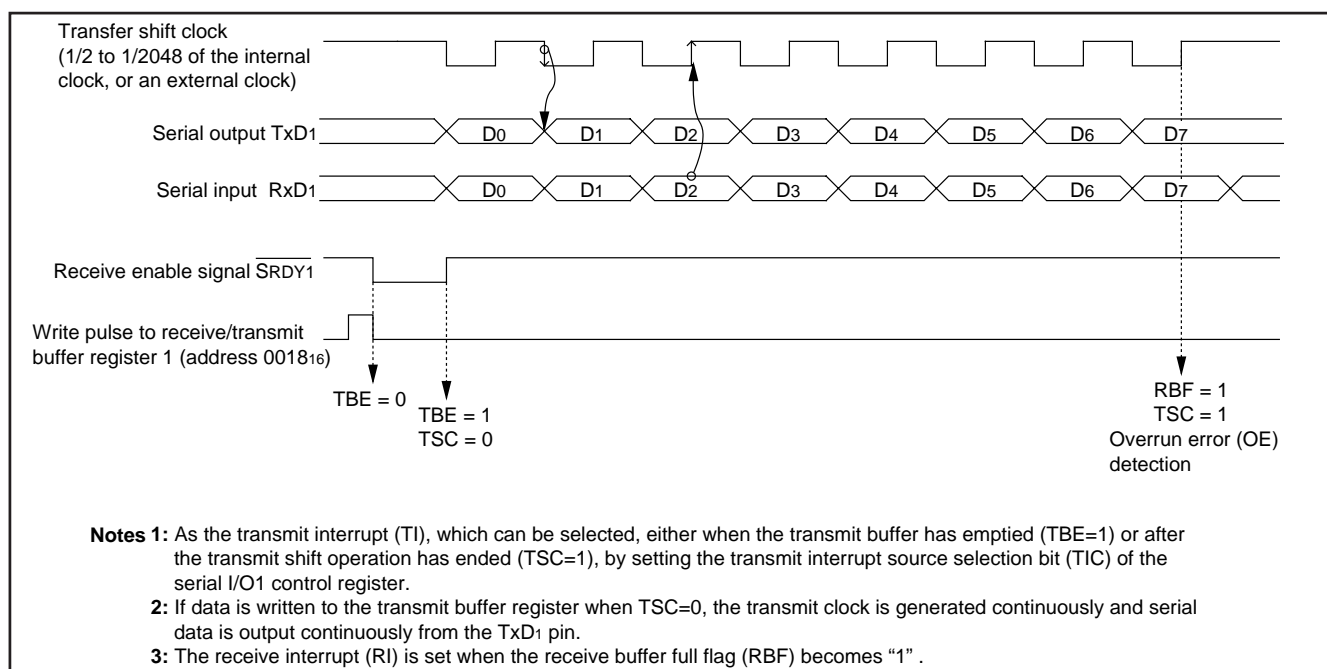


Fig. 53 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O1 (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

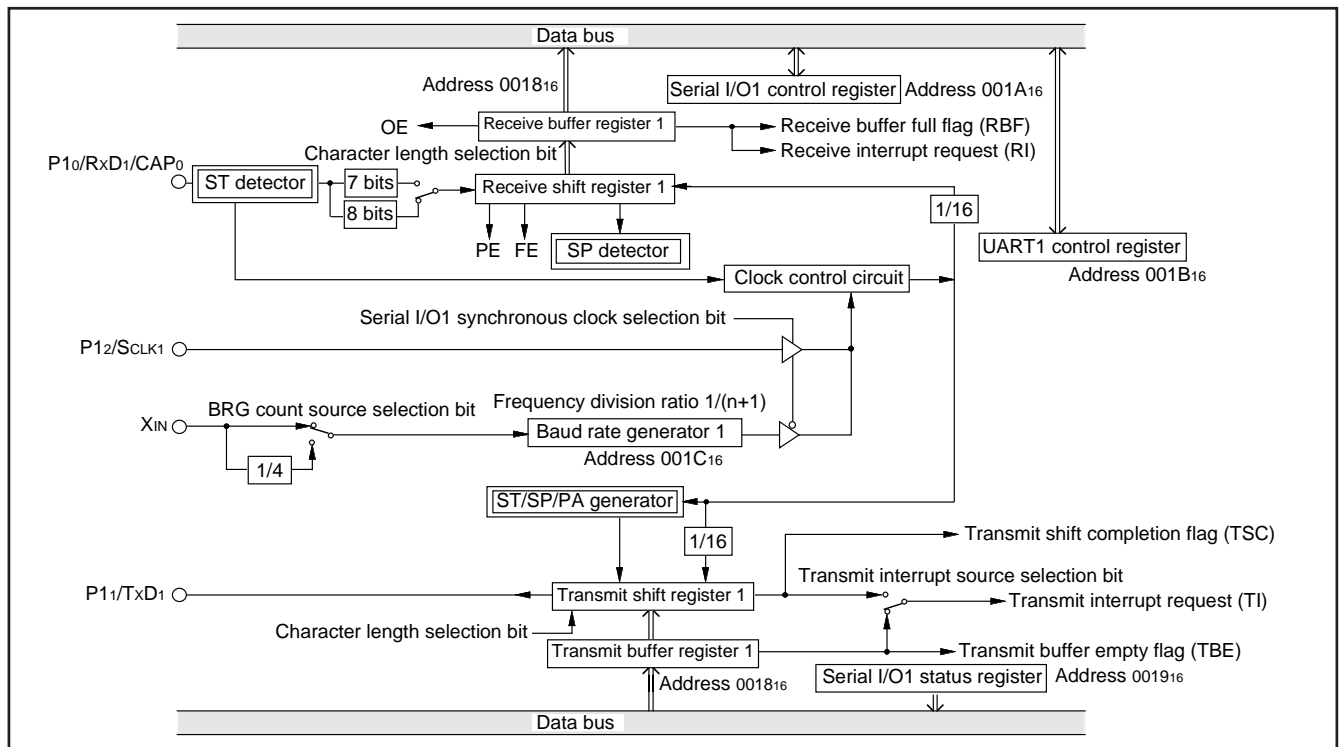


Fig. 54 Block diagram of UART serial I/O1

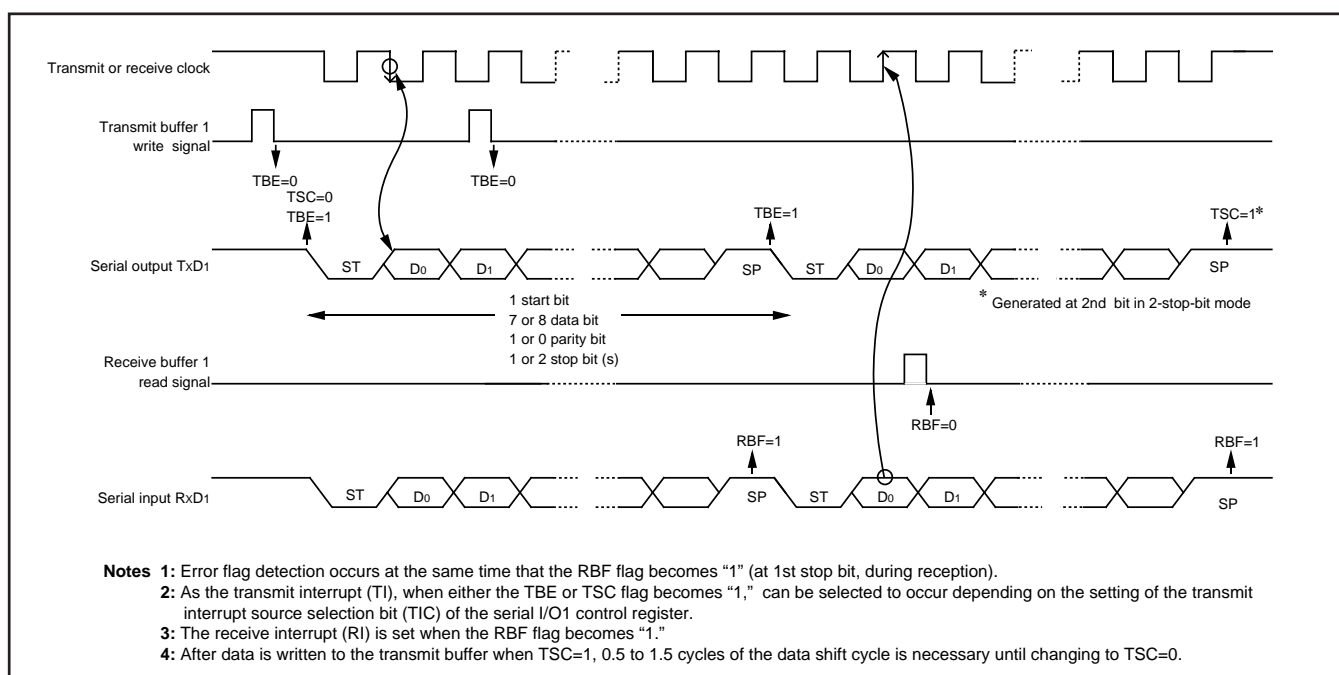


Fig. 55 Operation of UART serial I/O1 function

[Transmit buffer register 1/receive buffer register 1 (TB1/RB1)] 001816

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O1 status register (SIO1STS)] 001916

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O1 control register (SIO1CON)] 001A16

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART1 control register (UART1CON)] 001B16

The UART1 control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of a data transfer and one bit (bit 4) which is always valid and sets the output structure of the P11/TxD1 pin.

[Baud rate generator 1 (BRG1)] 001C16

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

■ Notes on Serial I/O1**• Serial I/O interrupt**

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- ① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ④ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O1 is enabled.

The functions of P12 and P13 are switched with the setting values of a serial I/O1 mode selection bit and a serial I/O1 synchronous clock selection bit as follows.

(1) Serial I/O1 mode selection bit → "1" :

Clock synchronous type serial I/O is selected.

Setup of a serial I/O1 synchronous clock selection bit

"0" : P12 pin turns into an output pin of a synchronous clock.

"1" : P12 pin turns into an input pin of a synchronous clock.

Setup of a $\overline{\text{SRDY1}}$ output enable bit (SRDY)

"0" : P13 pin can be used as a normal I/O pin.

"1" : P13 pin turns into a $\overline{\text{SRDY1}}$ output pin.

(2) Serial I/O1 mode selection bit → "0" :

Clock asynchronous (UART) type serial I/O is selected.

Setup of a serial I/O1 11synchronous clock selection bit

"0" : P12 pin can be used as a normal I/O pin.

"1" : P12 pin turns into an input pin of an external clock.

When clock asynchronous (UART) type serial I/O is selected, it is P13 pin. It can be used as a normal I/O pin.

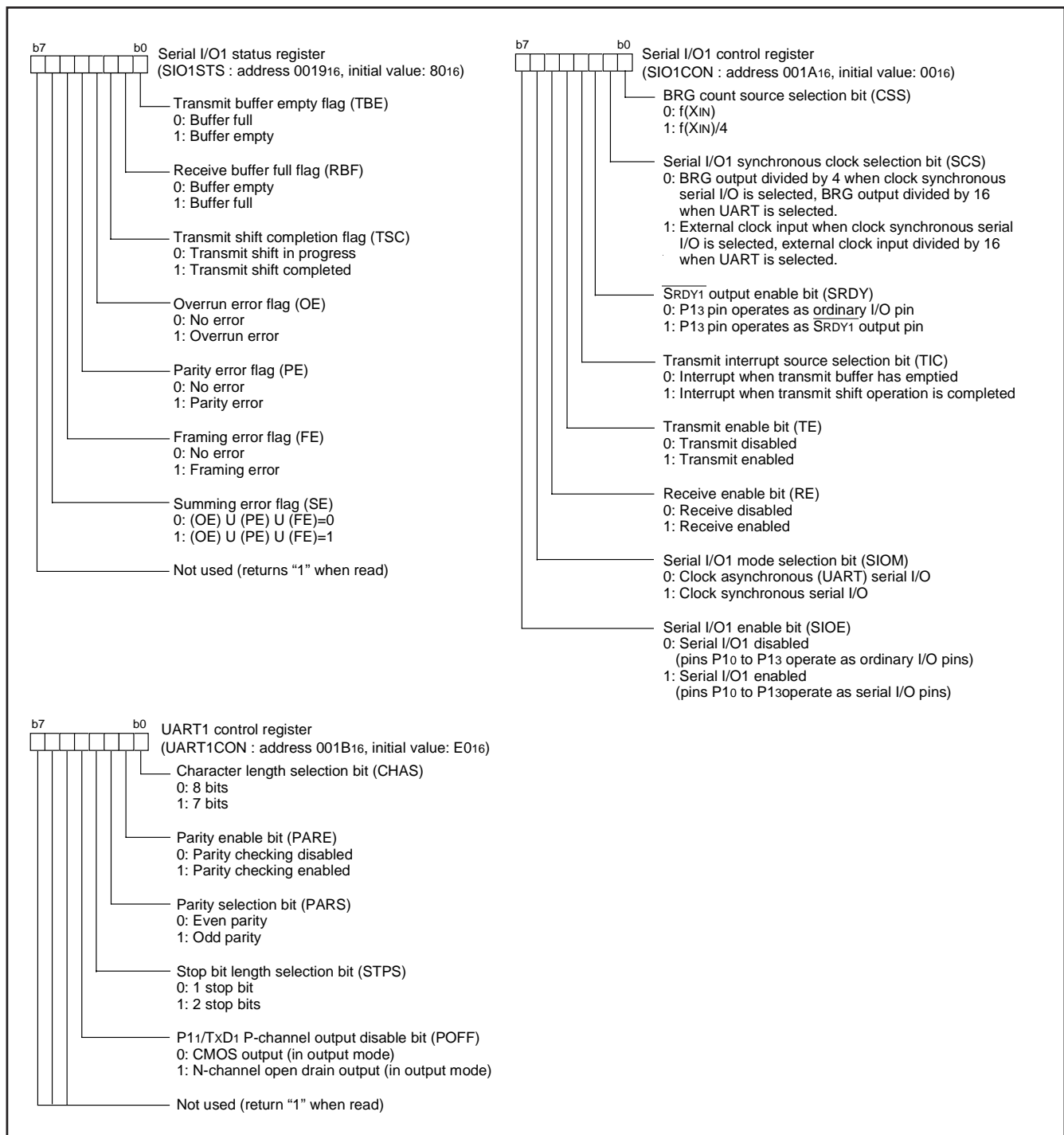


Fig. 56 Structure of serial I/O1-related registers

Bus collision detection (SIO1)

SIO1 can detect a bus collision by setting UART1 bus collision detection interrupt enable bit.

When transmission is started in the clock synchronous or asynchronous (UART) serial I/O mode, the transmit pin TxD1 is compared with the receive pin RxD1 in synchronization with rising edge of transmit shift clock. If they do not coincide with each other, a bus collision detection interrupt request occurs.

When a transmit data collision is detected between LSB and MSB of transmit data in the clock synchronous serial I/O mode or between the start bit and stop bit of transmit data in UART mode, a bus collision detection can be performed by both the internal clock and the external clock.

A block diagram is shown in Fig. 58.

A timing diagram is shown in Fig. 59.

Note: Bus collision detection can be used when SIO1 is operating at full-duplex communication. When SIO1 is operating at half-duplex communication, set bus collision detection interrupt to be disabled.

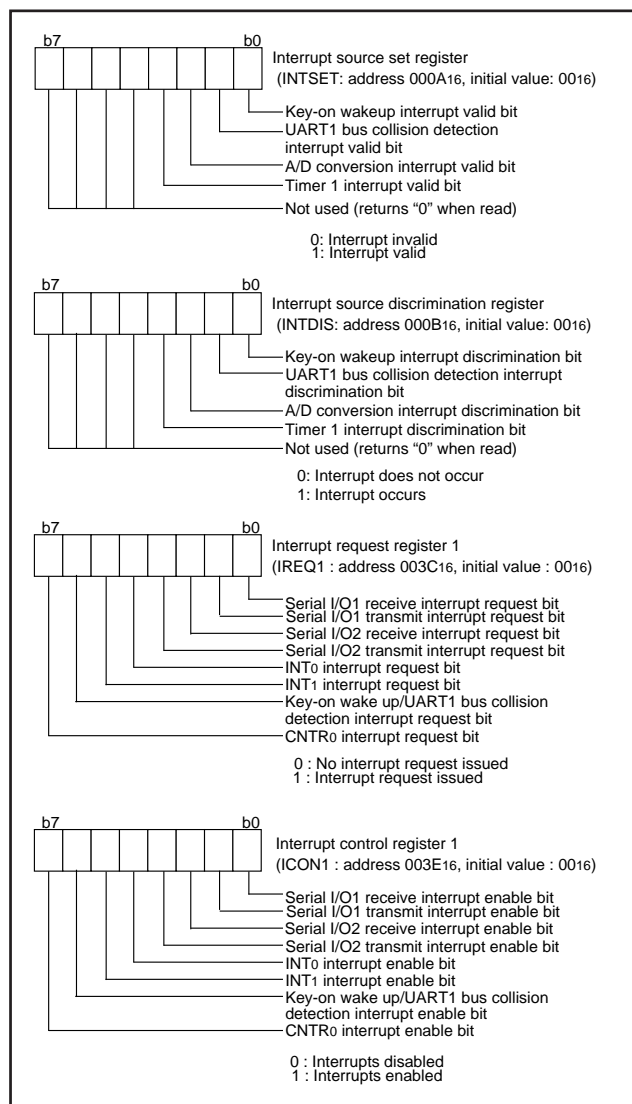


Fig. 57 Bus collision detection circuit related registers

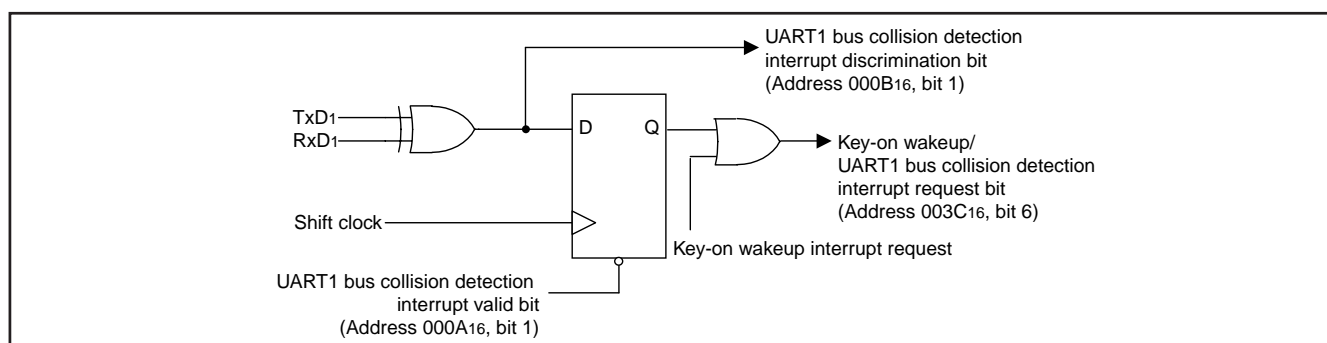


Fig. 58 Block diagram of bus collision detection interrupt circuit

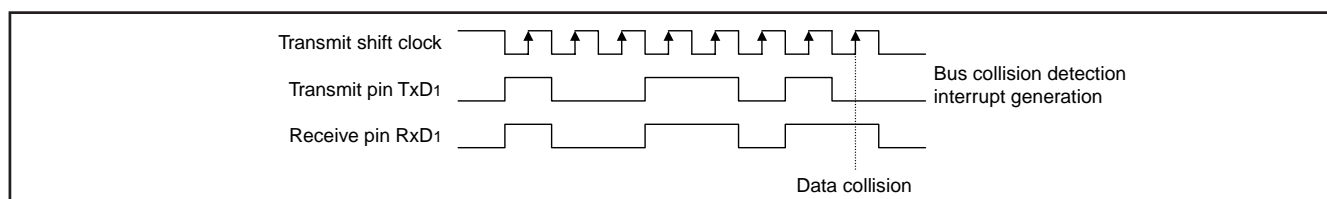


Fig. 59 Timing diagram of bus collision detection interrupt

●Serial I/O2

Serial I/O2 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O2 Mode

Clock synchronous serial I/O2 mode can be selected by setting the serial I/O2 mode selection bit of the serial I/O2 control register (bit 6) to "1".

For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

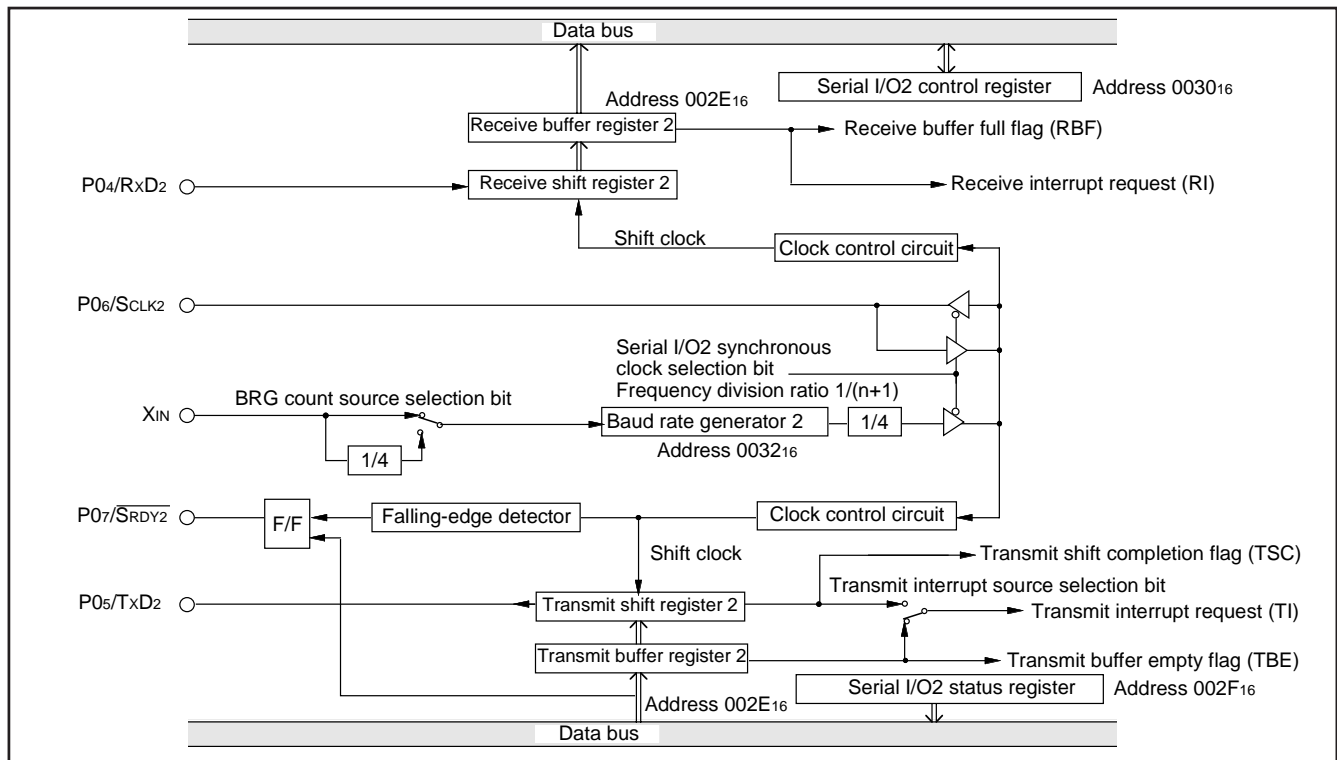


Fig. 60 Block diagram of clock synchronous serial I/O2

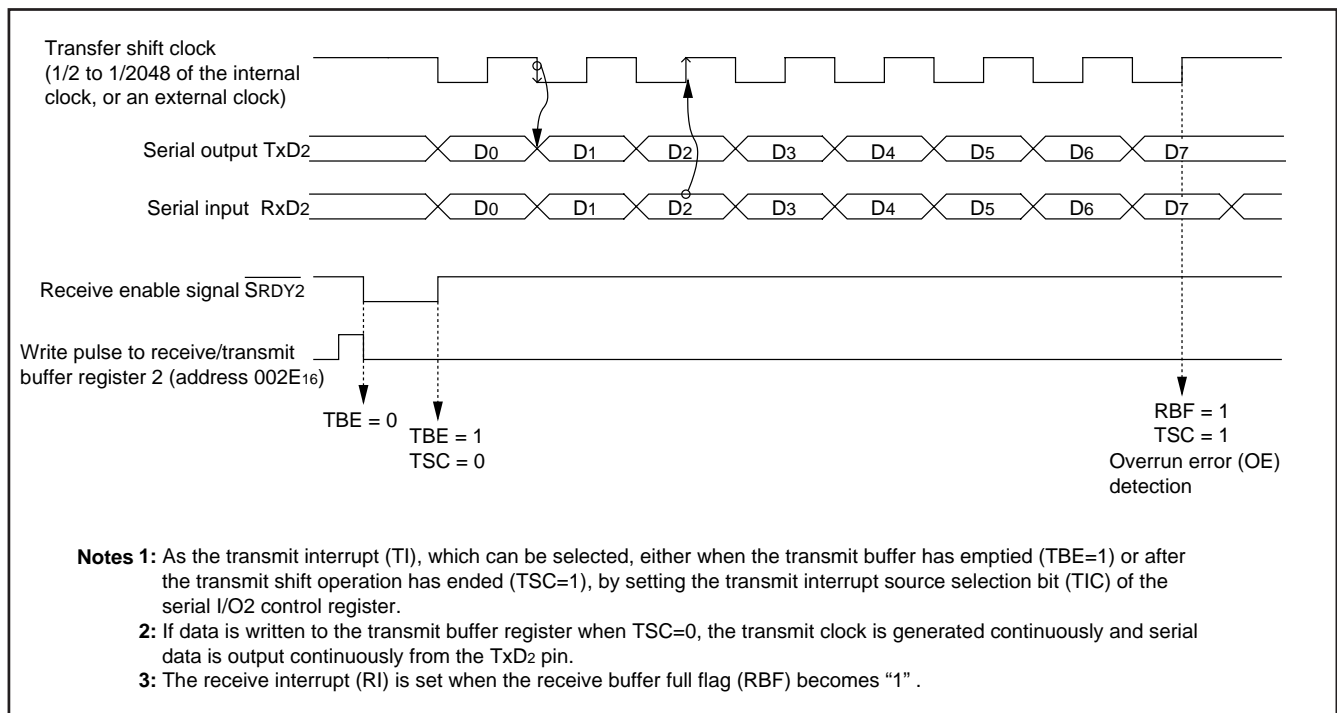


Fig. 61 Operation of clock synchronous serial I/O2 function

(2) Asynchronous Serial I/O2 (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O2 mode selection bit of the serial I/O2 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

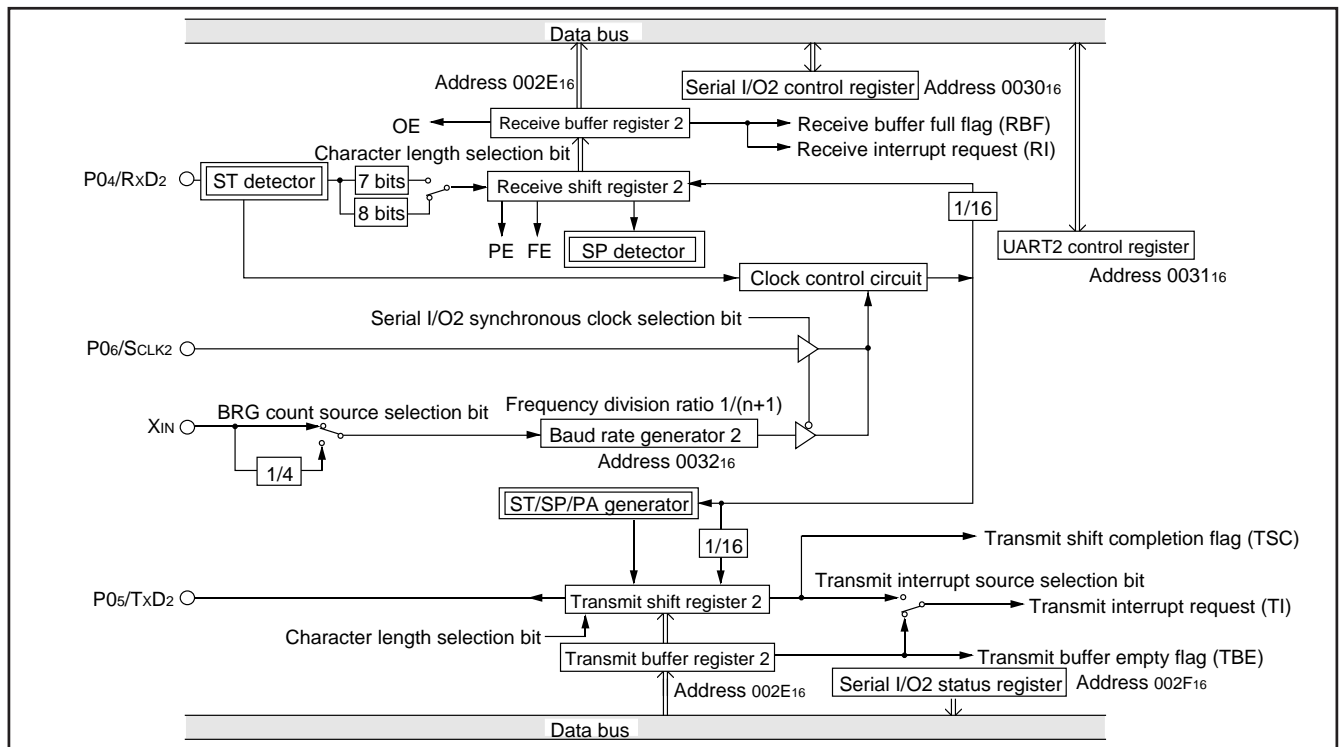


Fig. 62 Block diagram of UART serial I/O2

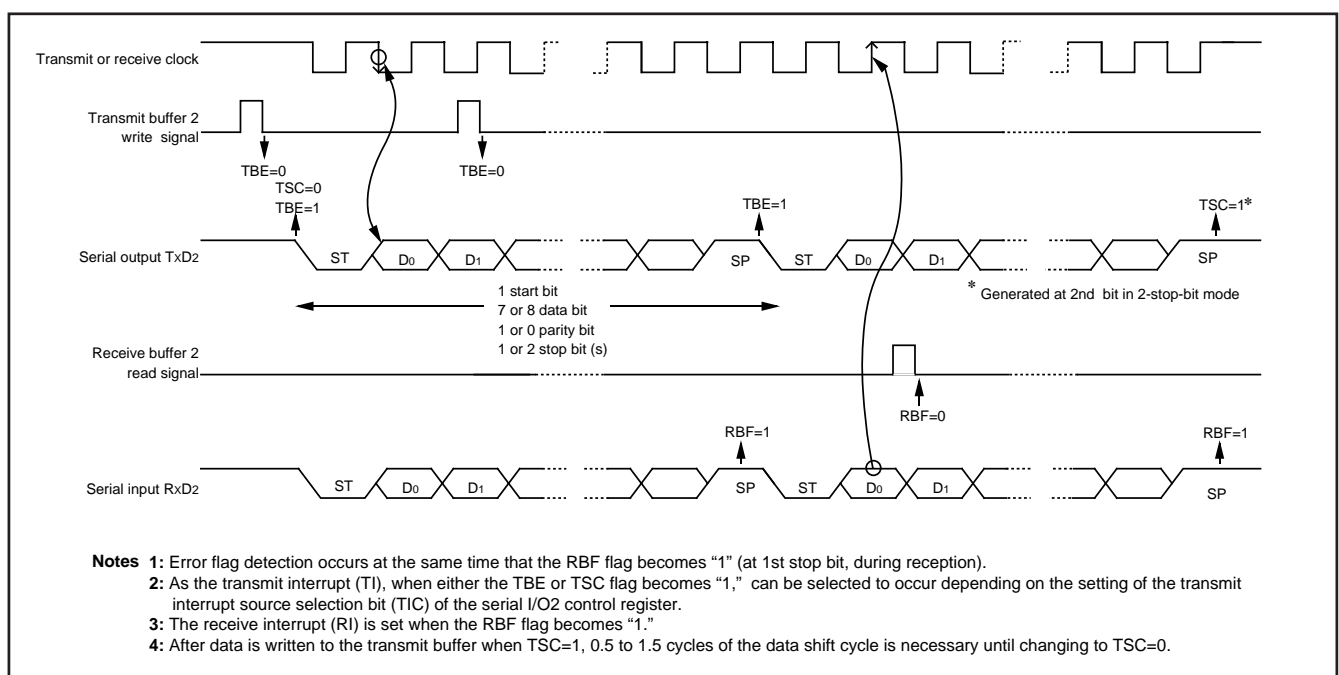


Fig. 63 Operation of UART serial I/O2 function

[Transmit buffer register 2/receive buffer register 2 (TB2/RB2)] 002E16

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O2 status register (SIO2STS)] 002F16

The read-only serial I/O2 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O2 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O2 enable bit SIOE (bit 7 of the serial I/O2 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O2 status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O2 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O2 control register (SIO2CON)] 003016

The serial I/O2 control register consists of eight control bits for the serial I/O2 function.

[UART2 control register (UART2CON)] 003116

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer.

[Baud rate generator 2 (BRG2)] 003216

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

■ Notes on Serial I/O2**• Serial I/O interrupt**

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- ① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ⑤ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

• I/O pin function when serial I/O2 is enabled.

The functions of P06 and P07 are switched with the setting values of a serial I/O2 mode selection bit and a serial I/O2 synchronous clock selection bit as follows.

(1) Serial I/O2 mode selection bit → "1" :

Clock synchronous type serial I/O is selected.

Setup of a serial I/O2 synchronous clock selection bit

"0" : P06 pin turns into an output pin of a synchronous clock.

"1" : P06 pin turns into an input pin of a synchronous clock.

Setup of a $\overline{\text{SRDY2}}$ output enable bit (SRDY)

"0" : P07 pin can be used as a normal I/O pin.

"1" : P07 pin turns into a $\overline{\text{SRDY2}}$ output pin.

(2) Serial I/O2 mode selection bit → "0" :

Clock asynchronous (UART) type serial I/O is selected.

Setup of a serial I/O2 synchronous clock selection bit

"0" : P06 pin can be used as a normal I/O pin.

"1" : P06 pin turns into an input pin of an external clock.

When clock asynchronous (UART) type serial I/O is selected, it is P07 pin. It can be used as a normal I/O pin.

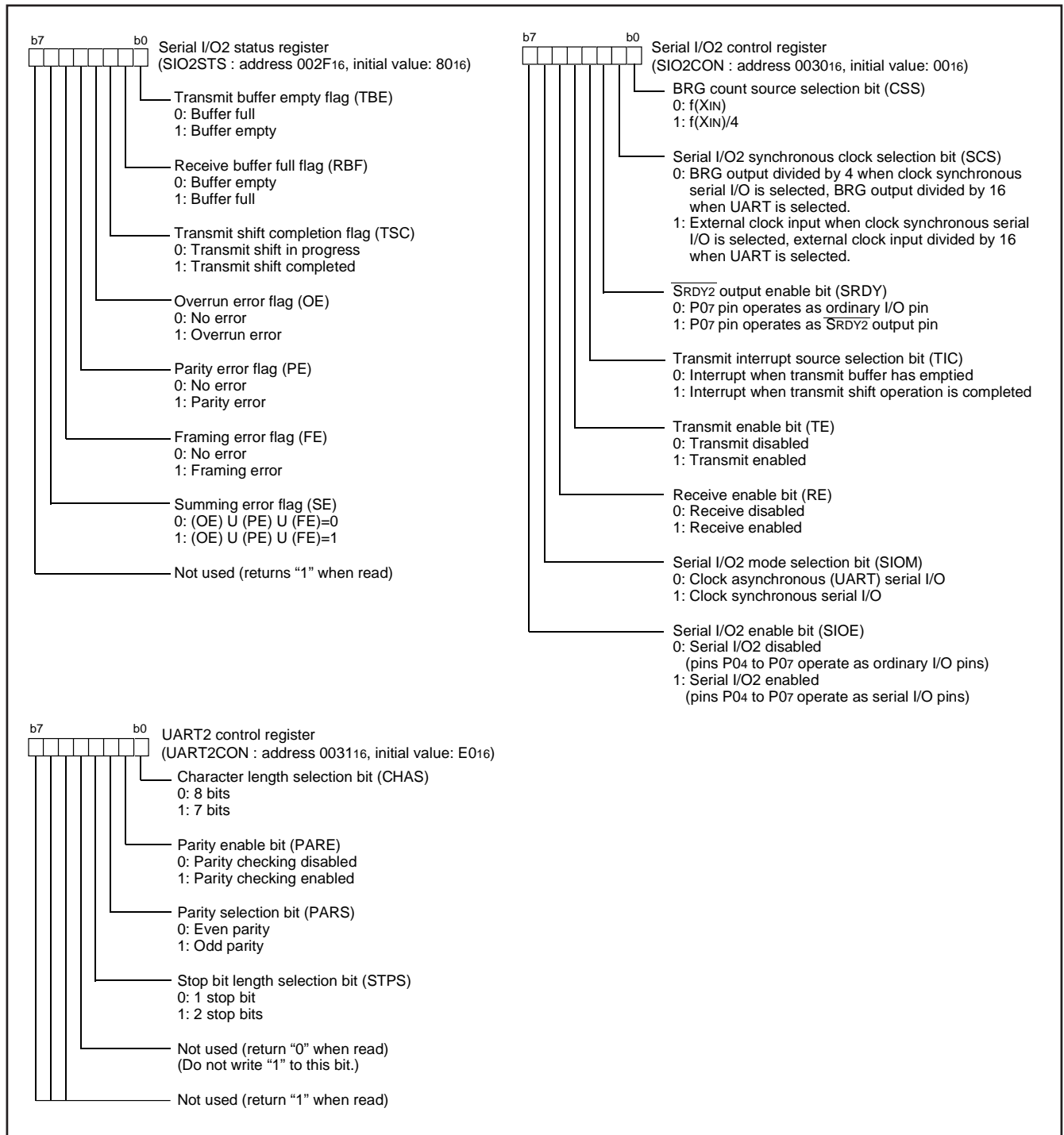


Fig. 64 Structure of serial I/O2-related registers

A/D Converter

The functional blocks of the A/D converter are described below.

[A/D conversion register] AD

The A/D conversion register is a read-only register that stores the result of A/D conversion. Do not read out this register during an A/D conversion.

[A/D control register] ADCON

The A/D control register controls the A/D converter.

Bit 2 to 0 are analog input pin selection bits.

Bit 3 is the A/D conversion clock selection bit. When "0" is set to this bit, the A/D conversion clock is $f(XIN)/2$ and the A/D conversion time is 122 cycles of $f(XIN)$. When "1" is set to this bit, the A/D conversion clock is $f(XIN)$ and the A/D conversion time is 61 cycles of $f(XIN)$.

Bit 4 is the A/D conversion completion bit. The value of this bit remains at "0" during A/D conversion, and changes to "1" at completion of A/D conversion.

A/D conversion is started by setting this bit to "0".

[Comparison voltage generator]

The comparison voltage generator divides the voltage between AVSS and VREF by 1024, and outputs the divided voltages.

[Channel selector]

The channel selector selects one of ports P25/AN5 to P20/AN0, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A/D conversion register. When A/D conversion is completed, the control circuit sets the A/D conversion completion bit and the A/D interrupt request bit to "1". Because the comparator is constructed linked to a capacitor, set $f(XIN)$ in order that the A/D conversion clock is 250 kHz or over during A/D conversion.

■ Notes on A/D converter

As for AD translation accuracy, on the following operating conditions, accuracy may become low.

- (1) Since the analog circuit inside a microcomputer becomes sensitive to noise when VREF voltage is set up lower than Vcc voltage, accuracy may become low rather than the case where VREF voltage and Vcc voltage are set up to the same value..
- (2) When VREF voltage is lower than [3.0 V], the accuracy at the low temperature may become extremely low compared with that at room temperature. When the system would be used at low temperature, the use at VREF=3.0 V or more is recommended.

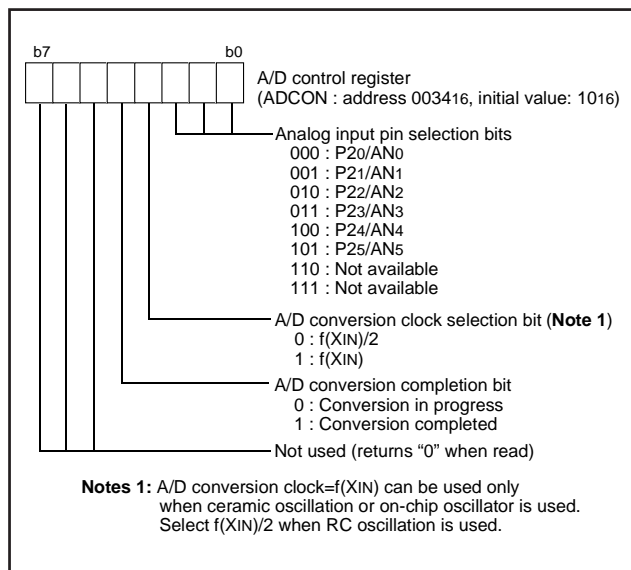


Fig. 65 Structure of A/D control register

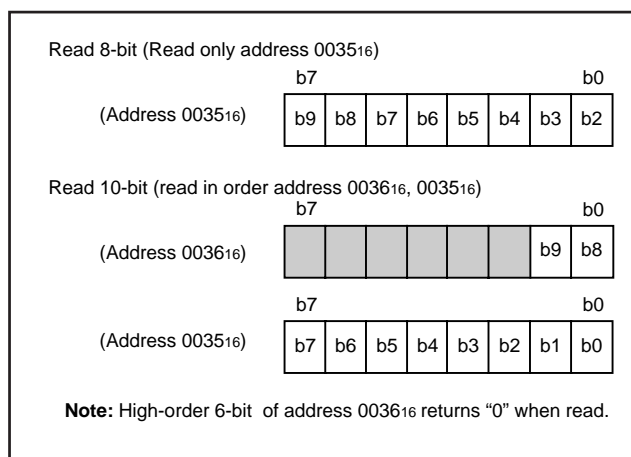
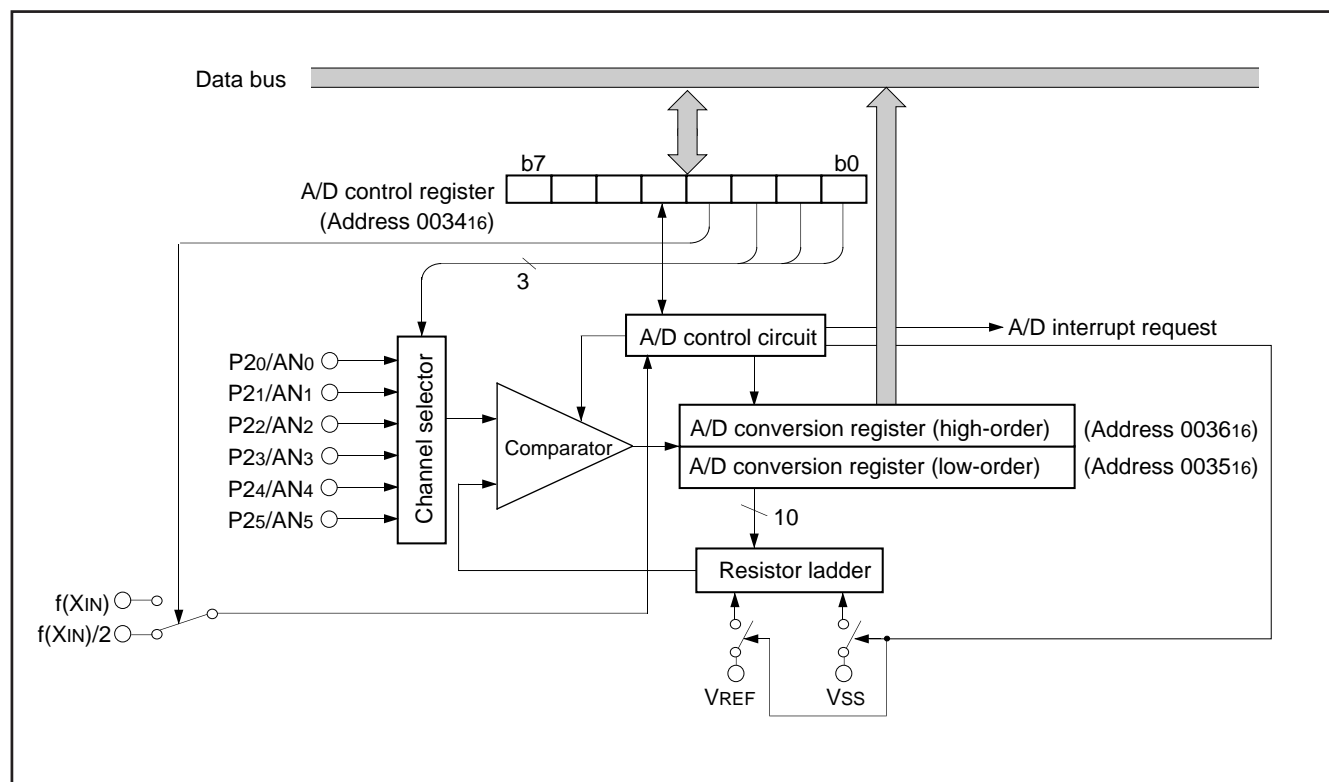


Fig. 66 Structure of A/D conversion register



Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

● Standard operation of watchdog timer

(1) Start of watchdog timer

The watchdog timer starts operating by setting value of the function set ROM data 2 (FSROM2: address 0FFA₁₆) or writing to the watchdog timer control register (WDTCN: address 0039₁₆).

Set "0" to the watchdog timer start selection bit (bit 1 of FSROM2) when operation starts by setting value of FSROM2. In this case, the watchdog timer starts operating after releasing reset.

Write an arbitrary value to WDTCN when FSROM2 is set to be invalid and operation starts by program. Operation by program can start even when "1" (stop state after releasing reset) is set to the watchdog timer start selection bit.

(2) Operation of watchdog timer

Watchdog timer L is set to "FF₁₆" and watchdog timer H is set to "FF₁₆" by reset or writing an arbitrary value to WDTCN.

When the watchdog timer starts operating, the selected clock is counted and internal reset occurs by the watchdog timer H underflow.

Accordingly, write to WDTCN before underflow by program.

When WDTCN is read, the values of the STP instruction function selection bit, watchdog timer H count source selection bit and the high-order 6 bits of the watchdog timer H are read.

(3) Count source clock of watchdog timer

The count source clock of the watchdog timer can be selected by the watchdog timer source clock selection bit (bit 0 of FSROM2).

If "0" is set to the watchdog timer source clock selection bit, the count source clock of the watchdog timer always is the on-chip oscillator output/16.

It changes by setting the clock division ratio selection bits (bit 7 and bit 6 of the CPU mode register) when "1" is set to the watchdog timer source clock selection bit or FSROM2 is set to be invalid.

When a double-speed mode, a high-speed mode, and a middle-speed mode are selected by the clock division ratio selection bits, the count source clock of the watchdog timer becomes $f(X_{IN})/16$. When the supply from on-chip oscillator is selected, it becomes the on-chip oscillator output/16.

(4) Watchdog timer H count source selection bit

The count source of watchdog timer H can be selected by FSROM2 or program.

When "0" is set to watchdog timer H count source selection bit (bit 2 of FSROM2), the watchdog timer L underflow signal is selected as the count source of watchdog timer H and the detection time is 131.072 ms at $f(X_{IN}) = 8$ MHz.

When "1" is set to this bit, the clock selected as the count source of watchdog timer L is input to watchdog timer H. In this case, the detection time is 512 μ s at $f(X_{IN}) = 8$ MHz.

When FSROM2 is set to be invalid, the count source of watchdog timer can be set by watchdog timer H count source selection bit (bit 7 of WDTCN).

When "0" is set to this bit, the watchdog timer L underflow signal is selected as the count source of watchdog timer H.

When "1" is set to this bit, the clock selected as the count source of watchdog timer L is input to watchdog timer H.

This bit is cleared to "0" after reset.

(5) STP instruction function selection bit

The function of the STP instruction can be selected by FSROM2 or program.

When "0" is set to the STP instruction function selection bit (bit 3 of FSROM2), system enters into the stop mode at the STP instruction execution.

When "1" is set to this bit, internal reset occurs at the STP instruction execution. When the function of the STP instruction is set by FSROM2, it cannot be changed by program.

When setting value of FSROM2 is invalid, the function of the STP instruction can be set by the STP instruction function selection bit (bit 6 of WDTCN).

When "0" is set to this bit, system enters into the stop mode at the STP instruction execution.

When "1" is set to this bit, internal reset occurs at the STP instruction execution.

Once this bit is set to "1", it cannot be changed to "0" by program.

This bit is cleared to "0" after reset.

■ Notes on watchdog timer

1. The watchdog timer is operating during the wait mode. Write data to the watchdog timer control register to prevent timer underflow.
2. The watchdog timer stops during the stop mode. However, the watchdog timer is running during the oscillation stabilizing time after the **STP** instruction is released. In order to avoid the underflow of the watchdog timer, the watchdog timer count source selection bit (bit 7 of watchdog timer control register (address 39₁₆)) before executing the **STP** instruction.
3. The **STP** instruction function selection bit (bit 6 of watchdog timer control register (address 39₁₆)) can be rewritten only once after releasing reset. After rewriting it is disable to write any data to this bit.

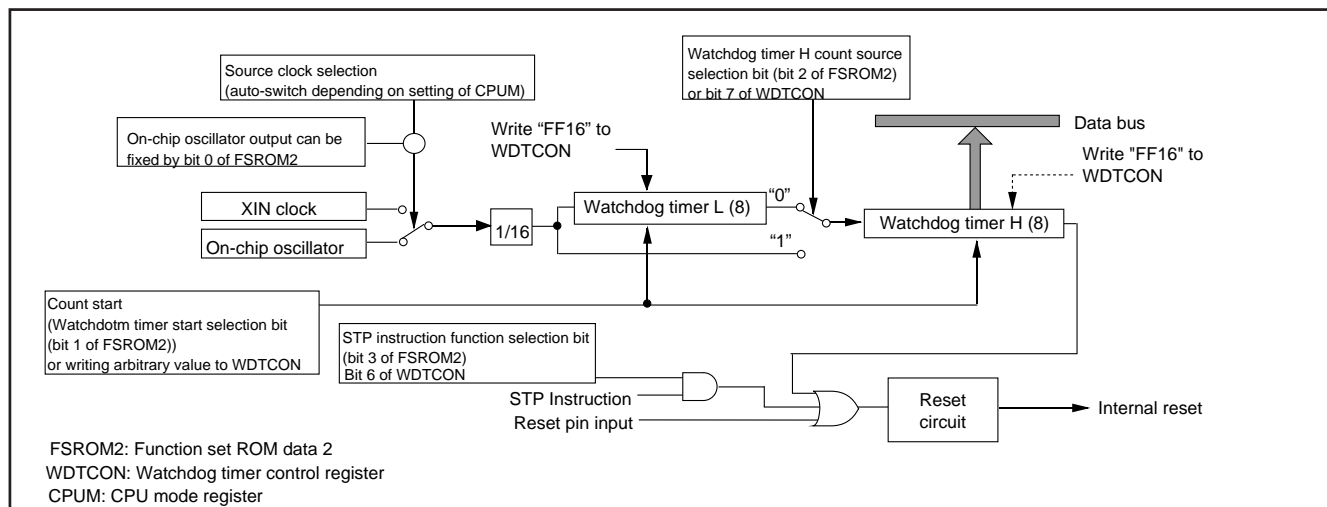


Fig. 68 Block diagram of watchdog timer

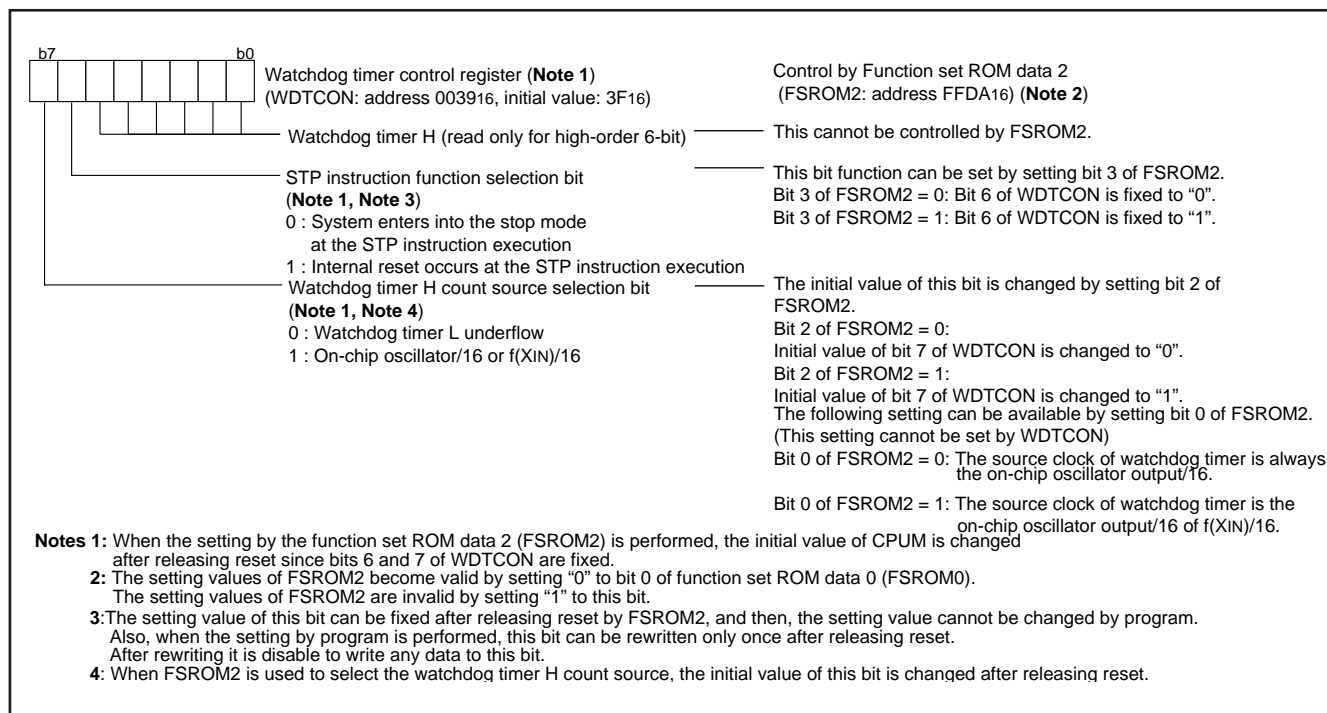


Fig. 69 Structure of watchdog timer control register

Power-on Reset Circuit

Reset can be automatically performed at power on (power-on reset) by the built-in power-on reset circuit.

In order to use the power-on reset circuit effectively, the time for the supply voltage to rise from 0 V to 1.8 V must be set to 1 ms or less.

When the built-in power-on reset circuit is used, pull-up the RESET pin to VCC.

Low Voltage Detection Circuit

The built-in low voltage detection circuit is designed to detect a drop in voltage and to reset the microcomputer if the power source voltage drops below a set value (Typ.1.90 V).

The low voltage detection circuit is valid by setting "1" to bit 1 of the function set ROM data 0.

Also, when "1" is set to bit 3 of the function set ROM data 0, the low voltage detection circuit can be valid even in the stop mode.

The low voltage detection circuit is stopped in the stop mode by setting "0" to this bit, so that the power dissipation is reduced.

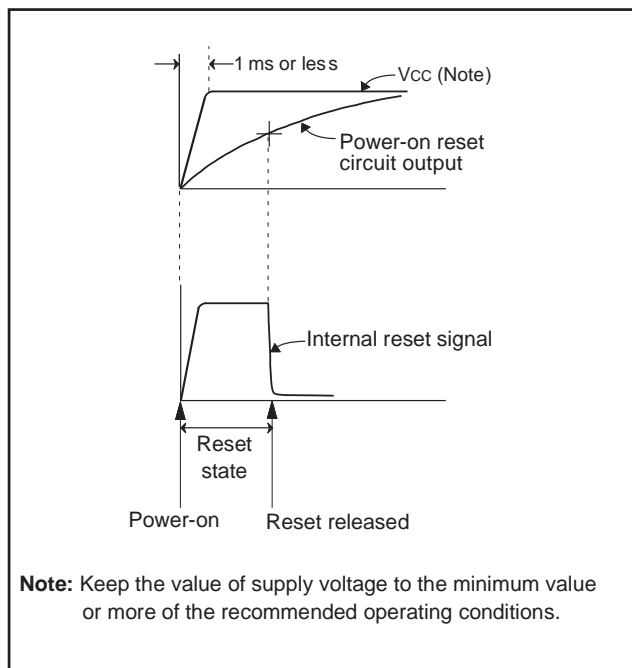


Fig. 70 Operation waveform diagram of power-on reset circuit

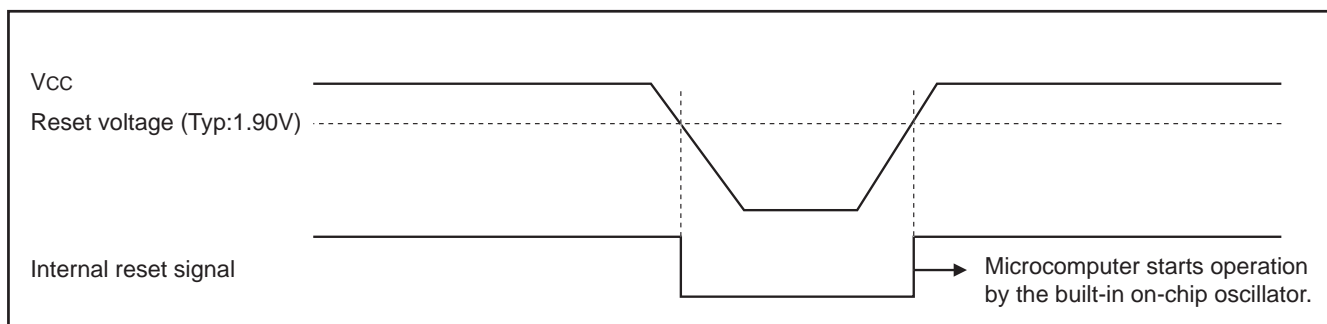


Fig. 71 Operation waveform diagram of low voltage detection circuit

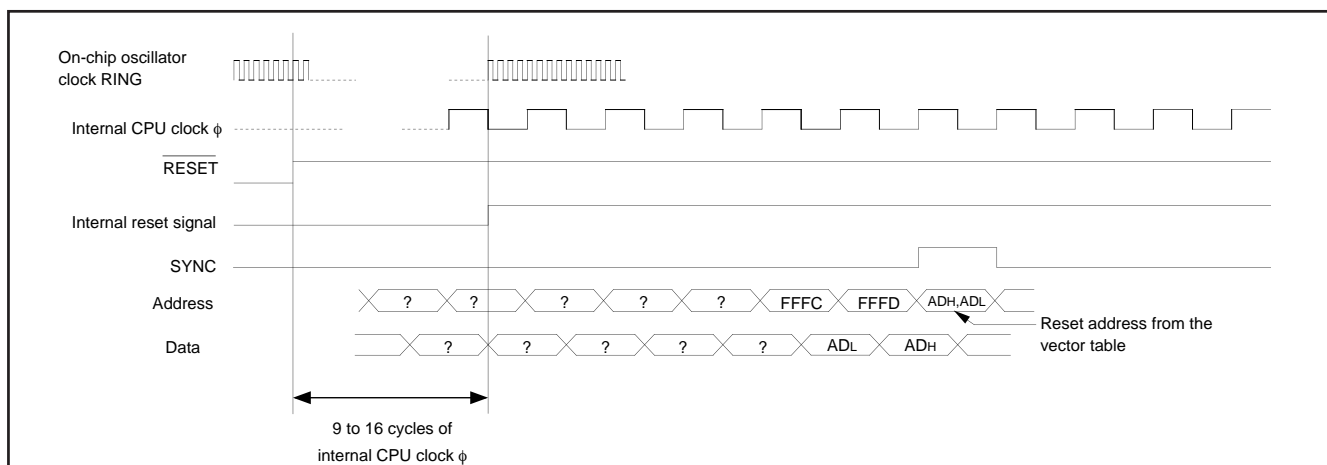


Fig. 72 Timing diagram at reset

| | Address | Register contents |
|---|--------------------|--|
| (1) Port P0 direction register (P0D) | 0001 ₁₆ | 00 ₁₆ |
| (2) Port P1 direction register (P1D) | 0003 ₁₆ | X X X 0 0 0 0 0 |
| (3) Port P2 direction register (P2D) | 0005 ₁₆ | 00 ₁₆ |
| (4) Port P3 direction register (P3D) | 0007 ₁₆ | 00 ₁₆ |
| (5) Interrupt source set register (INTSET) | 000A ₁₆ | 00 ₁₆ |
| (6) Interrupt source discrimination register (INTDIS) | 000B ₁₆ | 00 ₁₆ |
| (7) Compare register (low-order) (CMPL) | 0010 ₁₆ | 00 ₁₆ |
| (8) Compare register (high-order) (CMPH) | 0011 ₁₆ | 00 ₁₆ |
| (9) Capture/Compare register R/W pointer (CCRP) | 0012 ₁₆ | 00 ₁₆ |
| (10) Capture software trigger register (CSTR) | 0013 ₁₆ | 00 ₁₆ |
| (11) Compare register re-load register (CMPR) | 0014 ₁₆ | 00 ₁₆ |
| (12) Port P0P3 drive capacity control register (DCCR) | 0015 ₁₆ | 00 ₁₆ |
| (13) Pull-up control register (PULL) | 0016 ₁₆ | 00 ₁₆ |
| (14) Port P1P3 control register (P1P3C) | 0017 ₁₆ | 00 ₁₆ |
| (15) Serial I/O1 status register (SIO1STS) | 0019 ₁₆ | 1 0 0 0 0 0 0 0 |
| (16) Serial I/O1 control register (SIO1CON) | 001A ₁₆ | 00 ₁₆ |
| (17) UART1 control register (UART1CON) | 001B ₁₆ | 1 1 1 0 0 0 0 0 |
| (18) Timer A, B mode register (TABM) | 001D ₁₆ | 00 ₁₆ |
| (19) Capture/Compare port register (CCPR) | 001E ₁₆ | 00 ₁₆ |
| (20) Timer source selection register (TMSR) | 001F ₁₆ | 00 ₁₆ |
| (21) Capture mode register (CAPM) | 0020 ₁₆ | 00 ₁₆ |
| (22) Compare output mode register (CMOM) | 0021 ₁₆ | 00 ₁₆ |
| (23) Capture/Compare status register (CCSR) | 0022 ₁₆ | 00 ₁₆ |
| (24) Compare interrupt source register (CISR) | 0023 ₁₆ | 00 ₁₆ |
| (25) Timer A (low-order) (TAL) | 0024 ₁₆ | FF ₁₆ |
| (26) Timer A (high-order) (TAH) | 0025 ₁₆ | FF ₁₆ |
| (27) Timer B (low-order) (TBL) | 0026 ₁₆ | FF ₁₆ |
| (28) Timer B (high-order) (TBH) | 0027 ₁₆ | FF ₁₆ |
| (29) Prescaler 1 (PRE1) | 0028 ₁₆ | FF ₁₆ |
| (30) Timer 1 (T1) | 0029 ₁₆ | 01 ₁₆ |
| (31) Timer count source set register (TCSS) | 002A ₁₆ | 00 ₁₆ |
| (32) Timer X mode register (TXM) | 002B ₁₆ | 00 ₁₆ |
| (33) Prescaler X (PREX) | 002C ₁₆ | FF ₁₆ |
| (34) Timer X (TX) | 002D ₁₆ | FF ₁₆ |
| (35) Serial I/O2 control register (SIO2STS) | 002F ₁₆ | 1 0 0 0 0 0 0 0 |
| (36) Serial I/O2 register (SIO2CON) | 0030 ₁₆ | 00 ₁₆ |
| (37) UART2 control register (UART2CON) | 0031 ₁₆ | 1 1 1 0 0 0 0 0 |
| (38) A/D control register (ADCON) | 0034 ₁₆ | 0 0 0 1 0 0 0 0 |
| (39) On-chip oscillation division ratio selection register (RODR) | 0037 ₁₆ | 0 0 0 0 0 0 0 1 |
| (40) MISRG | 0038 ₁₆ | 00 ₁₆ |
| (41) Watchdog timer control register (WDTCON) (Note 3) | 0039 ₁₆ | 0 0 1 1 1 1 1 1 |
| (42) Interrupt edge selection register (INTEDGE) | 003A ₁₆ | 00 ₁₆ |
| (43) CPU mode register (CPUM) (Note 3) | 003B ₁₆ | 1 0 0 0 0 0 0 0 |
| (44) Interrupt request register 1 (IREQ1) | 003C ₁₆ | 00 ₁₆ |
| (45) Interrupt request register 2 (IREQ2) | 003D ₁₆ | 00 ₁₆ |
| (46) Interrupt control register 1 (ICON1) | 003E ₁₆ | 00 ₁₆ |
| (47) Interrupt control register 2 (ICON2) | 003F ₁₆ | 00 ₁₆ |
| (48) Processor status register | (PS) | X X X X X 1 X X |
| (49) Program counter | (PC _H) | Contents of address FFFD ₁₆ |
| | (PC _L) | Contents of address FFFC ₁₆ |
| (50) Watchdog timer H | | FF ₁₆ |
| (51) Watchdog timer L | | FF ₁₆ |

Notes 1: X : Undefined

2: The content of other registers is undefined when the microcomputer is reset.
The initial values must be surely set before you use it.

3: When the setting by the function set ROM data 2 (FSROM2) is performed,
the initial values of these registers at reset are changed.

Fig. 73 Internal status of microcomputer at reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.

Use the circuit constants in accordance with the resonator manufacturer's recommended values.

No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.)

(1) On-chip oscillator operation

When the MCU operates by the on-chip oscillator for the main clock, connect XIN pin to VCC through a resistor and leave XOUT pin open.

The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.

Be careful that variable frequencies when designing application products.

(2) Ceramic resonator

When the ceramic resonator is used for the main clock, connect the ceramic resonator and the external circuit to pins XIN and XOUT at the shortest distance. A feedback resistor is built in between pins XIN and XOUT.

(3) RC oscillation

When the RC oscillation is used for the main clock, connect the XIN pin and XOUT pin to the external circuit of resistor R and the capacitor C at the shortest distance.

The frequency is affected by a capacitor, a resistor and a micro-computer.

So, set the constants within the range of the frequency limits.

(4) External clock

When the external signal clock is used for the main clock, connect the XIN pin to the clock source and leave XOUT pin open.

Select "0" (ceramic oscillation) to oscillation mode selection bit of CPU mode register (003B16).

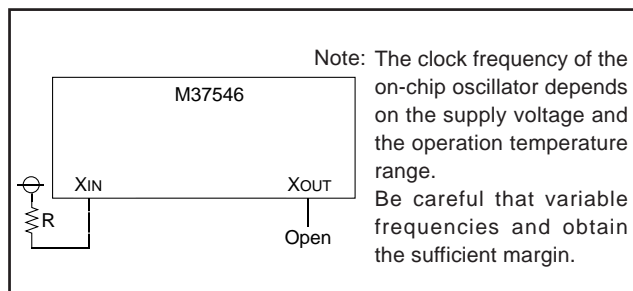


Fig. 74 Processing of XIN and XOUT pins at on-chip oscillator operation

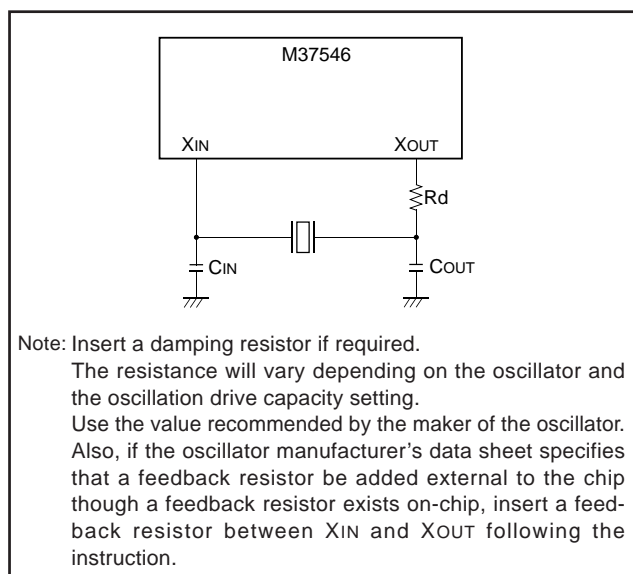


Fig. 75 External circuit of ceramic resonator

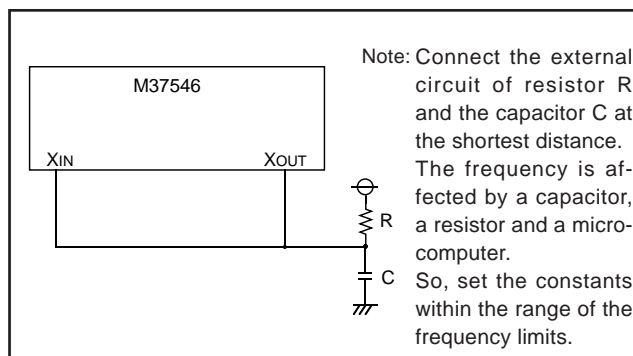


Fig. 76 External circuit of RC oscillation

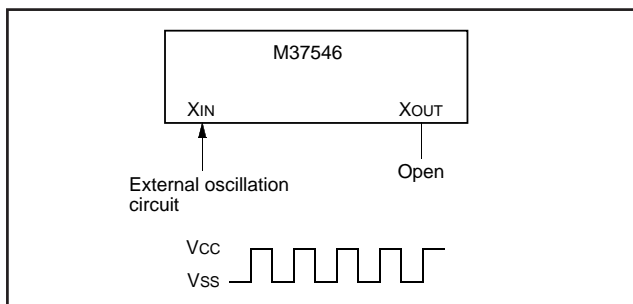


Fig. 77 External clock input circuit

- **Stop mode**

- **Wait mode**

If the WIT instruction is executed, the internal clock ϕ stops at an “H” level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to “1” before the STP or WIT instruction is executed.

■ Notes on Clock Generating Circuit

- Switch of ceramic and RC oscillations

After releasing reset the operation starts by starting an on-chip oscillator. Then, a ceramic oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

- Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

- CPU mode register

Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU "M37542RSS" is excluded.)

Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

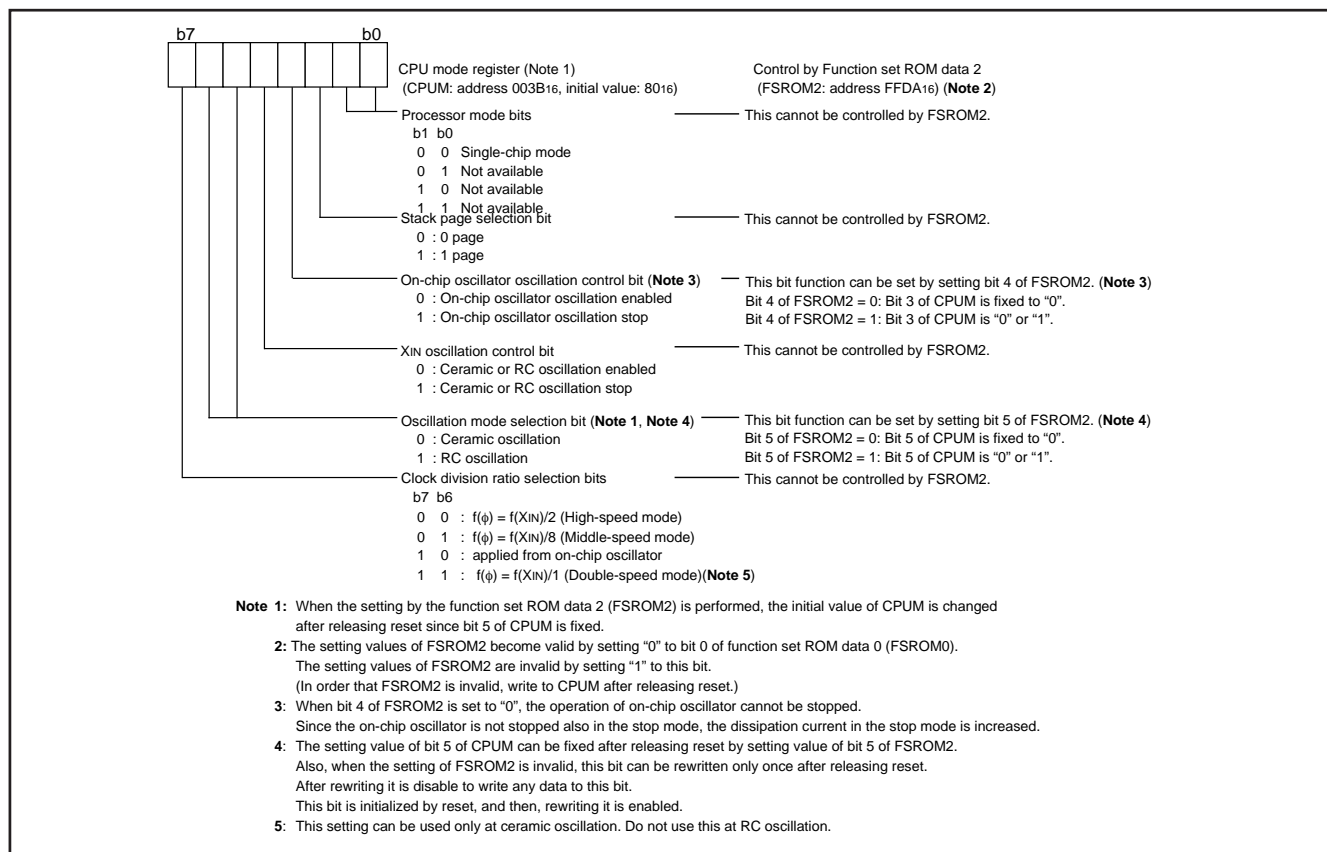


Fig. 78 Structure of CPU mode register

- Clock division ratio, XIN oscillation control, on-chip oscillator control

The state transition shown in Fig. 82 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), on-chip oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 82.

- Count source (Timer 1, Timer A, Timer B, Timer X, Serial I/O, Serial I/O2, A/D converter, Watchdog timer)

The count sources of these functions are affected by the clock division selection bit of the CPU mode register.

The $f(XIN)$ clock is supplied to the watchdog timer when selecting $f(XIN)$ as the CPU clock.

The on-chip oscillator output is supplied to these functions when selecting the on-chip oscillator output as the CPU clock.

However, the watchdog timer is also affected by the function set ROM.

● On-chip oscillation division ratio

At on-chip oscillator mode, division ratio of on-chip oscillator for CPU clock is selected by setting value of on-chip oscillation division ratio selection register. The division ratio of on-chip oscillation for CPU clock is selected from among 1/1, 1/2, 1/8, 1/128. The operation clock for the peripheral function block is not changed by setting value of this register.

■ Notes on On-chip Oscillation Division Ratio

- When system is released from reset, ROSC/8 (on-chip oscillator middle-speed mode) is selected for CPU clock.
- When state transition from the ceramic or RC oscillation to on-chip oscillator, ROSC/8 (on-chip oscillator middle-speed mode) is selected for CPU clock.
- When the MCU operates by on-chip oscillator for the main clock without external oscillation circuit, connect XIN pin to VCC through a resistor and leave XOUT pin open.
Set "10010x002" (x = 0 or 1) to CPUM.

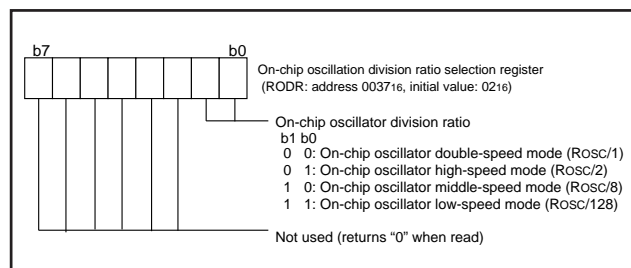


Fig. 79 Structure of on-chip oscillation division ratio selection register

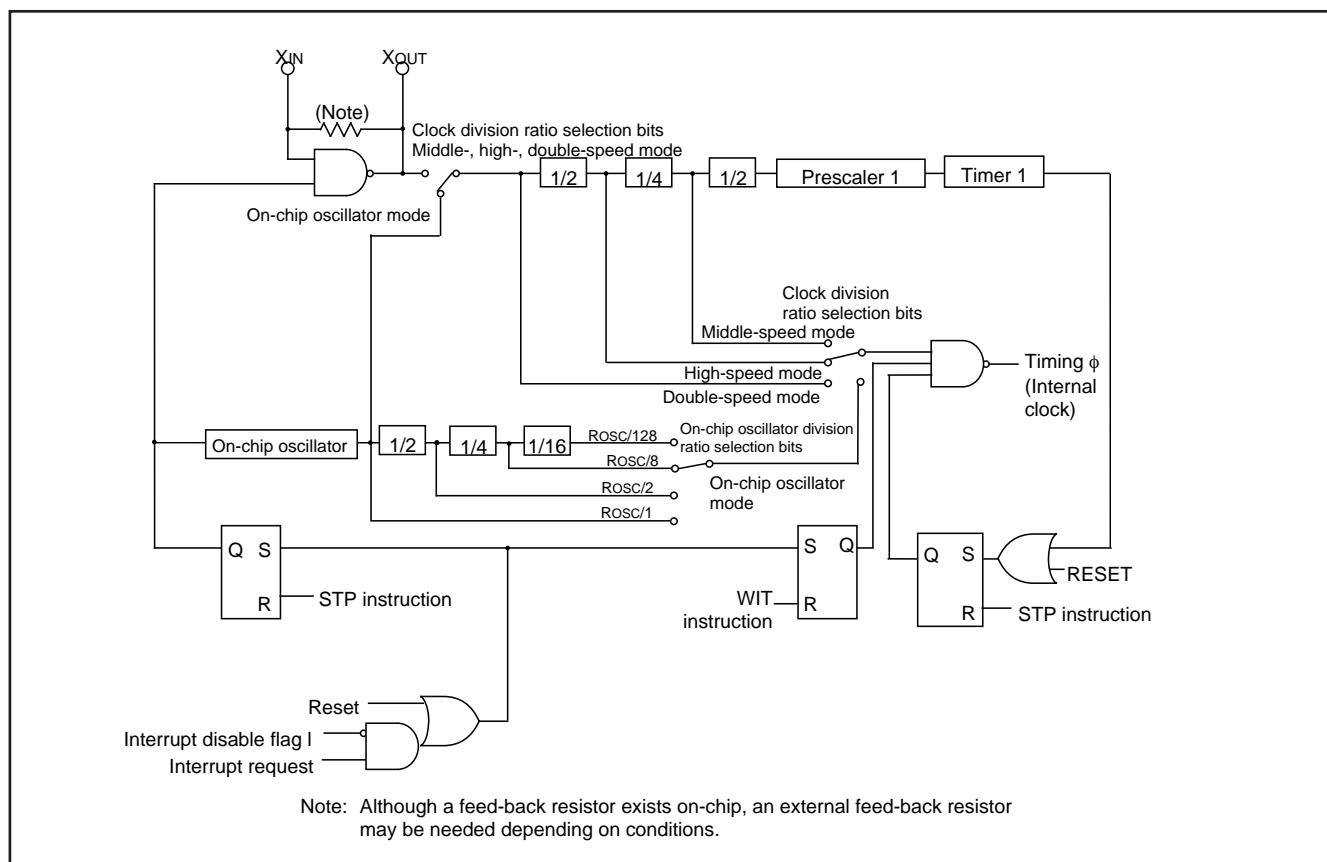


Fig. 80 Block diagram of internal clock generating circuit (for ceramic resonator)

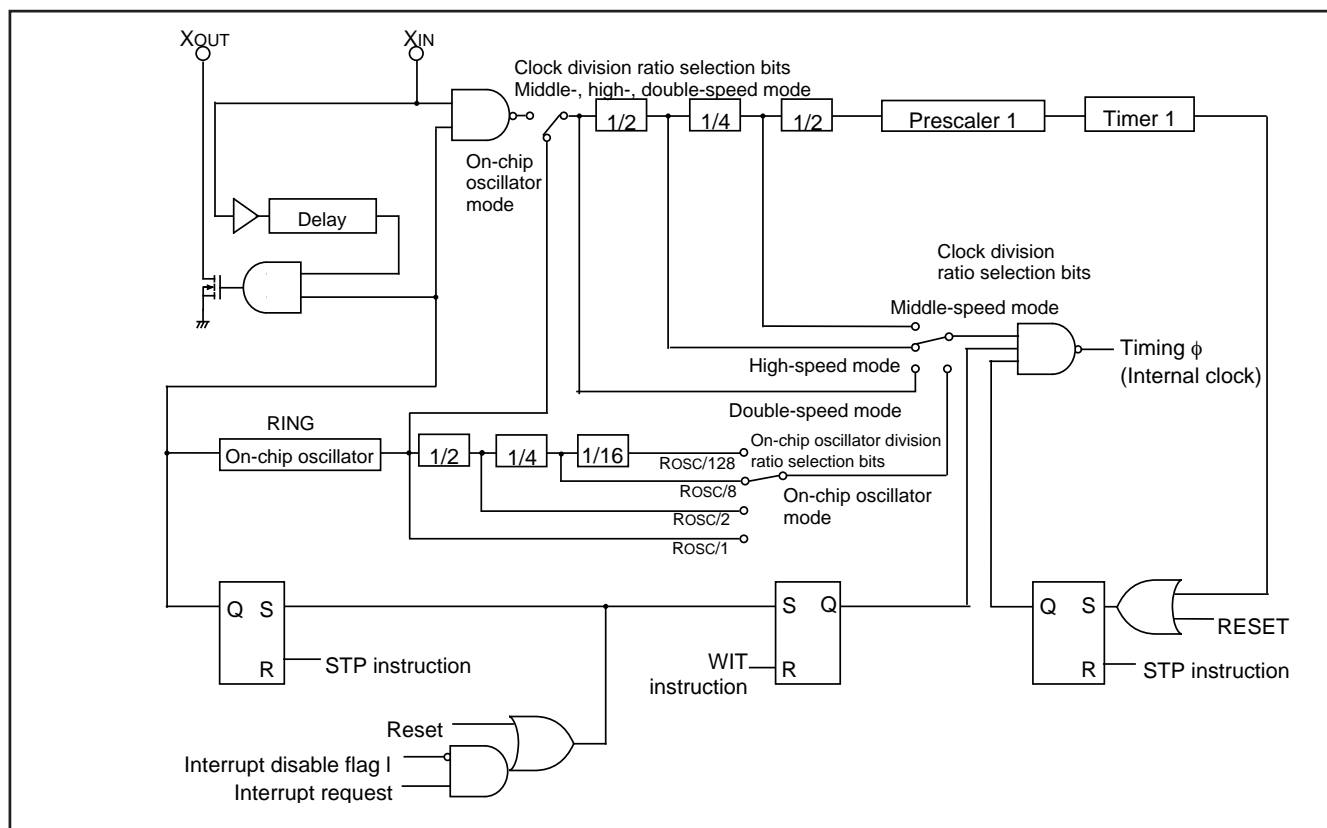
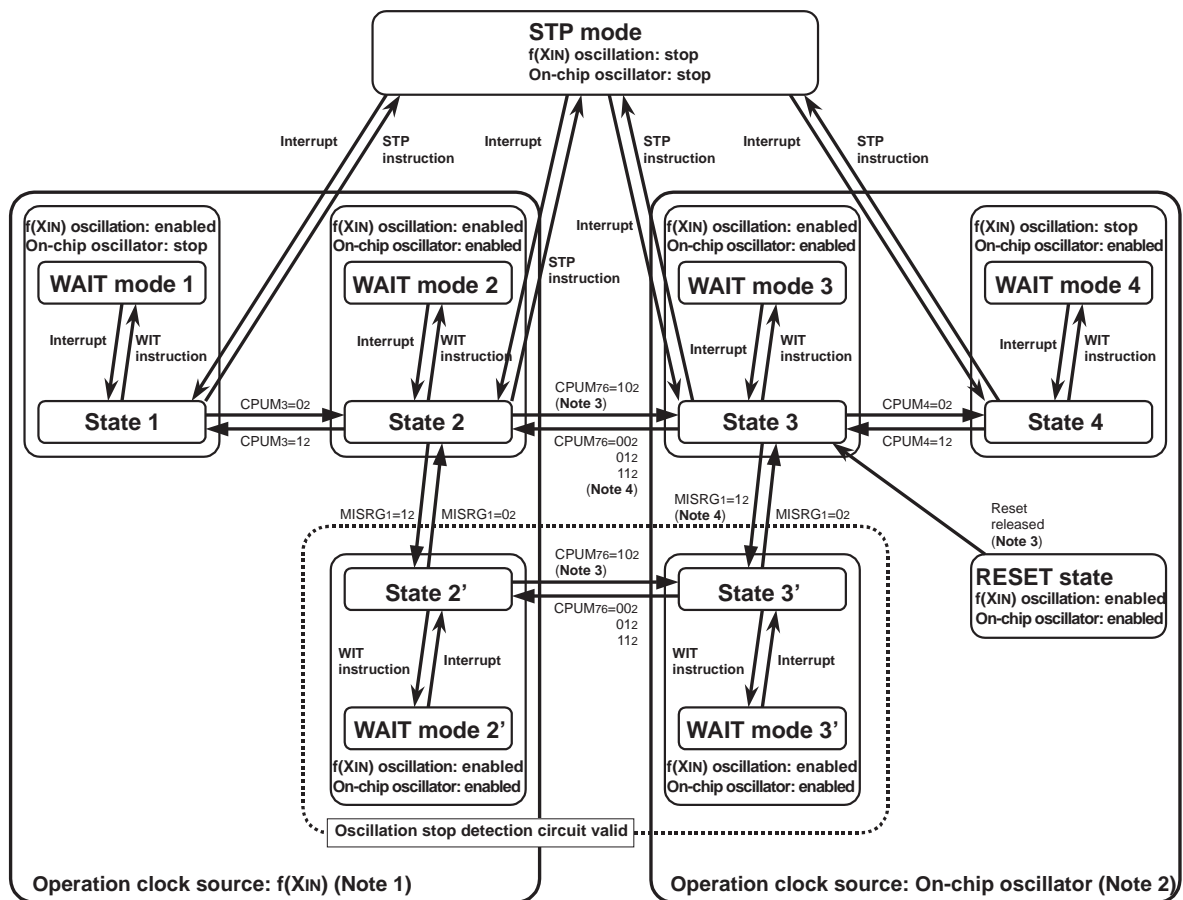


Fig. 81 Block diagram of internal clock generating circuit (for RC oscillation)



Notes on switch of clock

- (1) In operation clock = $f(XIN)$, the following can be selected for the CPU clock division ratio.
 - $f(XIN)/2$ (high-speed mode)
 - $f(XIN)/8$ (middle-speed mode)
 - $f(XIN)$ (double-speed mode, only at a ceramic oscillation)
- (2) In operation clock = On-chip oscillator, the following can be selected for the CPU clock division ratio.
 - ROSC/1 (On-chip oscillator double-speed mode)
 - ROSC/2 (On-chip oscillator high-speed mode)
 - ROSC/8 (On-chip oscillator middle-speed mode)
 - ROSC/128 (On-chip oscillator low-speed mode)
- (3) After system is released from reset, and state transition of state 2 → state 3 and state transition of state 2' → state 3', ROSC/8 (On-chip oscillator middle-speed mode) is selected for CPU clock.
- (4) Executing the state transition state 3 to 2 or state 3' to 2' after stabilizing XIN oscillation.
- (5) When the state 2 → state 3 → state 4 is performed, execute the NOP instruction as shown below according to the division ratio of CPU clock.
 1. CPUM76 = 102 (state 2 → state 3)
 2. NOP instruction
 - Transition from Double-speed mode: NOP × 3
 - Transition from High-speed mode: NOP × 1
 - Transition from Middle-speed mode: NOP × 0
 3. CPU4 = 12 (state 3 → state 4)
- (6) When the state 3 → state 2 → state 1 is performed, execute the NOP instruction as shown below according to the division ratio of CPU clock.
 1. CPUM76 = 002 or 012 or 112 (state 3 → state 2)
 2. NOP instruction
 - Transition from On-chip oscillator double-speed mode: NOP × 4
 - Transition from On-chip oscillator high-speed mode: NOP × 2
 - Transition from On-chip oscillator middle-speed mode: NOP × 0
 - Transition from On-chip oscillator low-speed mode: NOP × 0
 3. CPUM3 = 12 (state 2 → state 1)

Fig. 82 State transition

● Oscillation stop detection circuit

The oscillation stop detection circuit is used for reset occurrence when a ceramic resonator or RC oscillation circuit stops by disconnection. To use this circuit, set an on-chip oscillator to be in active.

The oscillation stop detection circuit is in active to set "1" to the ceramic or RC oscillation stop detection function active bit. When the oscillation stop detection circuit is in active, ceramic or RC oscillation is watched by the on-chip oscillator. When stop of ceramic or RC oscillation is detected, the oscillation stop detection status bit is set to "1". While "1" is set to the oscillation stop reset bit, internal reset occurs when oscillation stop is detected.

The external reset and the oscillation stop reset can be discriminated by reading the oscillation stop detection status bit.

The oscillation stop detection status bit retains "1", not initialized, when the oscillation stop reset occurs. The oscillation stop detection status bit is initialized to "0" when the external reset occurs. Accordingly, reset by oscillation stop can be confirmed by using this flag.

■ Notes on Oscillation Stop Detection Circuit

- Do not execute the transition to "state 2'a" shown in Fig. 84 because in this "state 2'a", MCU is stopped without reset even when XIN oscillation is stopped.
- Ceramic or RC oscillation stop detection function active bit is not cleared by the oscillation stop internal reset. Accordingly, the oscillation stop detection circuit is in active when system is released from internal reset cause of oscillation stop detection.
- Oscillation stop detection status bit is initialized by the following operation.
 - (1) External reset
 - (2) Write "0" data to the ceramic or RC oscillation stop detection function active bit.
- The oscillation stop detection circuit is not included in the emulator MCU "M37542RSS".

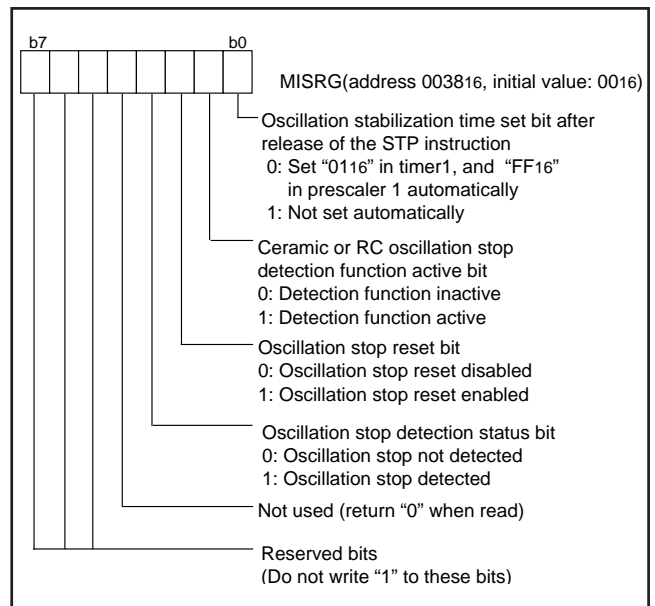
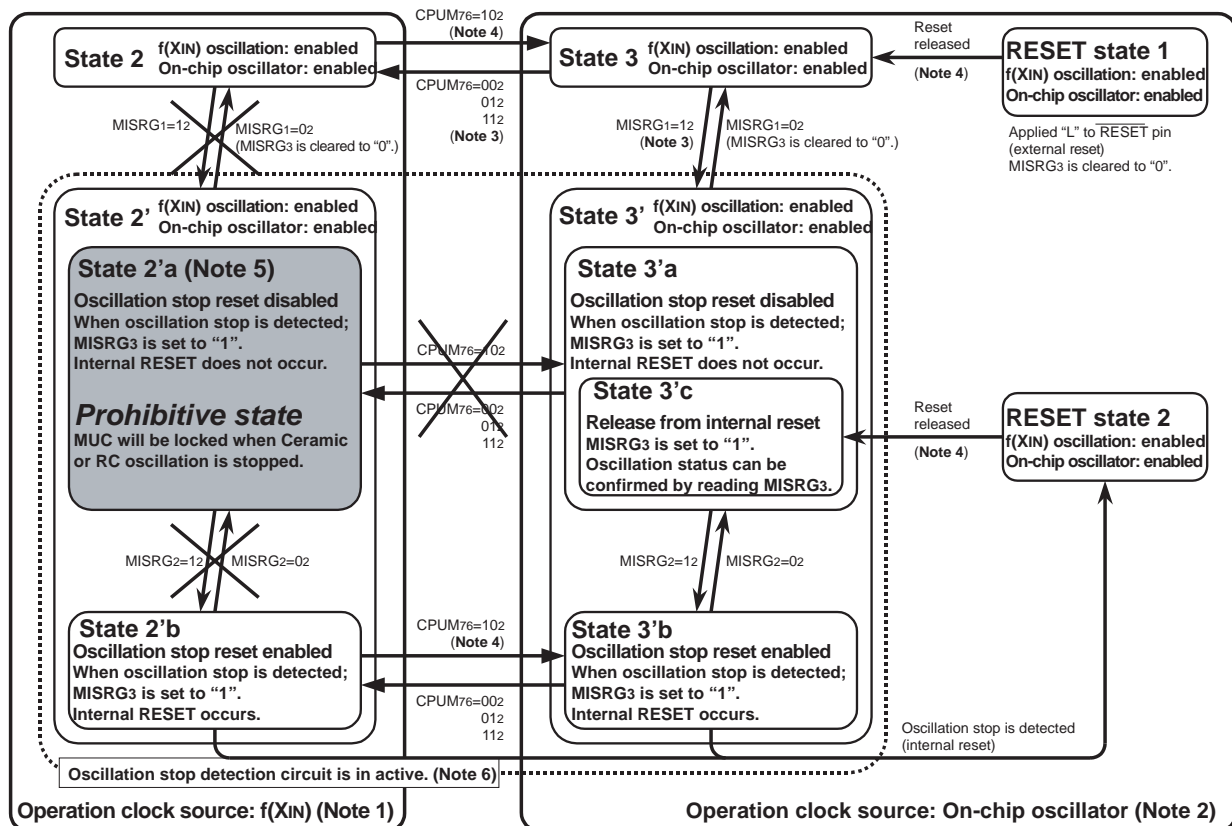


Fig. 83 Structure of MISRG



Notes on switch of clock

- (1) In operation clock = $f(XIN)$, the following can be selected for the CPU clock division ratio.
 $f(XIN)/2$ (High-speed mode)
 $f(XIN)/8$ (Middle-speed mode)
 $f(XIN)$ (Double-speed mode, only at a ceramic oscillation)
- (2) In operation clock = On-chip oscillator, the following can be selected for the CPU clock division ratio.
 ROSC/1 (On-chip oscillator double-speed mode)
 ROSC/2 (On-chip oscillator high-speed mode)
 ROSC/8 (On-chip oscillator middle-speed mode)
 ROSC/128 (On-chip oscillator low-speed mode)
- (3) Executing the state transition state 3 to 2 or state 3 to 3' after stabilizing XIN oscillation.
- (4) After system is released from reset, and state transition of state 2 → state 3 and state transition of state 2' → state 3',
 Rosc/8 (On-chip oscillator middle-speed mode) is selected for CPU clock.
- (5) MCU cannot be returned by On-chip oscillator and its operation is stopped since internal reset does not occur at oscillation stop detected.
 Accordingly, do not execute the transition to state 2'a.
- (6) STP instruction cannot be used when oscillation stop detection circuit is in active.

Fig. 84 State transition 2

● Function set ROM

Fig. 85 shows the Assignment of Function set ROM area.

The random data are written to the Renesas shipment test areas (addresses FFD4₁₆ to address FFD7₁₆).

Do not rewrite the data of these areas.

When the checksum is included in the user program, avoid assigning it to these areas.

The function set ROM data 0 to 2 (addresses FFD8₁₆ to FFDA₁₆) are used to set the peripheral function.

Data set to these areas become valid after releasing reset.

The ROM code protect to disable the reading of the built-in QzROM area is assigned to address FFDB₁₆.

[Function set ROM data] FSR0M0, FSR0M1, FSR0M2

Function set ROM data 0 to 2 (addresses FFD8₁₆ to FFDA₁₆) are used to set modes of peripheral functions.

By setting values to these areas, the operation mode of each peripheral function are set after releasing reset.

Refer to the descriptions of peripheral functions for the details of operation of peripheral functions.

- CPU mode register

- Watchdog timer

- Low voltage detection circuit

When "1" is set to bit 0 of function set ROM data 0 (address FFD8₁₆), the written values to bit 5 to bit 0 of function set ROM data 2 (address FFDA₁₆) can become invalid.

When the values of bit 5 to bit 0 of function set ROM data 2 (address FFDA₁₆) are invalid, the operation mode of the peripheral functions can be set by setting the related registers.

[ROM code protect]

By setting "00₁₆" to ROM code protect (address FFDB₁₆), reading of the built-in QzROM by the serial programmer is disabled.

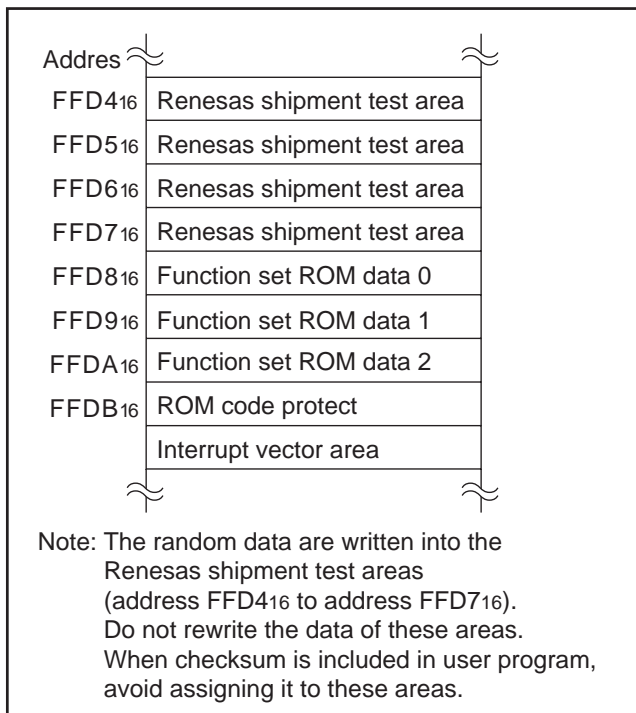


Fig. 85 Assignment of Function set ROM area

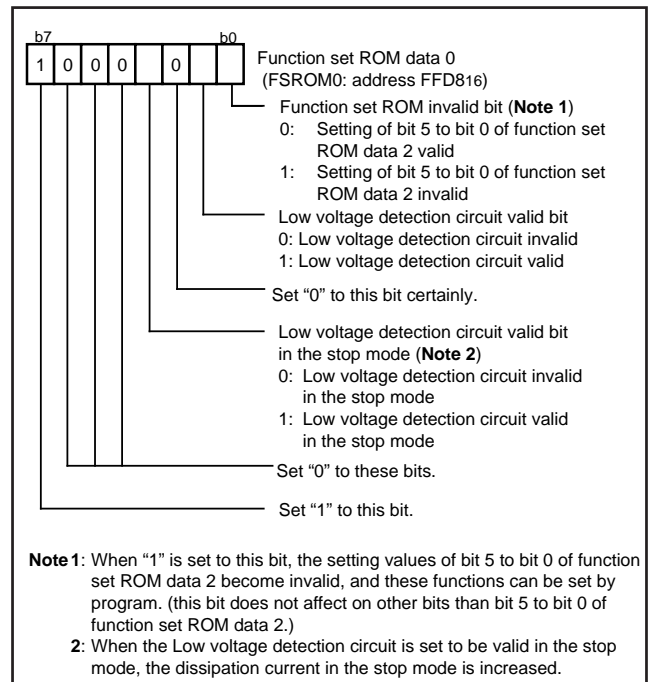


Fig. 86 Structure of Function set ROM data 0

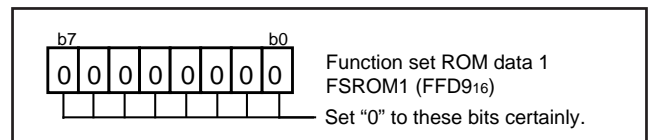


Fig. 87 Structure of Function set ROM data 1

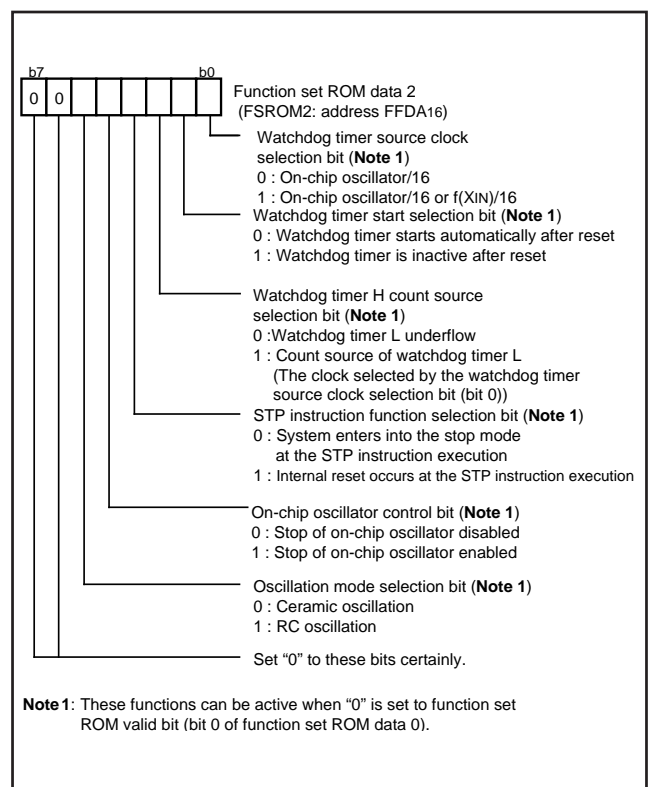


Fig. 88 Structure of Function set ROM data 2

QzROM Writing Mode

In the QzROM writing mode, the user ROM area can be rewritten while the microcomputer is mounted on-board by using a serial programmer which is applicable for this microcomputer.

Table 9 lists the pin description (QzROM writing mode) and Fig. 89, Fig. 90 and Fig. 91 show the pin connections.

Refer to Fig. 92 and Fig. 93 for example of a connection with a serial programmer.

Contact the manufacturer of your serial programmer for serial programmer . Refer to the user's manual of your serial programmer for details on how to use it.

Table 9 Pin description (QzROM writing mode)

| Pin | Name | I/O | Function |
|---|--------------------------|--------|--|
| VCC, VSS | Power source | Input | •Apply 1.8 to 5.5V to VCC, and 0V to VSS. |
| RESET | Reset input | Input | •Reset input pin for active "L". Reset occurs when RESET pin is hold at an "L" level for 16 cycles or more of XIN. |
| XIN | Clock input | Input | •Set the same termination as the single-chip mode. |
| XOUT | Clock output | Output | |
| VREF | Analog reference voltage | Input | •Input the reference voltage of A/D converter to VREF. |
| P00–P07 P13–P14 P20–P25 P30–P34, P37 | I/O port | I/O | •Input "H" or "L" level signal or leave the pin open. |
| CNVSS | VPP input | Input | •QzROM programmable power source pin. |
| P11 | ESDA input/output | I/O | •Serial data I/O pin. |
| P12 | ESCLK input | Input | •Serial clock input pin. |
| P10 | ESPGMB input | Input | •Read/program pulse input pin. |

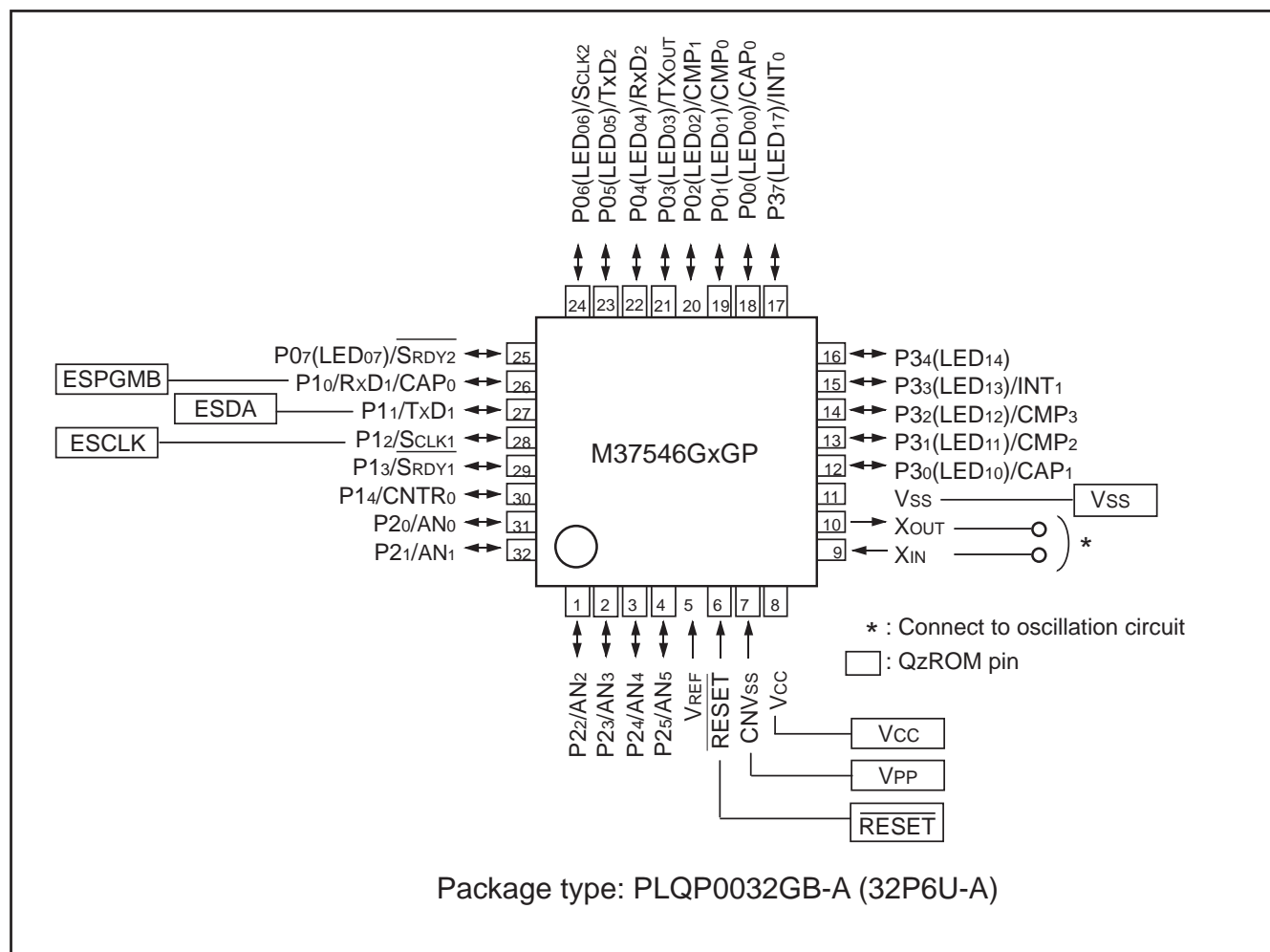


Fig. 89 Pin connection diagram (M37546GxGP)

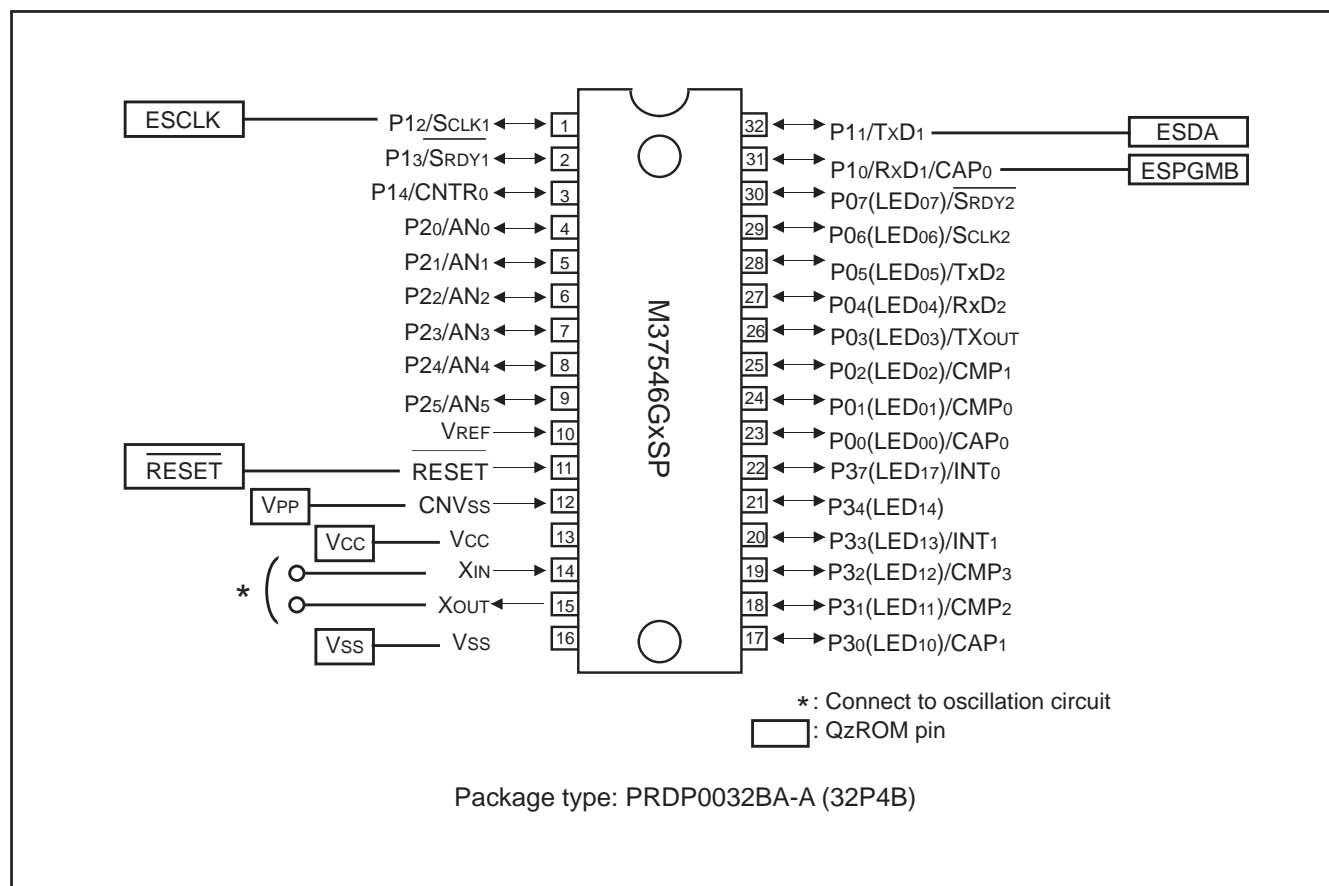


Fig. 90 Pin connection diagram (M37546GxSP)

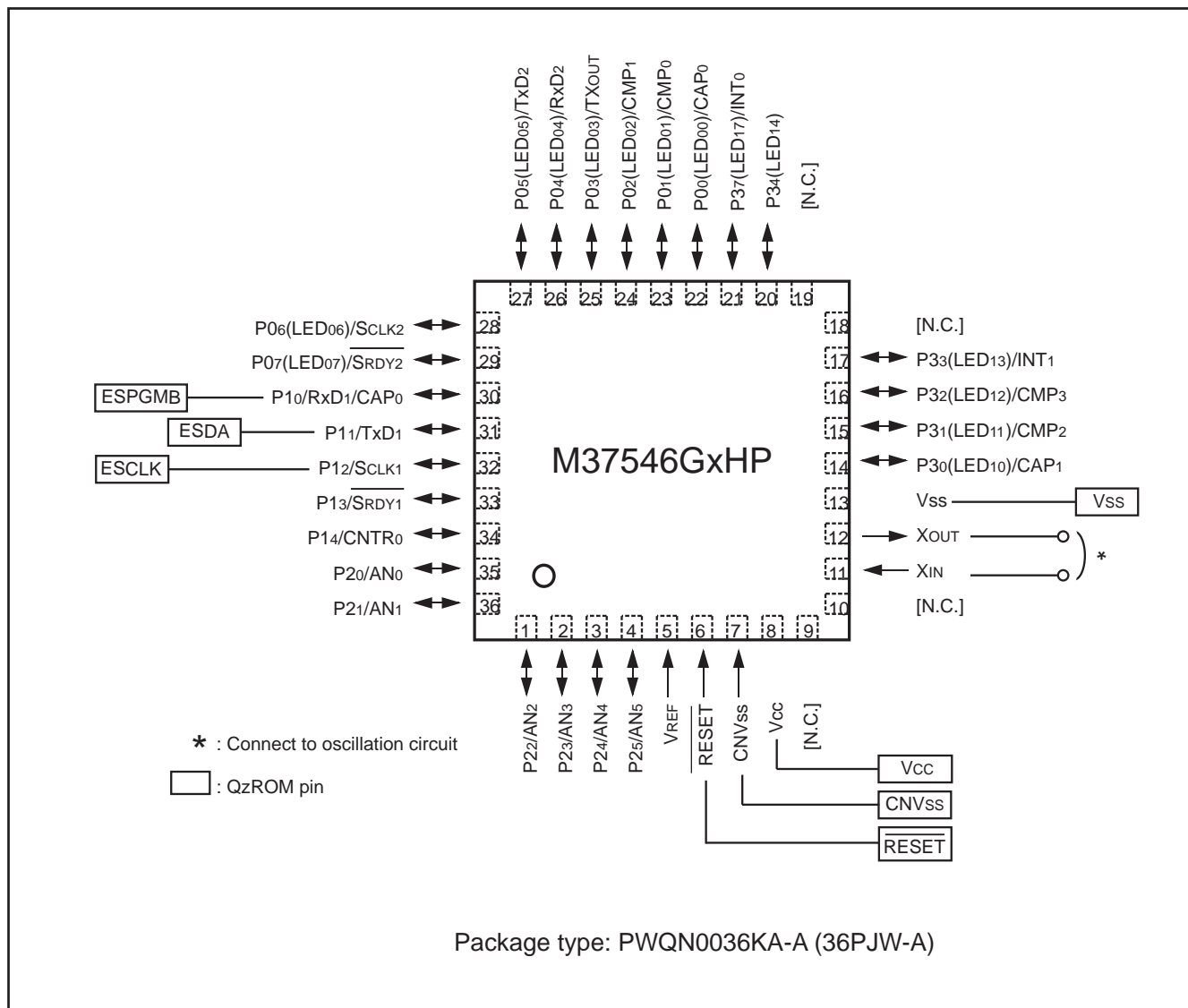


Fig. 91 Pin connection diagram (M37546GxHP)

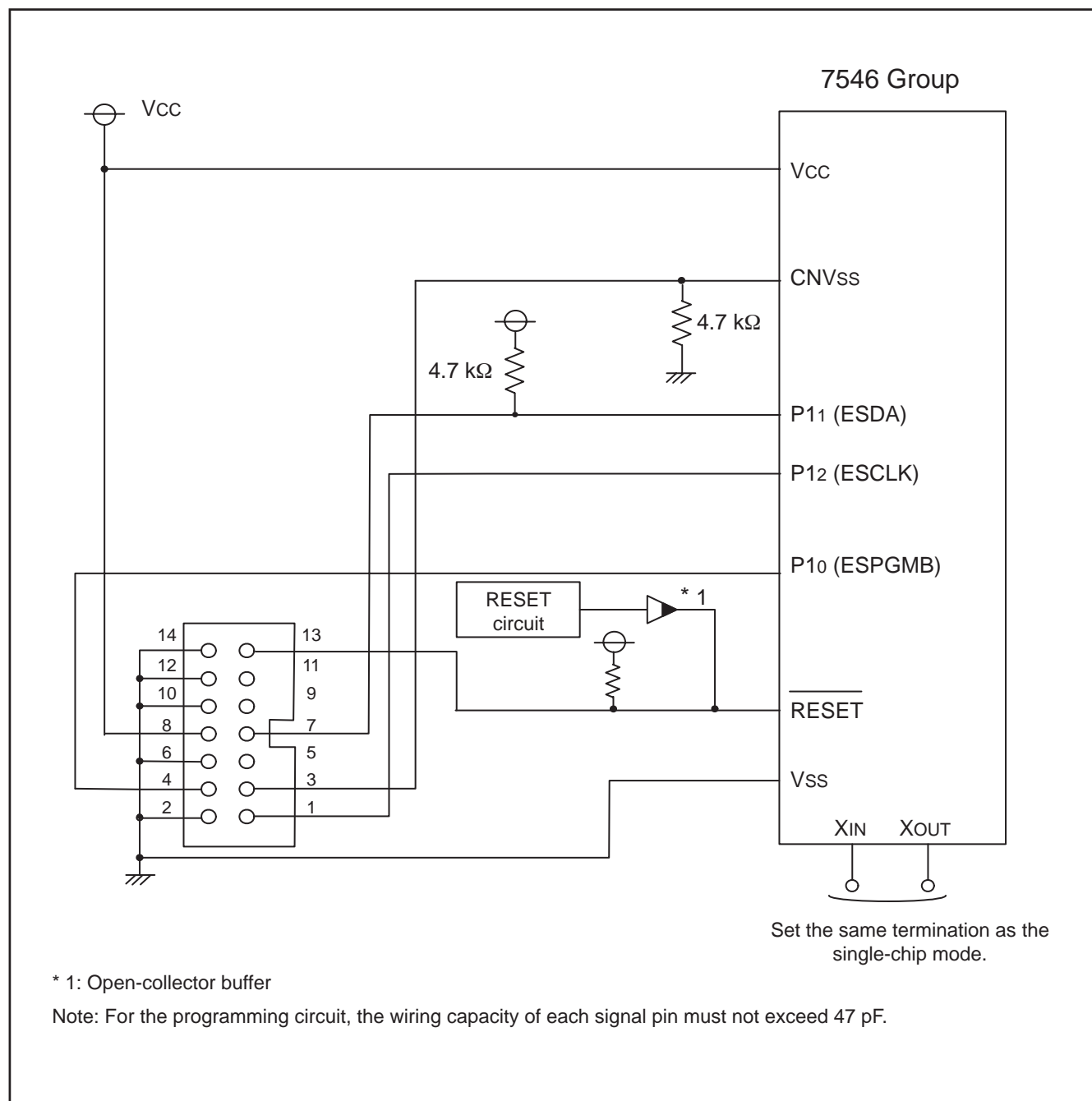


Fig. 92 When using E8 programmer, connection example

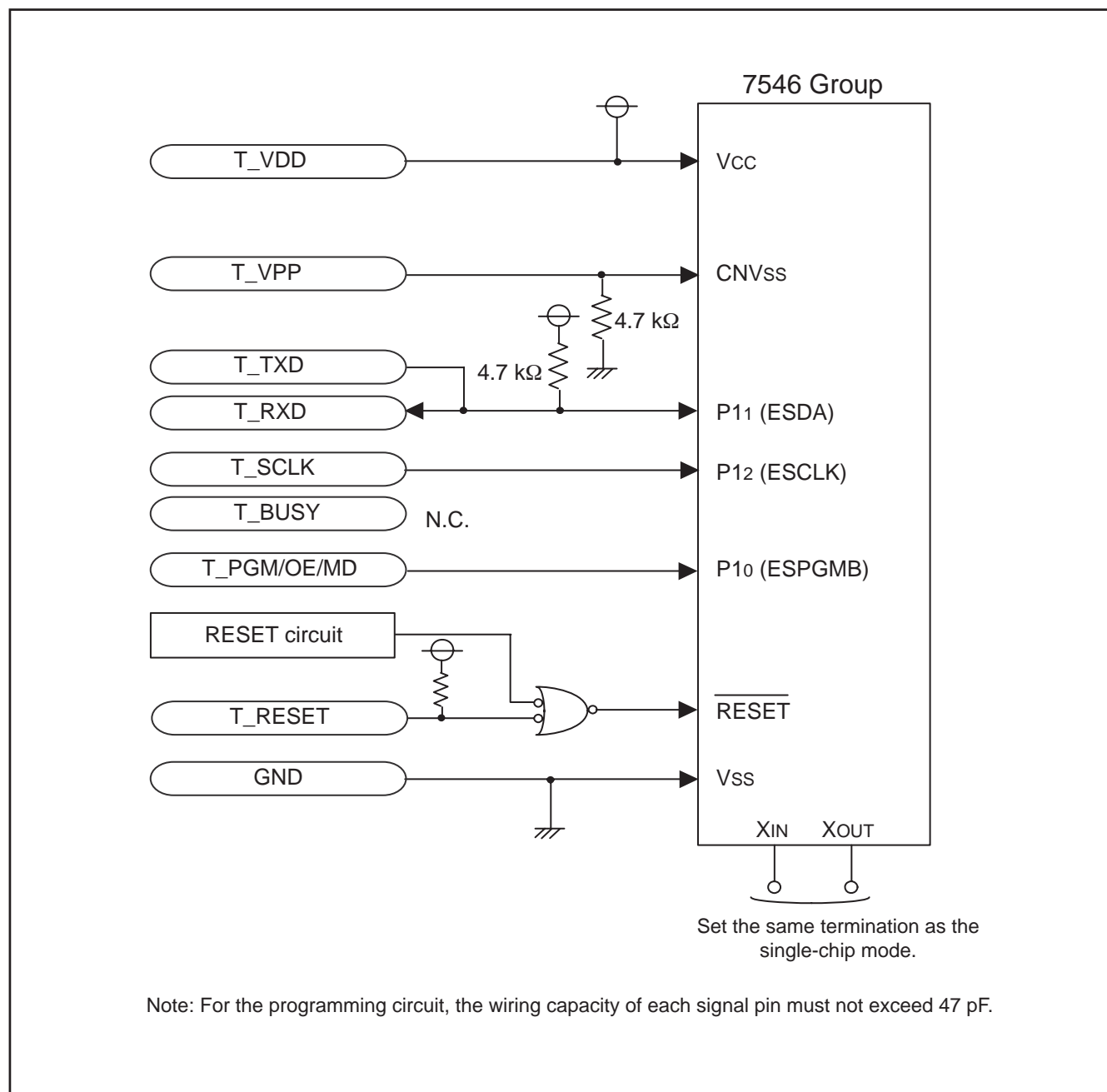


Fig. 93 When using programmer of Suisai Electronics System Co., LTD, connection example

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations. Initialize these flags at beginning of the program.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Ports

- The values of the port direction registers cannot be read. That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
- It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
- For setting direction registers, use the LDM instruction, STA instruction, etc.

A/D Conversion

Do not execute the STP instruction during A/D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.

The frequency of the internal clock ϕ is the same as that of the XIN in double-speed mode, twice the XIN cycle in high-speed mode and 8 times the XIN cycle in middle-speed mode.

CPU Mode Register

The oscillation mode selection bit and processor mode bits can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit. (Emulator MCU is excluded.)

When a ceramic oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

State transition

Do not stop the clock selected as the operation clock because of setting of CM3, 4.

NOTES ON HARDWARE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μ F to 0.1 μ F is recommended.

NOTES ON USE

Countermeasures against noise

1. Shortest wiring length

(1) Package

Select the smallest possible package to make the total wiring length short.

<Reason>

The wiring length depends on a microcomputer package. Use of a small package, for example QFP and not DIP, makes the total wiring length short to reduce influence of noise.

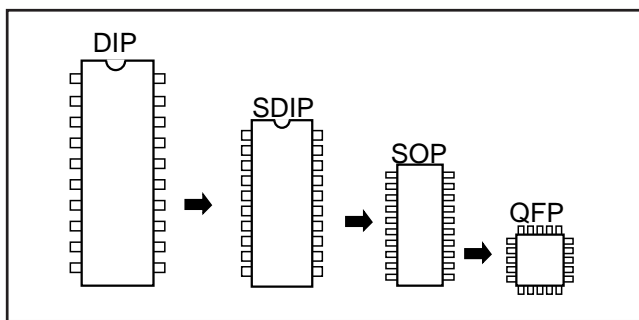


Fig. 94 Selection of packages

(2) Wiring for RESET pin

Make the length of wiring which is connected to the RESET pin as short as possible. Especially, connect a capacitor across the RESET pin and the Vss pin with the shortest possible wiring (within 20 mm).

<Reason>

The width of a pulse input into the RESET pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the RESET pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

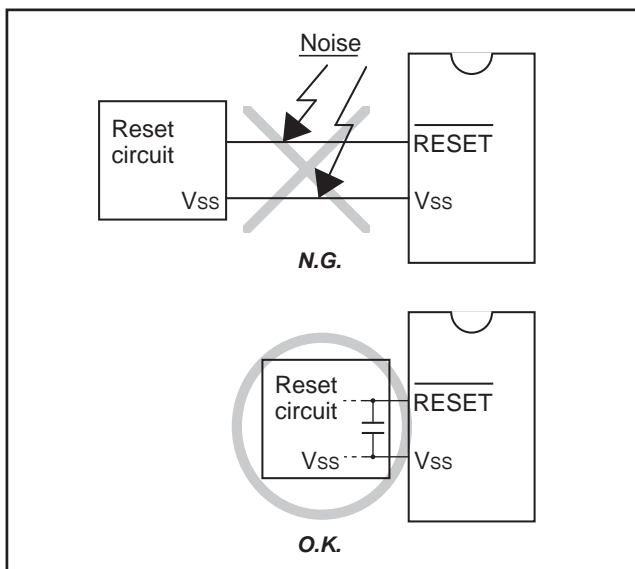


Fig. 95 Wiring for the RESET pin

(3) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

<Reason>

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

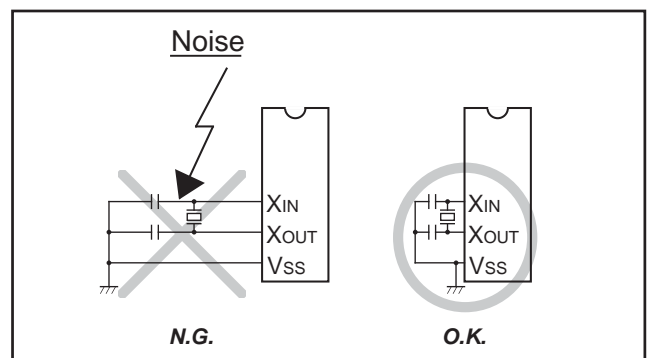


Fig. 96 Wiring for clock I/O pins

(4) Wiring to CNVss pin

Connect CNVss pin to a GND pattern at the shortest distance.

The GND pattern is required to be as close as possible to the GND supplied to Vss.

In order to improve the noise reduction, to connect a 5 kΩ resistor serially to the CNVss pin - GND line may be valid.

As well as the above-mentioned, in this case, connect to a GND pattern at the shortest distance. The GND pattern is required to be as close as possible to the GND supplied to Vss.

<Reason>

The CNVss pin of the QzROM is the power source input pin for the built-in QzROM. When programming in the built-in QzROM, the impedance of the CNVss pin is low to allow the electric current for writing flow into the QzROM. Because of this, noise can enter easily. If noise enters the CNVss pin, abnormal instruction codes or data are read from the built-in QzROM, which may cause a program runaway.

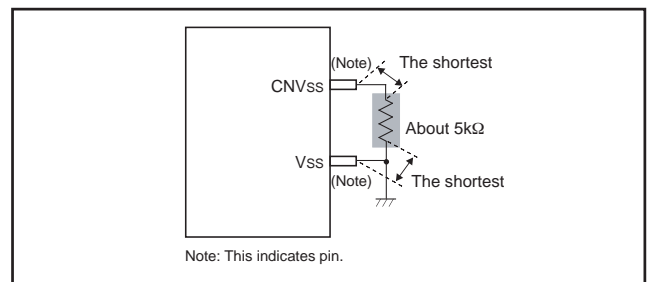


Fig. 97 Wiring for the CNVss pin of the QzPROM

2. Connection of bypass capacitor across Vss line and Vcc line
Connect an approximately 0.1 μF bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

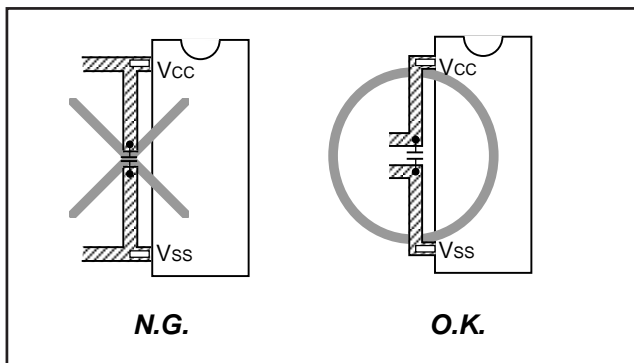


Fig. 98 Bypass capacitor across the Vss line and the Vcc line

3. Wiring to analog input pins

- Connect an approximately 100 Ω to 1 k Ω resistor to an analog signal line which is connected to an analog input pin in series. Besides, connect the resistor to the microcomputer as close as possible.
- Connect an approximately 1000 pF capacitor across the Vss pin and the analog input pin. Besides, connect the capacitor to the Vss pin as close as possible. Also, connect the capacitor across the analog input pin and the Vss pin at equal length.

<Reason>

Signals which is input in an analog input pin (such as an A/D converter/comparator input pin) are usually output signals from sensor. The sensor which detects a change of event is installed far from the printed circuit board with a microcomputer, the wiring to an analog input pin is longer necessarily. This long wiring functions as an antenna which feeds noise into the microcomputer, which causes noise to an analog input pin.

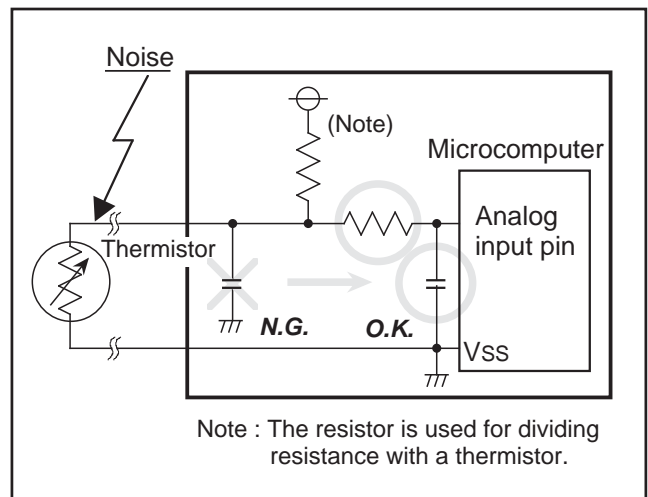


Fig. 99 Analog signal line and a resistor and a capacitor

- The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

4. Oscillator concerns

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

<Reason>

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

(2) Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

<Reason>

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

(3) Oscillator protection using Vss pattern

As for a two-sided printed circuit board, print a Vss pattern on the underside (soldering side) of the position (on the component side) where an oscillator is mounted.

Connect the Vss pattern to the microcomputer Vss pin with the shortest possible wiring. Besides, separate this Vss pattern from other Vss patterns.

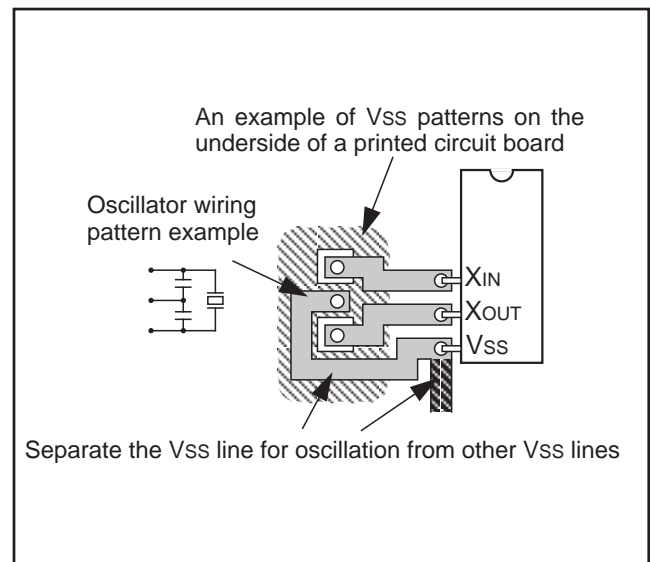


Fig. 101 Vss pattern on the underside of an oscillator

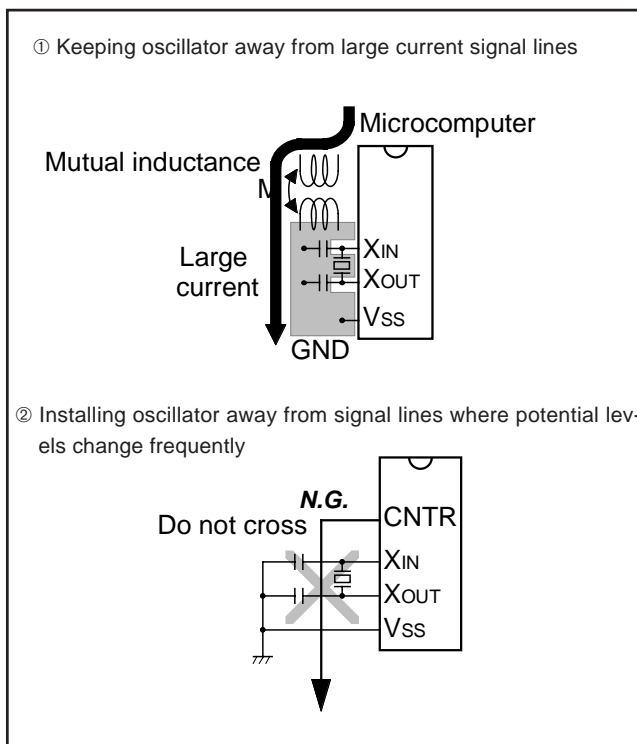


Fig. 100 Wiring for a large current signal line/Writing of signal lines where potential levels change frequently

5. Setup for I/O ports

Setup I/O ports using hardware and software as follows:

<Hardware>

- Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>

- As for an input port, read data several times by a program for checking whether input levels are equal or not.
- As for an output port, since the output data may reverse because of noise, rewrite data to its port latch at fixed periods.
- Rewrite data to direction registers and pull-up control registers at fixed periods.

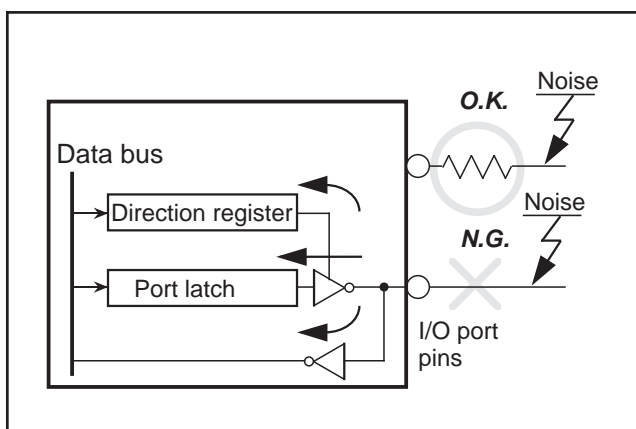


Fig. 102 Setup for I/O ports

6. Providing of watchdog timer function by software

If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer. The following shows an example of a watchdog timer provided by software.

In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine.

This example assumes that interrupt processing is repeated multiple times in a single main routine processing.

<The main routine>

- Assigns a single byte of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine. The initial value N should satisfy the following condition:

$$N+1 \geq (\text{Counts of interrupt processing executed in each main routine})$$

As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.

- Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing after the initial value N has been set.
- Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
 If the SWDT contents do not change after interrupt processing.

<The interrupt processing routine>

- Decrements the SWDT contents by 1 at each interrupt processing.
- Determines that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
- Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
 If the SWDT contents are not initialized to the initial value N but continued to decrement and if they reach 0 or less.

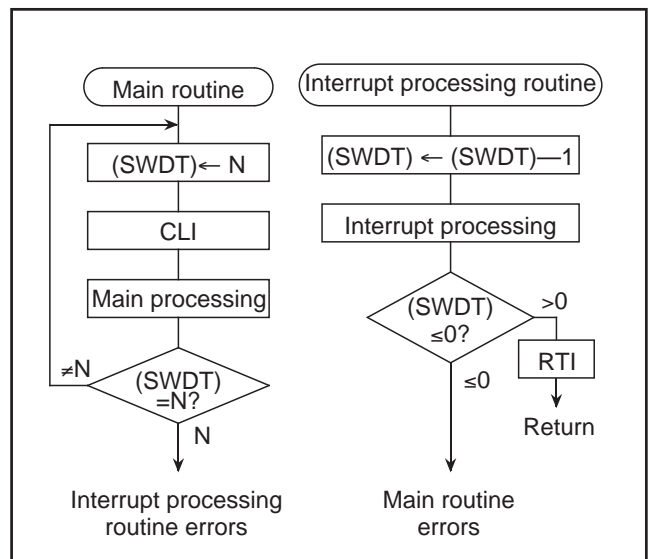


Fig. 103 Watchdog timer by software

NOTES ON QzROM

Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur. Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Precautions Regarding Overvoltage

Make sure that voltage exceeding the VCC pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in Figure below does not occur for CNVss pin (VPP power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

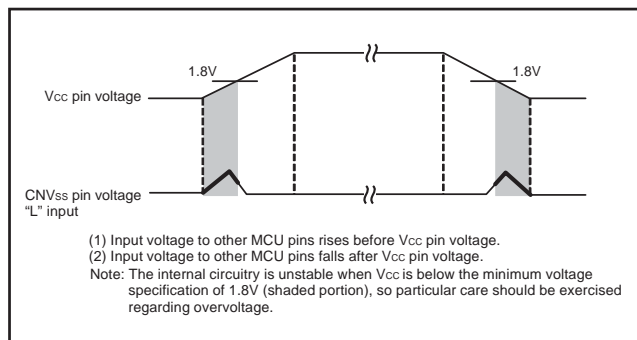


Fig. 104 Timing Diagram (bold-lined periods are applicable)

Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "0016" and "FF16" can not be accepted.
- Set "FF16" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF16" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

Data Required For QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (<http://www.renesas.com/homepage.jsp>).

Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

ELECTRICAL CHARACTERISTICS of 7546 Group

Absolute Maximum Ratings

Absolute maximum ratings

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|---|---|-------------------------------|------|
| V _{CC} | Power source voltage | All voltages are based on V _{SS} . When an input voltage is measured, output transistors are cut off. | −0.3 to 6.5 | V |
| V _I | Input voltage P00–P07, P10–P14, P20–P25, P30–P34, P37, VREF | | −0.3 to V _{CC} + 0.3 | V |
| V _I | Input voltage RESET, X _{IN} | | −0.3 to V _{CC} + 0.3 | V |
| V _I | Input voltage CNV _{SS} | | −0.3 to V _{CC} + 0.3 | V |
| V _O | Output voltage P00–P07, P10–P14, P20–P25, P30–P34, P37, X _{OUT} | | −0.3 to V _{CC} + 0.3 | V |
| P _d | Power dissipation | T _a = 25°C | 300 (Note) | mW |
| T _{opr} | Operating temperature | — | −20 to 85 | °C |
| T _{stg} | Storage temperature | — | −40 to 125 | °C |

Note : 200 mW for the PLQP0032GB-A package product.

Recommended Operating Conditions

Recommended operating conditions (1)

(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | | | Limits | | | Unit |
|--|--|----------------------------|------------------|--------|------|---------|------|
| | | | | Min. | Typ. | Max. | |
| VCC | Power source voltage (ceramic) | (Double-speed mode) | f(XIN) = 8 MHz | 4.5 | 5.0 | 5.5 | V |
| | | | f(XIN) = 6.5 MHz | 4.0 | 5.0 | 5.5 | V |
| | | | f(XIN) = 2 MHz | 2.4 | 5.0 | 5.5 | V |
| | | | f(XIN) = 1 MHz | 2.2 | 5.0 | 5.5 | V |
| | | (High-, Middle-speed mode) | f(XIN) = 8 MHz | 4.0 | 5.0 | 5.5 | V |
| | | | f(XIN) = 4 MHz | 2.4 | 5.0 | 5.5 | V |
| | | | f(XIN) = 2 MHz | 2.2 | 5.0 | 5.5 | V |
| | Power source voltage (RC) | (High-, Middle-speed mode) | f(XIN) = 4 MHz | 4.0 | 5.0 | 5.5 | V |
| | | | f(XIN) = 2 MHz | 2.4 | 5.0 | 5.5 | V |
| | | | f(XIN) = 1 MHz | 2.2 | 5.0 | 5.5 | V |
| Power source voltage (at on-chip oscillator) | | | 1.8 | 5.0 | 5.5 | V | |
| VSS | Power source voltage | | | | 0 | | V |
| VREF | Analog reference voltage | | | 1.8 | | Vcc | V |
| VIH | “H” input voltage P00–P07, P10–P14, P20–P25, P30–P34, P37 | | | 0.8Vcc | | Vcc | V |
| VIH | “H” input voltage (TTL input level selected) P10, P12, P13, P37 (Note 1) | | | 2.0 | | Vcc | V |
| VIH | “H” input voltage RESET, XIN | | | 0.8Vcc | | Vcc | V |
| VIL | “L” input voltage P00–P07, P10–P14, P20–P25, P30–P34, P37 | | | 0 | | 0.2Vcc | V |
| VIL | “L” input voltage (TTL input level selected) P10, P12, P13, P37 (Note 1) | | | 0 | | 0.8 | V |
| VIL | “L” input voltage RESET, CNVss | | | 0 | | 0.2Vcc | V |
| VIL | “L” input voltage XIN | | | 0 | | 0.16Vcc | V |
| ΣIOH(peak) | “H” total peak output current (Note 2) P00–P07, P10–P14, P20–P25, P30–P34, P37 | | | | | –80 | mA |
| ΣIOL(peak) | “L” total peak output current (Note 2) P10–P14, P20–P25 | | | | | 80 | mA |
| ΣIOL(peak) | “L” total peak output current (Note 2) P00–P07, P30–P34, P37 | | | | | 80 | mA |
| ΣIOH(avg) | “H” total average output current (Note 2) P00–P07, P10–P14, P20–P25, P30–P34, P37 | | | | | –40 | mA |
| ΣIOL(avg) | “L” total average output current (Note 2) P10–P14, P20–P25 | | | | | 40 | mA |
| ΣIOL(avg) | “L” total average output current (Note 2) P00–P07, P30–P34, P37 | | | | | 40 | mA |

Note 1: V_{CC} = 4.0 to 5.5V

2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Recommended operating conditions (2)(V_{CC} = 1.8 to 5.5V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------------------|---|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| I _{OH} (peak) | "H" peak output current (Note 1) P00–P07, P10–P14, P20–P25, P30–P34, P37 | | | –10 | mA |
| I _{OL} (peak) | "L" peak output current (Note 1) P00–P07, P30–P34, P37 (Drive capacity = "L") P10–P14, P20–P25 | | | 10 | mA |
| I _{OL} (peak) | "L" peak output current (Note 1) P00–P07, P30–P34, P37 (Drive capacity = "H") | | | 30 | mA |
| I _{OH} (avg) | "H" average output current (Note 2) P00–P07, P10–P14, P20–P25, P30–P34, P37 | | | –5 | mA |
| I _{OL} (avg) | "L" average output current (Note 2) P00–P07, P30–P34, P37 (Drive capacity = "L") P10–P14, P20–P25 | | | 5 | mA |
| I _{OL} (avg) | "L" average output current (Note 2) P00–P07, P30–P34, P37 (Drive capacity = "H") | | | 15 | mA |
| f(XIN) | Oscillation frequency (Note 3) at ceramic oscillation or external clock input (V _{CC} = 4.5 V to 5.5 V) Double-speed mode | | | 8 | MHz |
| | Oscillation frequency (Note 3) at ceramic oscillation or external clock input (V _{CC} = 4.0 V to 5.5 V) Double-speed mode | | | 6.5 | MHz |
| | Oscillation frequency (Note 3) at ceramic oscillation or external clock input (V _{CC} = 2.4 V to 5.5 V) Double-speed mode | | | 2 | MHz |
| | Oscillation frequency (Note 3) at ceramic oscillation or external clock input (V _{CC} = 2.2 V to 5.5 V) Double-speed mode | | | 1 | MHz |
| | Oscillation frequency (Note 3) at ceramic oscillation or external clock input (V _{CC} = 4.0 V to 5.5 V) High-, Middle-speed mode | | | 8 | MHz |
| | Oscillation frequency (Note 3) at ceramic oscillation or external clock input (V _{CC} = 2.4 V to 5.5 V) High-, Middle-speed mode | | | 4 | MHz |
| | Oscillation frequency (Note 3) at ceramic oscillation or external clock input (V _{CC} = 2.2 V to 5.5 V) High-, Middle-speed mode | | | 2 | MHz |
| | Oscillation frequency (Note 3) at RC oscillation (V _{CC} = 4.0 V to 5.5 V) High-, Middle-speed mode | | | 4 | MHz |
| | Oscillation frequency (Note 3) at RC oscillation (V _{CC} = 2.4 V to 5.5 V) High-, Middle-speed mode | | | 2 | MHz |
| | Oscillation frequency (Note 3) at RC oscillation (V _{CC} = 2.2 V to 5.5 V) High-, Middle-speed mode | | | 1 | MHz |
| | | | | | |
| | | | | | |

Notes 1: The peak output current is the peak current flowing in each port.**2:** The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.**3:** When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics

Electrical characteristics (1)

(V_{CC} = 1.8 to 5.5V, V_{SS} = 0 V, T_a = -20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|----------------------------------|--|--|----------------------|------|-------|------|
| | | | Min. | Typ. | Max. | |
| V _{OH} | “H” output voltage P00–P07, P10–P14, P20–P25, P30–P34, P37 (Note 1) | I _{OH} = -5 mA V _{CC} = 4.0 to 5.5 V | V _{CC} -1.5 | | | V |
| | | I _{OH} = -1.0 mA V _{CC} = 1.8 to 5.5 V | V _{CC} -1.0 | | | V |
| V _{OL} | “L” output voltage P00–P07, P30–P34, P37 (Drive capacity = “L”) P10–P14, P20–P25 | I _{OL} = 5 mA V _{CC} = 4.0 to 5.5 V | | | 1.5 | V |
| | | I _{OL} = 1.5 mA V _{CC} = 4.0 to 5.5 V | | | 0.3 | V |
| | | I _{OL} = 1.0 mA V _{CC} = 1.8 to 5.5 V | | | 1.0 | V |
| V _{OL} | “L” output voltage P00–P07, P30–P34, P37 (Drive capacity = “H”) | I _{OL} = 15 mA V _{CC} = 4.0 to 5.5 V | | | 2.0 | V |
| | | I _{OL} = 1.5 mA V _{CC} = 4.0 to 5.5 V | | | 0.3 | V |
| | | I _{OL} = 1.0 mA V _{CC} = 1.8 to 5.5 V | | | 1.0 | V |
| V _{T+} –V _{T–} | Hysteresis CNTR0, INT0, INT1, CAP0, CAP1 (Note 2) P00–P07 (Note 3) | | | 0.4 | | V |
| V _{T+} –V _{T–} | Hysteresis RxD0, SCLK0, RxD1, SCLK1 | | | 0.5 | | V |
| V _{T+} –V _{T–} | Hysteresis RESET | | | 0.5 | | V |
| I _{IH} | “H” input current P00–P07, P10–P14, P20–P25, P30–P34, P37 | V _I = V _{CC} (Pin floating. Pull up transistors “off”) | | | 5.0 | μA |
| I _{IH} | “H” input current RESET | V _I = V _{CC} | | | 5.0 | μA |
| I _{IH} | “H” input current X _{IN} | V _I = V _{CC} | | 4.0 | | μA |
| I _{IL} | “L” input current P00–P07, P10–P14, P20–P25, P30–P34, P37 | V _I = V _{SS} (Pin floating. Pull up transistors “off”) | | | -5.0 | μA |
| I _{IL} | “L” input current RESET | V _I = V _{SS} | | | -5.0 | μA |
| I _{IL} | “L” input current X _{IN} | V _I = V _{SS} | | -4.0 | | μA |
| I _{IL} | “L” input current P00–P07, P30–P34, P37 | V _I = V _{SS} (Pull up transistors “on”) | | -0.2 | -0.5 | mA |
| V _{RAM} | RAM hold voltage | When clock stopped | 1.6 | | 5.5 | V |
| R _{OSC} | On-chip oscillator oscillation frequency | V _{CC} = 5.0 V, T _a = 25 °C | 1000 | 2000 | 3000 | kHz |
| D _{OSC} | Oscillation stop detection circuit detection frequency | V _{CC} = 5.0 V, T _a = 25 °C | 62.5 | 125 | 187.5 | kHz |

Notes1: P11 is measured when the P11/TxD1 P-channel output disable bit of the UART1 control register (bit 4 of address 001B16) is “0”.

P05 is measured when the P05/TxD2 P-channel output disable bit of the UART2 control register (bit 4 of address 003116) is “0”.

2: RxD1, SCLK1 and INT0 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to “0” (CMOS level).

3: It is available only when operating key-on wake up.

Electrical characteristics (2)**(V_{CC} = 1.8 to 5.5V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)**

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|-----------------|--|---|------------------------|--------|------|------|------|
| | | | | Min. | Typ. | Max. | |
| I _{CC} | Power source current *LVD is valid (except at STP) | f(X _{IN}) = 8 MHz | Double-speed mode | | 5.9 | 9.5 | mA |
| | | Output transistors "off" | High-speed mode | | 3.9 | 7.0 | mA |
| | | | Middle-speed mode | | 2.4 | 5.5 | mA |
| | | f(X _{IN}) = 2 MHz, V _{CC} = 2.2 V | High-speed mode | | 0.45 | 1.25 | mA |
| | | On-chip oscillator operation mode, Output transistors "off" | Frequency/1 | | 1.55 | 3.3 | mA |
| | | | Frequency/2 | | 0.95 | 2.3 | mA |
| | | | Frequency/8 | | 0.4 | 1.1 | mA |
| | | | Frequency/128 | | 0.25 | 0.7 | mA |
| | | f(X _{IN}) = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors "off" | | | 2.0 | 3.5 | mA |
| | | f(X _{IN}) = 2 MHz, V _{CC} = 2.2 V (in WIT state), functions except timer 1 disabled, Output transistors "off" | | | 0.25 | | mA |
| | | On-chip oscillator operation mode, (in WIT state), functions except timer 1 disabled, Output transistors "off" | | | 0.25 | 0.7 | mA |
| | | Increment when A/D conversion is executed f(X _{IN}) = 8 MHz, V _{CC} = 5 V | | | 0.5 | | mA |
| | | All oscillation stopped (in STP state) Output transistors "off" | T _a = 25 °C | | 0.1 | 1.0 | μA |
| | | | T _a = 85 °C | | | 10 | μA |
| | | Low voltage detection circuit self consumption current | | | 70 | | μA |

Note: Increment when A/D conversion is executed includes the reference power source input current (I_{VREF}).

A/D Converter Characteristics

A/D Converter characteristics

(VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---------|--------------------------------------|---|--------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| — | Resolution | | | | 10 | Bits |
| — | Absolute accuracy | Ta = 25 °C VCC = VREF = 2.7 to 5.5 V | | | ± 3 | LSB |
| tCONV | Conversion time | AD conversion clock = f(XIN)/2 | | | 122 | tc(XIN) |
| | | AD conversion clock = f(XIN) | | | 61 | |
| RLADDER | Ladder resistor | | | 55 | | kΩ |
| IVREF | Reference power source input current | VREF = 5.0 V | 50 | 150 | 200 | μA |
| | | VREF = 3.0 V | 30 | 90 | 120 | |
| II(AD) | A/D port input current | | | | 5.0 | μA |

Note: AD conversion accuracy may be low under the following conditions;

- (1) When the VREF voltage is set to be lower than the VCC voltage, an analog circuit in this microcomputer is affected by noise.
The accuracy is lower than the case the VREF voltage is the same as VCC voltage.
- (2) When the VREF voltage is 3.0 V or less at the low temperature, the AD conversion accuracy may be very lower than at room temperature.
When system is used at low temperature, that VREF is 3.0 V or more is recommended.

Power-on reset circuit characteristics

Power-on reset circuit characteristics

(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|------------------------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{POR} | Valid start voltage of power-on reset circuit (Note) | | | | 0 | mV |
| TW(V _{POR}) | V _{POR} hold time | TW(V _{POR}) > 10 s | 10 | | | s |
| TW(V _{POR} -V _{DET}) | Rising time of valid power source of power-on reset circuit | | | | 20 | ms |

Note: V_{POR} is the start voltage level of V_{CC} for the built-in power-on reset circuit to operate normally.

Keep V_{POR} to be lower than the V_{CC} voltage before rising of the V_{CC} power source to use the built-in power-on reset circuit.

Set the built-in low voltage detection circuit to be valid when the built-in power-on reset is used.

Low voltage detection circuit characteristics

Low voltage detection circuit characteristics

(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|------------------|---|-------------------------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{LVD} | Valid start voltage of low voltage detection circuit (Note) | | 1.0 | | | V |
| V _{DET} | Detection voltage of low voltage detection circuit | T _a = 0 to 50 °C | 1.85 | 1.95 | 2.05 | V |
| | | T _a = –20 to 85 °C | 1.8 | 1.95 | 2.1 | V |
| T _{DET} | Detection time of low voltage detection circuit | | | 20 | | μs |

Note: V_{LVD} is the start voltage level of V_{CC} for the built-in low voltage detection circuit to operate normally.

If the V_{CC} power source becomes lower than V_{LVD}, first set the V_{CC} voltage to be lower than V_{POR}. Next, according to the electrical characteristics of the power-on reset circuit, perform the rising of V_{CC}.

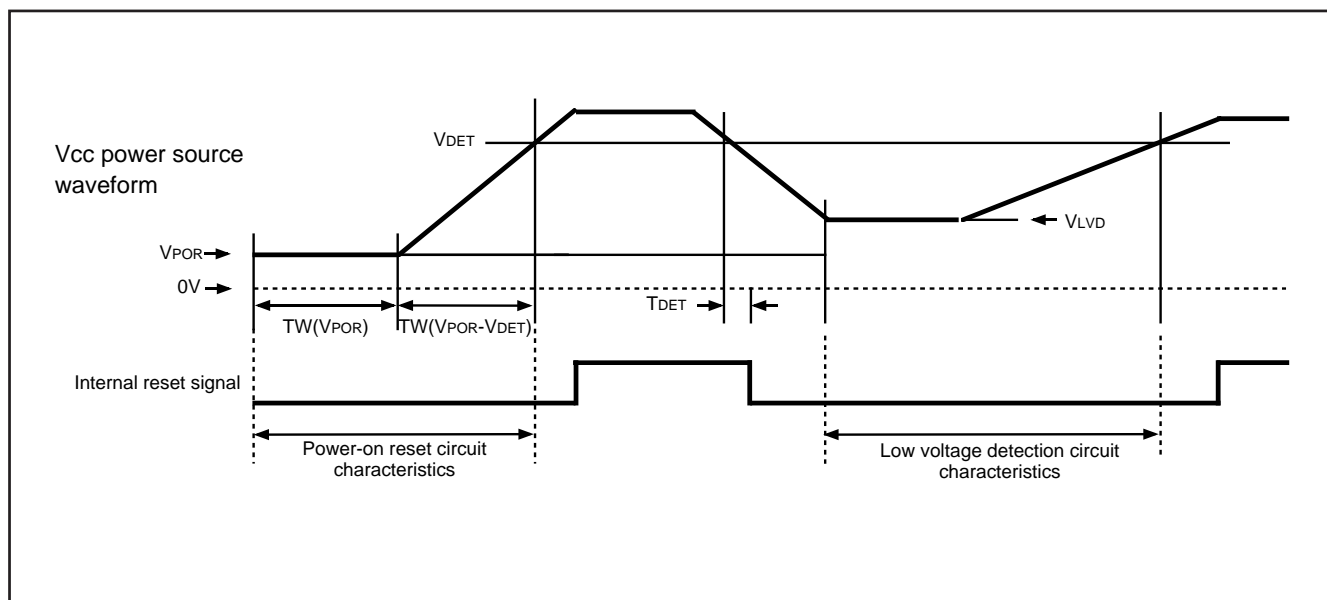


Fig. 105 Electrical characteristics of power-on reset circuit and low voltage detection circuit

Timing Requirements

Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|--|--|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| t _w (RESET) | Reset input “L” pulse width | 2 | | | μs |
| t _c (X _{IN}) | External clock input cycle time | 125 | | | ns |
| t _{WH} (X _{IN}) | External clock input “H” pulse width | 50 | | | ns |
| t _{WL} (X _{IN}) | External clock input “L” pulse width | 50 | | | ns |
| t _c (CNTR ₀) | CNTR ₀ input cycle time | 200 | | | ns |
| t _{WH} (CNTR ₀) | CNTR ₀ , INT ₀ , INT ₁ , CAP ₀ , CAP ₁ input “H” pulse width (Note 1) | 80 | | | ns |
| t _{WL} (CNTR ₀) | CNTR ₀ , INT ₀ , INT ₁ , CAP ₀ , CAP ₁ input “L” pulse width (Note 1) | 80 | | | ns |
| t _c (SCLK ₁) | Serial I/O1, serial I/O2 clock input cycle time (Note 2) | 800 | | | ns |
| t _{WH} (SCLK ₁) | Serial I/O1, serial I/O2 clock input “H” pulse width (Note 2) | 370 | | | ns |
| t _{WL} (SCLK ₁) | Serial I/O1, serial I/O2 clock input “L” pulse width (Note 2) | 370 | | | ns |
| t _{su} (RxD ₁ –SCLK ₁) | Serial I/O1, serial I/O2 input set up time | 220 | | | ns |
| t _h (SCLK ₁ –RxD ₁) | Serial I/O1, serial I/O2 input hold time | 100 | | | ns |

Notes 1: As for CAP₀, CAP₁, it is the value when noise filter is not used.

2: In this time, bit 6 of the serial I/O1 control register (address 001A16) is set to “1” (clock synchronous serial I/O is selected).

When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

In this time, bit 6 of the serial I/O2 control register (address 003016) is set to “1” (clock synchronous serial I/O is selected).

When bit 6 of the serial I/O2 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Timing requirements (2)

(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|--|--|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| t _w (RESET) | Reset input “L” pulse width | 2 | | | μs |
| t _c (X _{IN}) | External clock input cycle time | 250 | | | ns |
| t _{WH} (X _{IN}) | External clock input “H” pulse width | 100 | | | ns |
| t _{WL} (X _{IN}) | External clock input “L” pulse width | 100 | | | ns |
| t _c (CNTR ₀) | CNTR ₀ input cycle time | 500 | | | ns |
| t _{WH} (CNTR ₀) | CNTR ₀ , INT ₀ , INT ₁ , CAP ₀ , CAP ₁ input “H” pulse width (Note 1) | 230 | | | ns |
| t _{WL} (CNTR ₀) | CNTR ₀ , INT ₀ , INT ₁ , CAP ₀ , CAP ₁ input “L” pulse width (Note 1) | 230 | | | ns |
| t _c (SCLK ₁) | Serial I/O1, serial I/O2 clock input cycle time (Note 2) | 2000 | | | ns |
| t _{WH} (SCLK ₁) | Serial I/O1, serial I/O2 clock input “H” pulse width (Note 2) | 950 | | | ns |
| t _{WL} (SCLK ₁) | Serial I/O1, serial I/O2 clock input “L” pulse width (Note 2) | 950 | | | ns |
| t _{su} (RxD ₁ –SCLK ₁) | Serial I/O1, serial I/O2 input set up time | 400 | | | ns |
| t _h (SCLK ₁ –RxD ₁) | Serial I/O1, serial I/O2 input hold time | 200 | | | ns |

Notes 1: As for CAP₀, CAP₁, it is the value when noise filter is not used.

2: In this time, bit 6 of the serial I/O1 control register (address 001A16) is set to “1” (clock synchronous serial I/O is selected).

When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

In this time, bit 6 of the serial I/O2 control register (address 003016) is set to “1” (clock synchronous serial I/O is selected).

When bit 6 of the serial I/O2 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Timing requirements (3)

(VCC = 2.2 to 5.5 V, VSS = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------------------------|---|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| t _w (RESET) | Reset input "L" pulse width | 2 | | | μs |
| t _c (XIN) | External clock input cycle time | 500 | | | ns |
| t _{WH} (XIN) | External clock input "H" pulse width | 200 | | | ns |
| t _{WL} (XIN) | External clock input "L" pulse width | 200 | | | ns |
| t _c (CNTR0) | CNTR0 input cycle time | 1000 | | | ns |
| t _{WH} (CNTR0) | CNTR0, INT0, INT1, CAP0, CAP1 input "H" pulse width (Note 1) | 460 | | | ns |
| t _{WL} (CNTR0) | CNTR0, INT0, INT1, CAP0, CAP1 input "L" pulse width (Note 1) | 460 | | | ns |
| t _c (SCLK1) | Serial I/O1, serial I/O2 clock input cycle time (Note 2) | 4000 | | | ns |
| t _{WH} (SCLK1) | Serial I/O1, serial I/O2 clock input "H" pulse width (Note 2) | 1900 | | | ns |
| t _{WL} (SCLK1) | Serial I/O1, serial I/O2 clock input "L" pulse width (Note 2) | 1900 | | | ns |
| t _{su} (RxD1–SCLK1) | Serial I/O1, serial I/O2 input set up time | 800 | | | ns |
| t _h (SCLK1–RxD1) | Serial I/O1, serial I/O2 input hold time | 400 | | | ns |

Notes 1: As for CAP0, CAP1, it is the value when noise filter is not used.**2:** In this time, bit 6 of the serial I/O1 control register (address 001A16) is set to "1" (clock synchronous serial I/O is selected).

When bit 6 of the serial I/O1 control register is "0" (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.

In this time, bit 6 of the serial I/O2 control register (address 003016) is set to "1" (clock synchronous serial I/O is selected).

When bit 6 of the serial I/O2 control register is "0" (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Switching Characteristics

Switching characteristics (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-----------------------------|---|-----------------------------|------|------|------|
| | | Min. | Typ. | Max. | |
| t _{WH} (SCLK1) | Serial I/O1, serial I/O2 clock output "H" pulse width | t _C (SCLK1)/2–30 | | | ns |
| t _{WL} (SCLK1) | Serial I/O1, serial I/O2 clock output "L" pulse width | t _C (SCLK1)/2–30 | | | ns |
| t _d (SCLK1–TxD1) | Serial I/O1, serial I/O2 output delay time | | | 140 | ns |
| t _v (SCLK1–TxD1) | Serial I/O1, serial I/O2 output valid time | –30 | | | ns |
| t _r (SCLK1) | Serial I/O1, serial I/O2 clock output rising time | | | 30 | ns |
| t _f (SCLK1) | Serial I/O1, serial I/O2 clock output falling time | | | 30 | ns |
| t _r (CMOS) | CMOS output rising time (Note 1) | | 10 | 30 | ns |
| t _f (CMOS) | CMOS output falling time (Note 1) | | 10 | 30 | ns |

Note 1: Pin XOUT is excluded.

Switching characteristics (2)

(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-----------------------------|---|-----------------------------|------|------|------|
| | | Min. | Typ. | Max. | |
| t _{WH} (SCLK1) | Serial I/O1, serial I/O2 clock output "H" pulse width | t _C (SCLK1)/2–50 | | | ns |
| t _{WL} (SCLK1) | Serial I/O1, serial I/O2 clock output "L" pulse width | t _C (SCLK1)/2–50 | | | ns |
| t _d (SCLK1–TxD1) | Serial I/O1, serial I/O2 output delay time | | | 350 | ns |
| t _v (SCLK1–TxD1) | Serial I/O1, serial I/O2 output valid time | –30 | | | ns |
| t _r (SCLK1) | Serial I/O1, serial I/O2 clock output rising time | | | 50 | ns |
| t _f (SCLK1) | Serial I/O1, serial I/O2 clock output falling time | | | 50 | ns |
| t _r (CMOS) | CMOS output rising time (Note 1) | | 20 | 50 | ns |
| t _f (CMOS) | CMOS output falling time (Note 1) | | 20 | 50 | ns |

Note 1: Pin XOUT is excluded.

Switching characteristics (3)

(V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-----------------------------|---|-----------------------------|------|------|------|
| | | Min. | Typ. | Max. | |
| t _{WH} (SCLK1) | Serial I/O1, serial I/O2 clock output "H" pulse width | t _C (SCLK1)/2–70 | | | ns |
| t _{WL} (SCLK1) | Serial I/O1, serial I/O2 clock output "L" pulse width | t _C (SCLK1)/2–70 | | | ns |
| t _d (SCLK1–TxD1) | Serial I/O1, serial I/O2 output delay time | | | 450 | ns |
| t _v (SCLK1–TxD1) | Serial I/O1, serial I/O2 output valid time | –30 | | | ns |
| t _r (SCLK1) | Serial I/O1, serial I/O2 clock output rising time | | | 70 | ns |
| t _f (SCLK1) | Serial I/O1, serial I/O2 clock output falling time | | | 70 | ns |
| t _r (CMOS) | CMOS output rising time (Note 1) | | 25 | 70 | ns |
| t _f (CMOS) | CMOS output falling time (Note 1) | | 25 | 70 | ns |

Note 1: Pin XOUT is excluded.

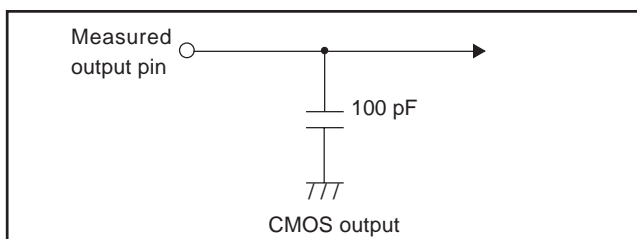


Fig. 106 Switching characteristics measurement circuit diagram

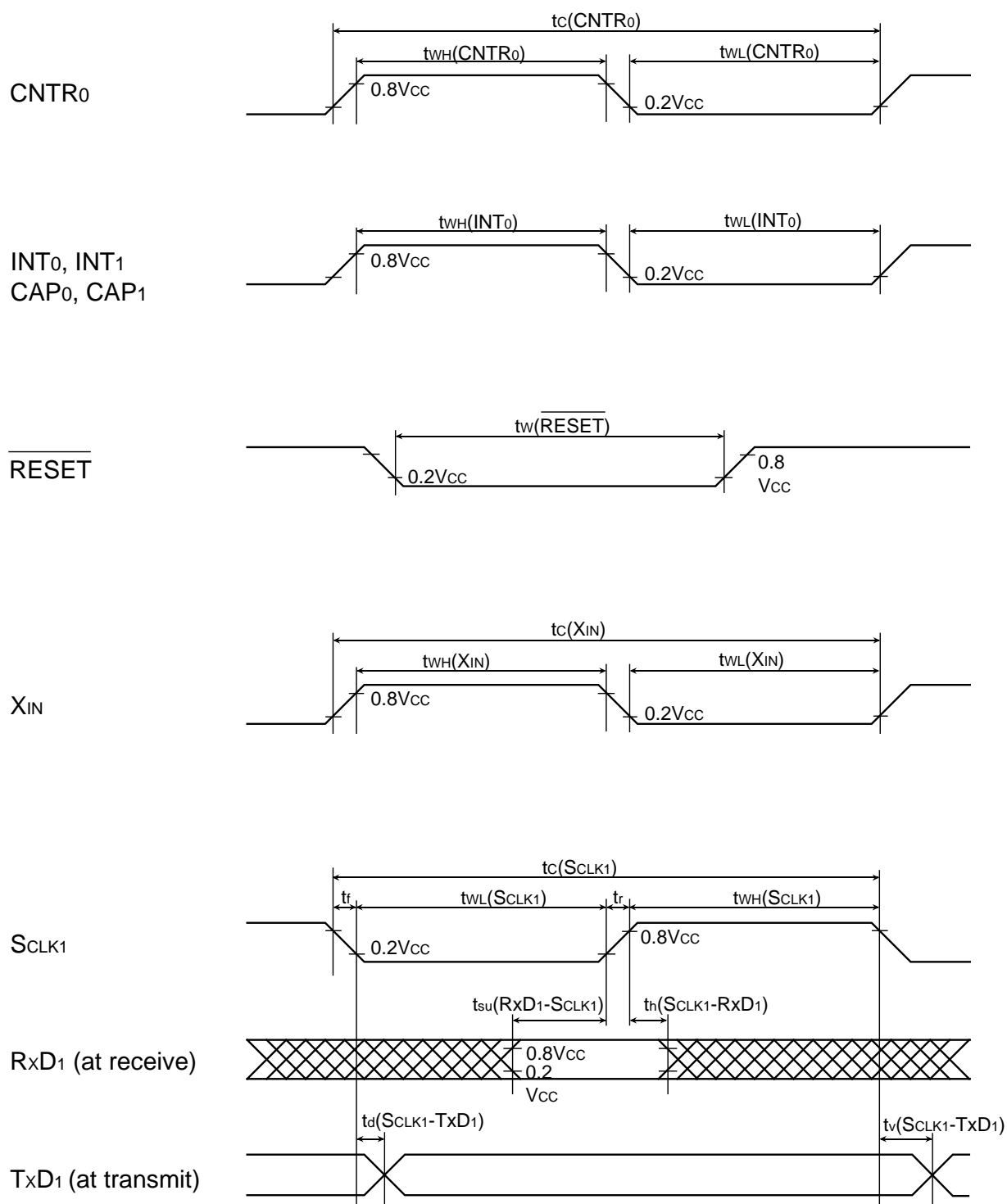
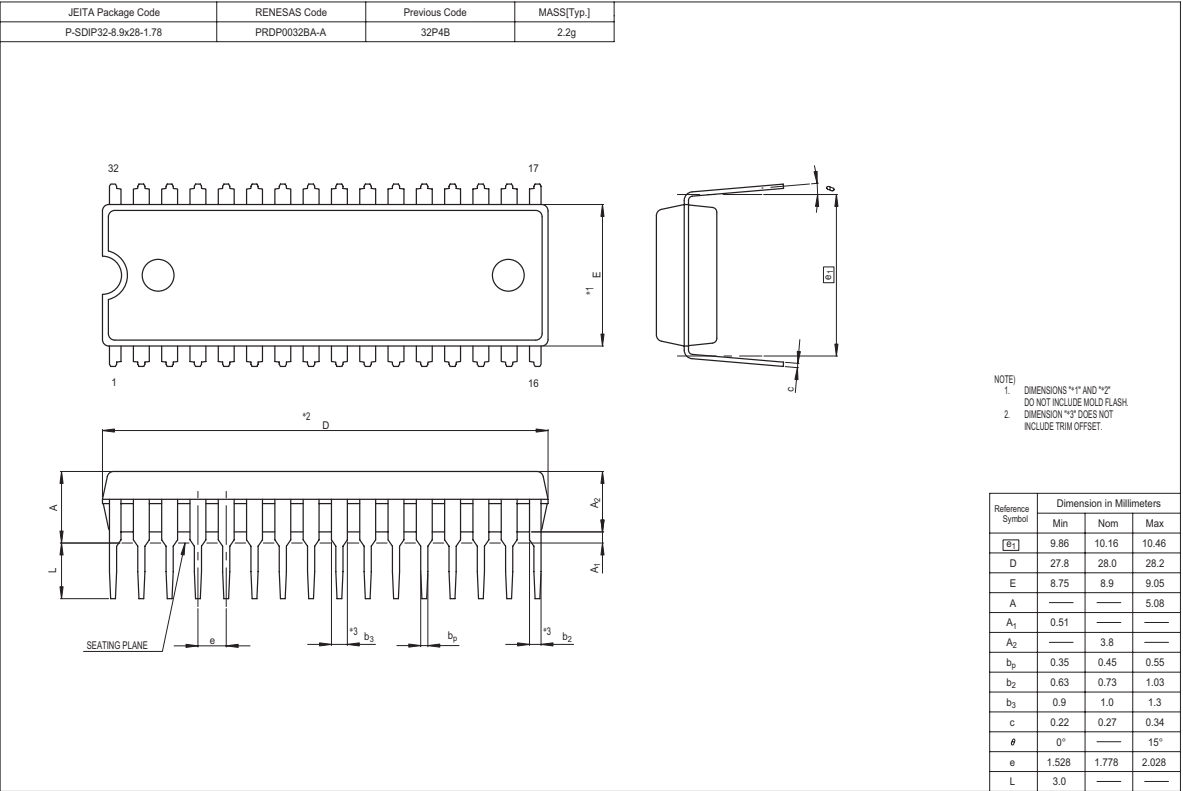
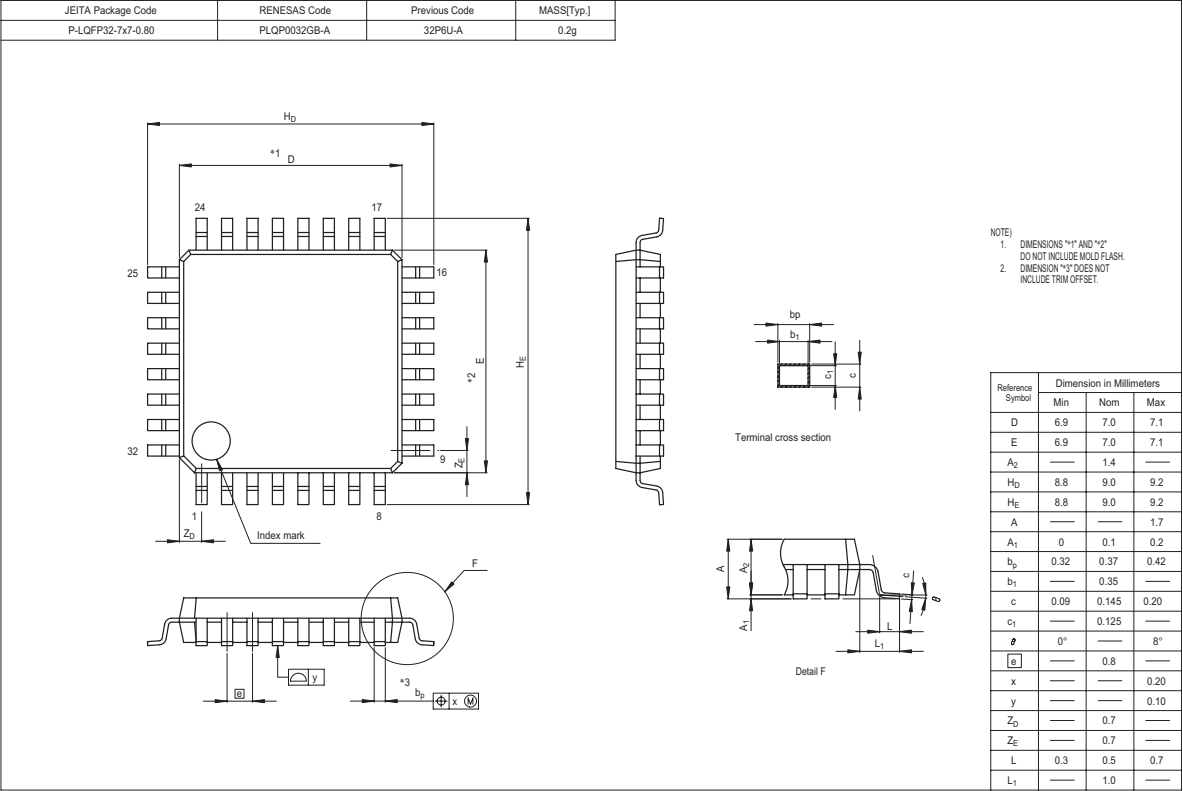
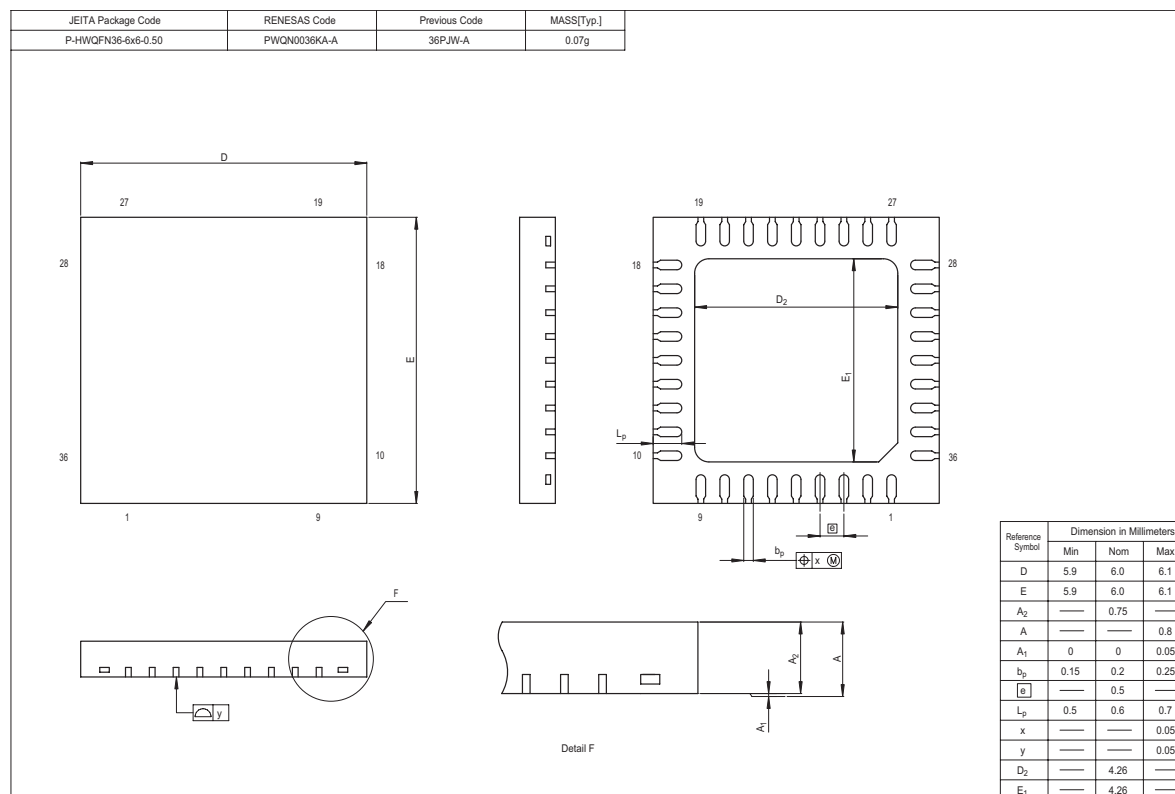


Fig. 107 Timing chart

PACKAGE OUTLINE

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.





APPENDIX

NOTES ON PROGRAMMING

1. Processor Status Register

(1) Initializing of processor status register

Flags which affect program execution must be initialized after a reset.

In particular, it is essential to initialize the T and D flags because they have an important effect on calculations. Initialize these flags at beginning of the program.

<Reason>

After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1".

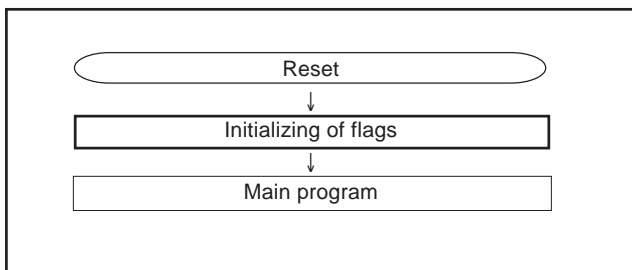


Fig. 1 Initialization of processor status register

(2) How to reference the processor status register

To reference the contents of the processor status register (PS), execute the **PHP** instruction once then read the contents of (S+1). If necessary, execute the **PLP** instruction to return the PS to its original status.

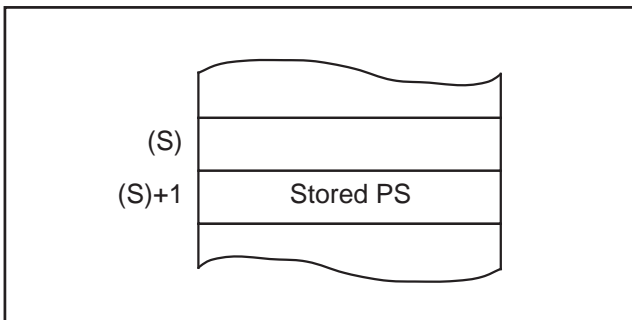


Fig.2 Stack memory contents after PHP instruction execution

2. Decimal calculations

(1) Execution of decimal calculations

The **ADC** and **SBC** are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to "1" with the **SED** instruction. After executing the **ADC** or **SBC** instruction, execute another instruction before executing the **SEC**, **CLC**, or **CLD** instruction.

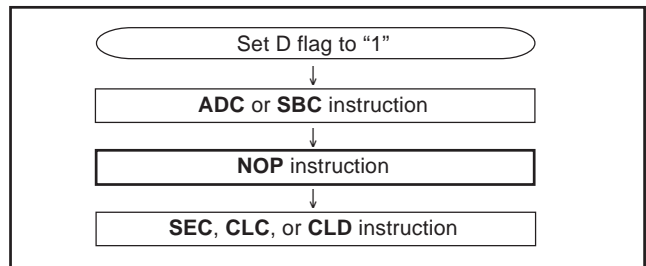


Fig. 3 Instructions for decimal calculations

(2) Notes on status flag in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a **ADC** or **SBC** instruction is executed.

The carry flag (C) is set to "1" if a carry is generated as a result of the calculation, or is cleared to "0" if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to "0" before each calculation. To check for a borrow, the C flag must be initialized to "1" before each calculation.

3. JMP instruction

When using the **JMP** instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

4. Multiplication and Division Instructions

- (1) The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- (2) The execution of these instructions does not change the contents of the processor status register.

5. Read-modify-write instruction

Do not execute a read-modify-write instruction to the read invalid address (SFR).

The read-modify-write instruction operates in the following sequence: read one-byte of data from memory, modify the data, write the data back to original memory. The following instructions are classified as the read-modify-write instructions in the 740 Family.

- (1) Bit management instructions: CLB, SEB
- (2) Shift and rotate instructions: ASL, LSR, ROL, ROR, RRF
- (3) Add and subtract instructions: DEC, INC
- (4) Logical operation instructions (1's complement): COM

Add and subtract/logical operation instructions (ADC, SBC, AND, EOR, and ORA) when T flag = "1" operate in the way as the read-modify-write instruction. Do not execute the read invalid SFR.

<Reason>

When the read-modify-write instruction is executed to read invalid SFR, the instruction may cause the following consequence: the instruction reads unspecified data from the area due to the read invalid condition. Then the instruction modifies this unspecified data and writes the data to the area. The result will be random data written to the area or some unexpected event.

NOTES ON PERIPHERAL FUNCTIONS

Notes on I/O Ports

1. Port direction register

- Set bits 6 and 7 of port P2 direction register to "1".
- Set bits 5 and 6 of port P3 direction register to "1".

2. Interrupt edge selection register

Set bit 2 of interrupt edge selection register to "1".

3. Be sure to set bit 1 of port P1P3 control register (address 001716) to "0".

4. Port P0P3 drive capacity control register

The number of LED drive port (drive capacity is HIGH) is 8.

5. Pull-up control register

When using each port which built in pull-up resistor as an output port, the pull-up control bit of corresponding port becomes invalid, and pull-up resistor is not connected.

<Reason>

Pull-up control is effective only when each direction register is set to the input mode.

6. Notes in stand-by state

In stand-by state*1 for low-power dissipation, do not make input levels of an input port and an I/O port "undefined".

Pull-up (connect the port to Vcc) or pull-down (connect the port to Vss) these ports through a resistor.

When determining a resistance value, note the following points:

- External circuit
- Variation of output levels during the ordinary operation
When using a built-in pull-up resistor, note on varied current values:
- When setting as an input port : Fix its input level
- When setting as an output port : Prevent current from flowing out to external.

<Reason>

The output transistor becomes the OFF state, which causes the ports to be the high-impedance state. Note that the level becomes "undefined" depending on external circuits.

Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of an input port and an I/O port are "undefined". This may cause power source current.

*1 stand-by state : the stop mode by executing the **STP** instruction
the wait mode by executing the **WIT** instruction

7. Modifying output data with bit handling instruction

When the port latch of an I/O port is modified with the bit handling instruction*1, the value of an unspecified bit may change.

<Reason>

I/O ports can be set to input mode or output mode in byte units. When the port register is read or written, the following will be operated:

- Port as input mode
Read: Read the pin level
Write: Write to the port latch
- Port as output mode
Read: Read the port latch or peripheral function output (specifications vary depending on the port)
Write: Write to the port latch (output the content of the port latch from the pin)

Meanwhile, the bit handling instructions are the read-modifywrite instructions*2. Executing the bit handling instruction to the port register allows reading and writing a bit unspecified with the instruction at the same time.

If an unspecified bit is set to input mode, the pin level is read and the value is written to the port latch. At this time, if the original content of the port latch and the pin level do not match, the content of the port latch changes.

If an unspecified bit is set to output mode, the port latch is normally read, but the peripheral function output is read in some ports and the value is written to the port latch. At this time, if the original content of the port latch and the peripheral function output do not match, the content of the port latch changes.

*1 Bit handling instructions: **CLB**, **SEB**

*2 Read-modify-write instruction: Reads 1-byte of data from memory, modifies the data, and writes 1-byte of the data to the original memory.

8. Direction register

The values of the port direction registers cannot be read.

That is, it is impossible to use the **LDA** instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as **BBC** and **BBS**.

It is also impossible to use bit operation instructions such as **CLB** and **SEB** and read-modify-write instructions of direction registers for calculations such as **ROR**.

For setting direction registers, use the **LDM** instruction, **STA** instruction, etc.

Termination of Unused Pins

1. Terminate unused pins

Perform the following wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

(1) I/O ports

Set the I/O ports for the input mode and connect each pin to VCC or VSS through each resistor of 1 k Ω to 10 k Ω . The port which can select a built-in pull-up resistor can also use the built-in pull-up resistor.

When using the I/O ports as the output mode, open them at "L" or "H".

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

2. Termination remarks

(1) I/O ports setting as input mode

[1] Do not open in the input mode.

<Reason>

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination (1) shown on the above "1. Terminate unused pins".

[2] Do not connect to VCC or VSS directly.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur.

[3] Do not connect multiple ports in a lump to VCC or VSS through a resistor.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

Notes on Interrupts

1. Change of relevant register settings

When not requiring for the interrupt occurrence synchronous with the following case, take the sequence shown in Fig. 4.

- When switching external interrupt active edge
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

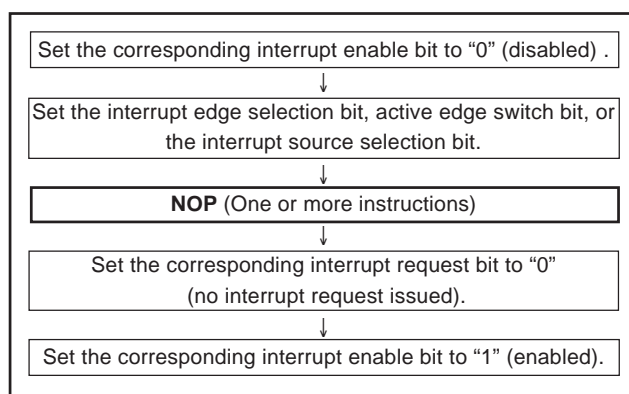


Fig. 4 Sequence of changing relevant register

<Reason>

When setting the followings, the interrupt request bit of the corresponding interrupt may be set to "1".

- When switching external interrupt active edge
 - INT0 interrupt edge selection bit
(bit 0 of Interrupt edge selection register (address 003A16))
 - INT1 interrupt edge selection bit
(bit 1 of Interrupt edge selection register)
 - CNTR0 active edge switch bit
(bit 2 of timer X mode register (address 002B16))
 - Capture 0 interrupt edge selection bit
(bits 1 and 0 of capture mode register (address 002016))
 - Capture 1 interrupt edge selection bit
(bits 3 and 2 of capture mode register)

2. Check of interrupt request bit

When executing the **BBC** or **BBS** instruction to determine an interrupt request bit immediately after this bit is set to "0", take the following sequence.

<Reason>

If the **BBC** or **BBS** instruction is executed immediately after an interrupt request bit is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

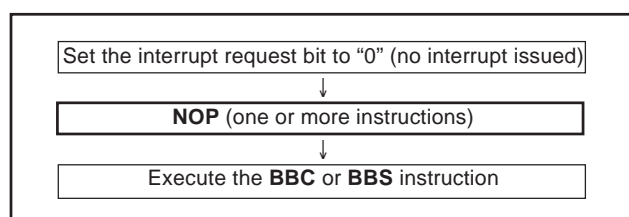


Fig. 5 Sequence of check of interrupt request bit

3. Interrupt discrimination bit

Use an LDM instruction to clear to "0" an interrupt discrimination bit.

LDM #0000XXXX, \$0B

Set the following values to "X"

"0": an interrupt discrimination bit to clear

"1": other interrupt discrimination bits

Ex.) When a key-on wakeup interrupt discrimination bit is cleared; LDM #00001110 and \$0B.

4. Interrupt discrimination bit and interrupt request bit

For key-on wakeup, UART1 bus collision detection, A/D conversion and Timer 1 interrupt, even if each interrupt valid bit (interrupt source set register (address 000A16)) is set "0: Invalid", each interrupt discrimination bit (interrupt source discrimination register (address 000B16)) is set to "1: interrupt occurs" when corresponding interrupt request occurs.

But corresponding interrupt request bit (interrupt request registers 1, 2 (addresses 003C16, 003D16)) is not affected.

Notes on Timers

- When n (0 to 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.
- When a count source of timer X, timer A or timer B is switched, stop a count of the timer.

Notes on Timer X

1. CNTR0 interrupt active edge selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit (bit 2 of timer X mode register (address 002B16)).

When this bit is "0", the CNTR0 interrupt request bit is set to "1" at the falling edge of CNTR0 pin input signal. When this bit is "1", the CNTR0 interrupt request bit is set to "1" at the rising edge of CNTR0 pin input signal.

2. Timer X count source selection

The $f(X_{IN})$ (frequency not divided) can be selected by the timer X count source selection bits (bits 1 and 0 of timer count source set register (address 002A16)) only when the ceramic oscillation or the on-chip oscillator is selected.

Do not select it for the timer X count source at the RC oscillation.

3. Pulse output mode

Set the direction register of port P14, which is also used as CNTR0 pin, to output.

When the TXOUT pin is used, set the direction register of port P03, which is also used as TXOUT pin, to output.

4. Pulse width measurement mode

Set the direction register of port P14, which is also used as CNTR0 pin, to input.

Notes on Timer A, B

1. Setting of timer value

When "1: Write to only latch" is set to the timer A (B) write control bit (bit 0 (bit 2) of timer X mode register (address 001D16)), written data to timer register is set to only latch even if timer is stopped or operating. Accordingly, in order to set the initial value for timer when it is stopped, set "0: Write to latch and timer simultaneously" to timer A (B) write control bit.

2. Read/write of timer A

Stop timer A to read/write its data in the following state;

X_{IN} oscillation selected by clock division ratio selection bits (bits 7 and 6 of CPU mode register (address 003B16)), and the on-chip oscillator output is selected as the timer A count source.

3. Read/write of timer B

Stop timer B to read/write its data in the following state;

X_{IN} oscillation selected by clock division ratio selection bits, the timer A underflow is selected as the timer B count source, and the on-chip oscillator output is selected as the timer A count source.

Notes on Output Compare

- When the selected source timer of each compare channel is stopped, written data to compare register is loaded to the compare latch simultaneously.
- Do not write the same data to both of compare latch x0 (x=0, 1, 2, 3) and x1.
- When setting value of the compare register is larger than timer setting value, compare match signal is not generated. Accordingly, the output waveform is fixed to "L" or "H" level. However, when setting value of another compare register is smaller than timer setting value, this compare match signal is generated. Accordingly, if the corresponding compare latch y (y=00, 01, 10, 11, 20, 21, 30, 31) interrupt source bit is set to "1" (valid), compare match interrupt request occurs.
- When the compare x trigger enable bit is cleared to "0" (disabled), the match trigger to the waveform output circuit is disabled. Accordingly, the output waveform can be fixed to "L" or "H" level. However, in this case, the compare match signal is generated. Accordingly, if the corresponding compare latch y (y=00, 01, 10, 11, 20, 21, 30, 31) interrupt source bit is set to "1" (valid), compare match interrupt request occurs.

Notes on Input Capture

1. If the capture trigger is input while the capture register (low-order and high-order) is in read, captured value is changed between high-order reading and low-order reading. Accordingly, some countermeasure by program is recommended, for example comparing the values that twice of read.
2. Timer A cannot be used for the capture source timer in the following state;
 - XIN oscillation selected by clock division ratio selection bits (bits 7 and 6 of CPU mode register (address 003B16))
 - Timer A count source: On-chip oscillator output.
 Timer B cannot be used for the capture source timer in the following state;
 - XIN oscillation selected by clock division ratio selection bits
 - Timer B count source: Timer A underflow
 - Timer A count source: On-chip oscillator output.
3. As shown below, when the capture input is performed to both capture latch 00 and 01 at the same time, the value of capture 0 status bit (bit 4 of capture/compare status register (address 002216)) is undefined (same as capture 1).
 - When "1" is written to capture latch 00 software trigger bit (bit 0 of capture software trigger register (address 001316)) and capture latch 01 software trigger bit (bit 1 of capture software trigger register) at the same time
 - When external trigger of capture latch 00 and software trigger of capture latch 01 occur at the same time
 - When external trigger of capture latch 01 and software trigger of capture latch 00 occur at the same time
4. When the capture interrupt is used as the interrupt for return from stop mode, set the capture 0 noise filter clock selection bits (bits 5 and 4 of capture mode register (address 002016)) to "00 (Filter stop)" (same as capture 1).

Notes on Serial I/Oi (i=1, 2)

1. Clock synchronous serial I/O
 - (1) When the transmit operation is stopped, clear the serial I/Oi enable bit and the transmit enable bit to "0" (serial I/Oi and transmit disabled).

<Reason>

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/Oi enable bit is cleared to "0" (serial I/Oi disabled), the internal transmission is running (in this case, since pins TxDi, RxDi, SCLKi, and $\overline{\text{SRDYi}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/Oi enable bit is set to "1" at this time, the data during internally shifting is output to the TxDi pin and an operation failure occurs.
 - (2) When the receive operation is stopped, clear the receive enable bit to "0" (receive disabled), or clear the serial I/Oi enable bit to "0" (serial I/Oi disabled).
 - (3) When the transmit/receive operation is stopped, clear both the transmit enable bit and receive enable bit to "0" (transmit and receive disabled) simultaneously. (any one of data transmission and reception cannot be stopped.)

<Reason>

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception.

If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized. In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit cannot be initialized even if the serial I/Oi enable bit is cleared to "0" (serial I/Oi disabled) (same as (1)).
 - (4) When signals are output from the $\overline{\text{SRDYi}}$ pin on the reception side by using an external clock, set all of the receive enable bit, the $\overline{\text{SRDYi}}$ output enable bit, and the transmit enable bit to "1".
 - (5) When the $\overline{\text{SRDYi}}$ signal input is used, set the using pin to the input mode before data is written to the transmit/receive buffer register.

2. UART

When the transmit operation is stopped, clear the transmit enable bit to "0" (transmit disabled).

<Reason>

Same as (1) shown on the above "1. Clock synchronous serial I/O". When the receive operation is stopped, clear the receive enable bit to "0" (receive disabled).

When the transmit/receive operation is stopped, clear the transmit enable bit to "0" (transmit disabled) and receive enable bit to "0" (receive disabled).

3. Notes common to clock synchronous serial I/O and UART

- (1) Set the serial I/Oi (i=1, 2) control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0."

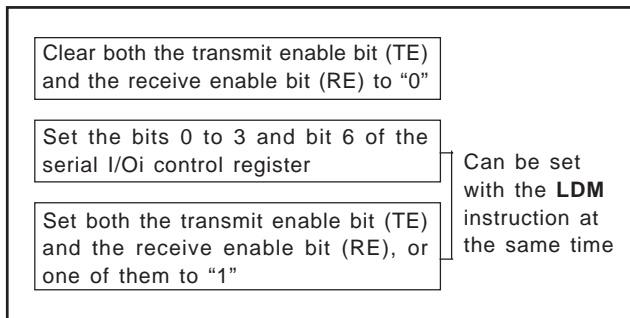


Fig. 6 Sequence of setting serial I/Oi control register again

- (2) The transmit shift completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.
- (3) When data transmission is executed at the state that an external clock input is selected as the synchronous clock, set "1" to the transmit enable bit while the SCLKi is "H" state. Also, write to the transmit buffer register while the SCLKi is "H" state.
- (4) When the transmit interrupt is used, set as the following sequence.
- ① Serial I/Oi transmit interrupt enable bit is set to "0" (disabled).
 - ② Serial I/Oi transmit enable bit is set to "1".
 - ③ Serial I/Oi transmit interrupt request bit is set to "0" after 1 or more instructions have been executed.
 - ④ Serial I/Oi transmit interrupt enable bit is set to "1" (enabled).
- <Reason>
When the transmit enable bit is set to "1", the transmit buffer empty flag and transmit shift completion flag are set to "1". Accordingly, even if the timing when any of the above flags is set to "1" is selected for the transmit interrupt source, interrupt request occurs and the transmit interrupt request bit is set.
- (5) Write to the baud rate generator (BRGi) while the transmit/receive operation is stopped.

Notes on Serial I/O1

1. I/O pin function when serial I/O1 is enabled.

The pin functions of P12/SCLK1 and P13/SRDY1 are switched to as follows according to the setting values of a serial I/O1 mode selection bit (bit 6 of serial I/O1 control register (address 001A16)) and a serial I/O1 synchronous clock selection bit (bit 1 of serial I/O1 control register).

(1) Serial I/O1 mode selection bit → "1" :

Clock synchronous type serial I/O is selected.

- Setup of a serial I/O1 synchronous clock selection bit
"0" : P12 pin turns into an output pin of a synchronous clock.
"1" : P12 pin turns into an input pin of a synchronous clock.
- Setup of a SRDY1 output enable bit (SRDY)
"0" : P13 pin can be used as a normal I/O pin.
"1" : P13 pin turns into a SRDY1 output pin.

(2) Serial I/O1 mode selection bit → "0" :

Clock asynchronous (UART) type serial I/O is selected.

- Setup of a serial I/O1 synchronous clock selection bit
"0" : P12 pin can be used as a normal I/O pin.
"1" : P12 pin turns into an input pin of an external clock.
- When clock asynchronous (UART) type serial I/O is selected, it functions P13 pin. It can be used as a normal I/O pin.

Note on Bus Collision Detection

When serial I/O1 is operating at half-duplex communication, set bus collision detection interrupt to be disabled.

Notes on Serial I/O2

1. I/O pin function when serial I/O2 is enabled

The pin functions of P06/SCLK2 and P07/SRDY2 are switched to as follows according to the setting values of a serial I/O2 mode selection bit (bit 6 of serial I/O2 control register (address 003016)) and a serial I/O2 synchronous clock selection bit (bit 2 of serial I/O2 control register).

(1) Serial I/O2 mode selection bit → "1" :

Clock synchronous type serial I/O is selected.

- Setup of a serial I/O2 synchronous clock selection bit
"0" : P06 pin turns into an output pin of a synchronous clock.
"1" : P06 pin turns into an input pin of a synchronous clock.
- Setup of a SRDY2 output enable bit (SRDY)
"0" : P07 pin can be used as a normal I/O pin.
"1" : P07 pin turns into a SRDY2 output pin.

(2) Serial I/O2 mode selection bit → "0" :

Clock asynchronous (UART) type serial I/O is selected.

- Setup of a serial I/O2 synchronous clock selection bit
"0" : P06 pin can be used as a normal I/O pin.
"1" : P06 pin turns into an input pin of an external clock.
- When clock asynchronous (UART) type serial I/O is selected, it functions P07 pin. It can be used as a normal I/O pin.

Notes on A/D conversion

1. Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μ F to 1 μ F. Further, be sure to verify the operation of application products on the user side.

<Reason>

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A/D conversion/comparison precision to be worse.

2. Clock frequency during A/D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. This may cause the A/D conversion precision to be worse. Accordingly, set $f(XIN)$ in order that the A/D conversion clock is 250 kHz or over during A/D conversion.

3. A/D conversion clock selection

Select $f(XIN)/2$ as an A/D conversion clock by setting the A/D conversion clock selection bit (bit 3 of A/D control register (address 003416)) when RC oscillation is used.

The $f(XIN)$ can be also used as an A/D conversion clock only when ceramic oscillation or on-chip oscillator is used.

4. Read A/D conversion register

• 8-bit read

Read only the A/D conversion low-order register (address 003516).

• 10-bit read

Read the A/D conversion high-order register (address 003616) first, and then, read the A/D conversion low-order register (address 003516).

In this case, the high-order 6 bits of address 003616 returns "0" when read.

5. A/D conversion accuracy

As for AD translation accuracy, on the following operating conditions, accuracy may become low.

- (1) Since the analog circuit inside a microcomputer becomes sensitive to noise when V_{REF} voltage is set up lower than V_{CC} voltage, accuracy may become low rather than the case where V_{REF} voltage and V_{CC} voltage are set up to the same value..
- (2) When V_{REF} voltage is lower than [3.0 V], the accuracy at the low temperature may become extremely low compared with that at room temperature. When the system would be used at low temperature, the use at $V_{REF}=3.0$ V or more is recommended.

Notes on Watchdog Timer

1. The watchdog timer is operating during the wait mode. Write data to the watchdog timer control register to prevent timer underflow.

2. The watchdog timer stops during the stop mode. However, the watchdog timer is running during the oscillation stabilizing time after the **STP** instruction is released. In order to avoid the underflow of the watchdog timer, the watchdog timer count source selection bit (bit 7 of watchdog timer control register (address 003916)) before executing the **STP** instruction.

3. The **STP** instruction function selection bit (bit 6 of watchdog timer control register (address 003916)) can be rewritten only once after releasing reset. After rewriting it is disable to write any data to this bit.

Notes on RESET pin

1. Connecting capacitor

In case where the \overline{RESET} signal rise time is long, connect a ceramic capacitor or others across the \overline{RESET} pin and the V_{SS} pin. And use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

<Reason>

If the several nanosecond or several ten nanosecond impulse noise enters the \overline{RESET} pin, it may cause a microcomputer failure.

Notes on Clock Generating Circuit

1. Switch of ceramic and RC oscillations

After releasing reset, the oscillation mode selection bit (bit 5 of CPU mode register (address 003B16)) is "0" (ceramic oscillation selected). When the RC oscillation is used, after releasing reset, set this bit to "1".

2. Double-speed mode

The double-speed mode can be used only when a ceramic oscillation is selected. Do not use it when an RC oscillation is selected.

3. CPU mode register

Oscillation mode selection bit (bit 5), processor mode bits (bits 1 and 0) of CPU mode register (address 003B16) are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by erroneously writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting, it is disabled to write any data to the bit. (The emulator MCU "M37542RSS" is excluded.)

Also, when the read-modify-write instructions (SEB, CLB, etc.) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

4. Clock division ratio, XIN oscillation control, on-chip oscillator control

The state transition shown in Fig. 82 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), on-chip oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 82.

5. On-chip oscillator operation

When the MCU operates by the on-chip oscillator for the main clock, connect XIN pin to VCC through a 1 kΩ to 10 kΩ resistor and leave XOUT pin open.

The clock frequency of the on-chip oscillator depends on the supply voltage and the operation temperature range.

Be careful that this margin of frequencies when designing application products.

6. Ceramic resonator

When the ceramic resonator is used for the main clock, connect the ceramic resonator and the external circuit to pins XIN and XOUT at the shortest distance. Externally connect a damping resistor Rd depending on the oscillation frequency. A feedback resistor is built-in.

Use the resonator manufacturer's recommended value because constants such as capacitance depend on the resonator.

7. RC oscillation

When the RC oscillation is used for the main clock, connect the XIN pin and XOUT pin to the external circuit of resistor R and the capacitor C at the shortest distance.

The frequency is affected by a capacitor, a resistor and a microcomputer.

So, set the constants within the range of the frequency limits.

8. External clock

When the external signal clock is used for the main clock, connect the XIN pin to the clock source and leave XOUT pin open.

Select "0" (ceramic oscillation) to oscillation mode selection bit.

9. Count source (Timer 1, Timer A, Timer B, Timer X, Serial I/O, Serial I/O2, A/D converter, Watchdog timer)

The count sources of these functions are affected by the clock division selection bit of the CPU mode register.

The f(XIN) clock is supplied to the watchdog timer when selecting f(XIN) as the CPU clock.

The on-chip oscillator output is supplied to these functions when selecting the on-chip oscillator output as the CPU clock.

However, the watchdog timer is also affected by the function set ROM.

Notes on Oscillation Control

1. Oscillation stop detection circuit

(1) When the stop mode is used, set the oscillation stop detection function to "invalid".

(2) When the ceramic or RC oscillation is stopped by the XIN oscillation control bit (bit 4 of CPU mode register (address 003B16)), set the oscillation stop detection function to "invalid".

2. Stop mode

(1) When the stop mode is used, set the oscillation stop detection function to "invalid".

(2) When the stop mode is used, set "0" (**STP** instruction enabled) to the **STP** instruction function selection bit of the watchdog timer control register (bit 6 of watchdog timer control register (address 003916)).

(3) The oscillation stabilizing time after release of **STP** instruction can be selected from "set automatically"/"not set automatically" by the oscillation stabilizing time set bit after release of the **STP** instruction (bit 0 of MISRG (address 003816)). When "0" is set to this bit, "0116" is set to timer 1 and "FF16" is set to prescaler 1 automatically at the execution of the **STP** instruction. When "1" is set to this bit, set the wait time to timer 1 and prescaler 1 according to the oscillation stabilizing time of the oscillation. Also, when timer 1 is used, set values again to timer 1 and prescaler 1 after system is returned from the stop mode.

(4) Do not execute the **STP** instruction during the A/D conversion.

Notes on On-chip Oscillation Division Ratio

- When the clock division ratio is switched from f(XIN) to on-chip oscillator by the clock division ratio selection bits (bits 7 and 6 of CPU mode register (address 003B16)), the on-chip oscillator division ratio (bits 1 and 0 of on-chip oscillator division ratio selection register (address 003716)) is "102" (on-chip oscillator middle-speed mode (ROSC/8)).

Notes on Oscillation Stop Detection Circuit

1. After the reset by the oscillation stop detection, the value of following bits are retained, not initialized.

- Ceramic or RC oscillation stop detection function active bit
Bit 1 of MISRG (address 003B16)
- Oscillation stop detection status bit
Bit 3 of MISRG

2. Oscillation stop detection status bit is initialized ("0") by the following operation.

- External reset
- Write "0" data to the ceramic or RC oscillation stop detection function active bit.

3. The oscillation stop detection circuit is not included in the emulator MCU "M37542RSS".

Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.

In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

NOTES ON HARDWARE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μ F to 0.1 μ F is recommended.

NOTES ON QzROM

Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.

Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Precautions Regarding Overvoltage

Make sure that voltage exceeding the Vcc pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in Figure below does not occur for CNVss pin (VPP power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

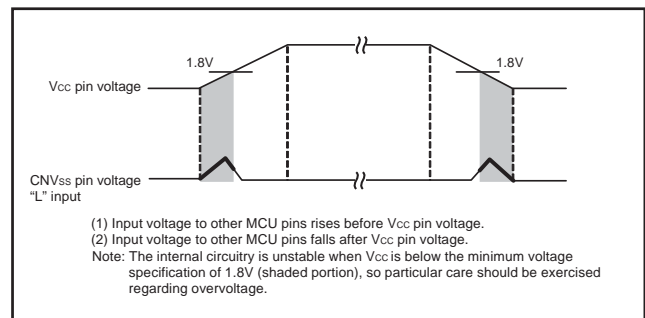


Fig. 7 Timing Diagram (bold-lined periods are applicable)

Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "0016" and "FF16" can not be accepted.
- Set "FF16" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF16" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

Data Required For QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:

1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (<http://www.renesas.com/homepage.jsp>).

Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

REVISION HISTORY

7546 Group Datasheet

| Rev. | Date | Description | |
|------|--------------|--|---|
| | | Page | Summary |
| 1.00 | Oct 14, 2005 | – | First Edition issued |
| 1.10 | Jun 05, 2006 | – 1 2, 3 4 9 22 39 41 56 62 67 74 75 76 77 78, 79 80 81 84 | <p>“Preliminary” eliminated.</p> <p>Power dissipation added.</p> <p>Fig.1, Fig.2 and Fig.3: part numbers added.</p> <p>Power source voltage (at on-chip oscillator) and power dissipation added.</p> <p>Memory expansion plan: “Under development” eliminated.</p> <p>Notes on use (2): \$0Bn → \$0B</p> <p>Notes on Input Capture; 2nd note: some description added.</p> <p>Block diagram of capture channel 0: address of capture pointer revised.</p> <p>Low Voltage Detection Circuit: bit number of the function set ROM data 0 revised.</p> <p>State transition: (4) revised.</p> <p>Wiring for the VPP pin of the QzPROM revised.</p> <p>Electrical characteristics (1) VRAM Min. value is added.</p> <p>Electrical characteristics (2)</p> <ul style="list-style-type: none"> - Parameter The condition is added. - Limits Typ. and Max. values are changed. <p>A/D Converter characteristics</p> <ul style="list-style-type: none"> - Absolute accuracy Max. value is revised. <p>Power-on reset circuit characteristics and Low voltage detection circuit added.</p> <p>Timing requirements is added.</p> <p>Switching characteristics is added.</p> <p>Timing chart added.</p> <p>BRK instruction eliminated.</p> |
| 1.20 | Aug 30, 2006 | 9 54, 91 59, 92 70 75 77 91 | <p>Table 3: ROM size revised and note added.</p> <p>Notes on watchdog timer: note 3 revised.</p> <p>Notes on clock generating circuit: note added.</p> <p>5. Setup for I/O ports: Note eliminated.</p> <p>Electrical characteristics (2)</p> <ul style="list-style-type: none"> - Low voltage detection circuit self consumption current added. <p>Low voltage detection circuit characteristics.</p> <ul style="list-style-type: none"> - Unit of VLVD mV → \underline{V} <p>(1) Analog input pin: description revised.</p> |
| 1.21 | Nov 30, 2006 | 73 | All f(XIN): VCC conditi on added. |
| 1.22 | Mar 13, 2009 | 19 21 22 to 27 67 to 72 73 74 78 | <p>Fig. 18 (9), (12) revised</p> <p>Table 7 XIN and XOUT added</p> <p>“Interrupts” revised</p> <p>“QzROM Writing Mode” added</p> <p>“Processor Status Register” revised</p> <p>“(4) Writng to CNVss pin” revised</p> <p>“NOTES ON QzROM” added</p> |

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|------------------|----------------------|
| REVISION HISTORY | 7546 Group Datasheet |
|------------------|----------------------|

| Rev. | Date | Description | |
|------|--------------|-------------|---|
| | | Page | Summary |
| 1.22 | Mar 13, 2009 | 85 | <ul style="list-style-type: none"> - Power-on reset circuit characteristics: TW(VPOR) Limits Max. and Min. values changed. - Low voltage detection circuit characteristics: TW(VLVD) and TW (VLVD -VDET) eliminated. VDET- → VDET, V(VDET+-VDET-) deleted. - Fig. 105 revised. |
| | | 92 | <ul style="list-style-type: none"> - "1. Processor Status Register" revised - The last Fig. 2 Sequence of PLP Instruction execution deleted. - Figure title of Fig. 3 revised |
| | | 93 | "7. Modifying output data with bit managing instruction" revised. |
| | | 100 | <ul style="list-style-type: none"> - "Precautions Regarding Overvoltage" added - "Notes On QzROM Writing Orders" revised. |

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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
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Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
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1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
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Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
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