

1. General description

Planar passivated high commutation three quadrant triac in a SOT404 (D2PAK) surface mountable plastic package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series B" triac will commute the full RMS current at the maximum rated junction temperature without the aid of a snubber.

2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High voltage capability
- Less sensitive gate for highest noise immunity
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- Electronic thermostats (heating and cooling)
- High power motor controls e.g. washing machines and vacuum cleaners
- Rectifier-fed DC inductive loads e.g. DC motors and solenoids

4. Quick reference data

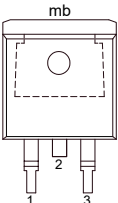
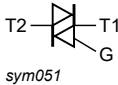
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 100\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	12	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	100	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 16.7\text{ ms}$	-	-	110	A
T_j	junction temperature		-	-	125	$^{\circ}\text{C}$
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_2 + G+$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	2	-	50	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	2	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	2	-	50	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	-	60	mA
V_T	on-state voltage	$I_T = 15\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	1.3	1.6	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential circuit; gate open circuit	1000	2000	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 12\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit	30	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 D2PAK (SOT404)	 sym051
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BTA312B-600B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		-	600	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{mb} ≤ 100 °C; Fig. 1; Fig. 2; Fig. 3	-	12	A
I _{TSM}	non-repetitive peak on-state current	full sine wave; T _{j(init)} = 25 °C; t _p = 20 ms; Fig. 4; Fig. 5	-	100	A
		full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms	-	110	A
I ² t	I ² t for fusing	t _p = 10 ms; SIN	-	50	A ² s
dI _T /dt	rate of rise of on-state current	I _G = 100 mA	-	100	A/μs
I _{GM}	peak gate current		-	2	A
P _{GM}	peak gate power		-	5	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.5	W
T _{stg}	storage temperature		-40	150	°C
T _j	junction temperature		-	125	°C

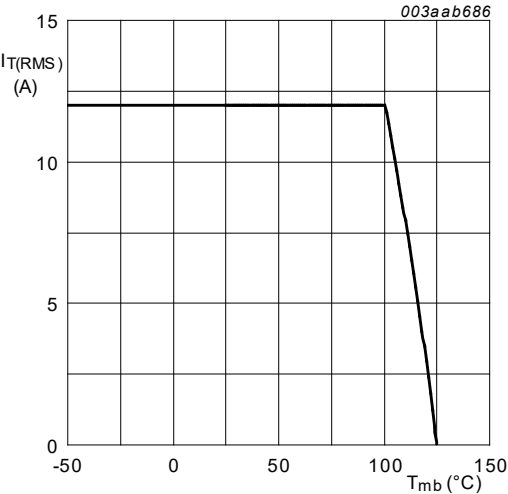


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

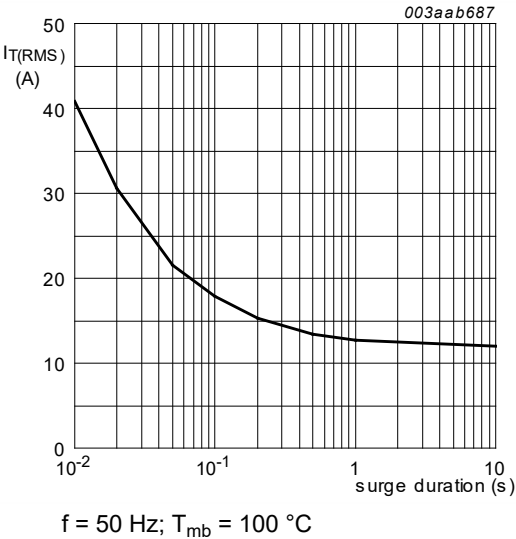
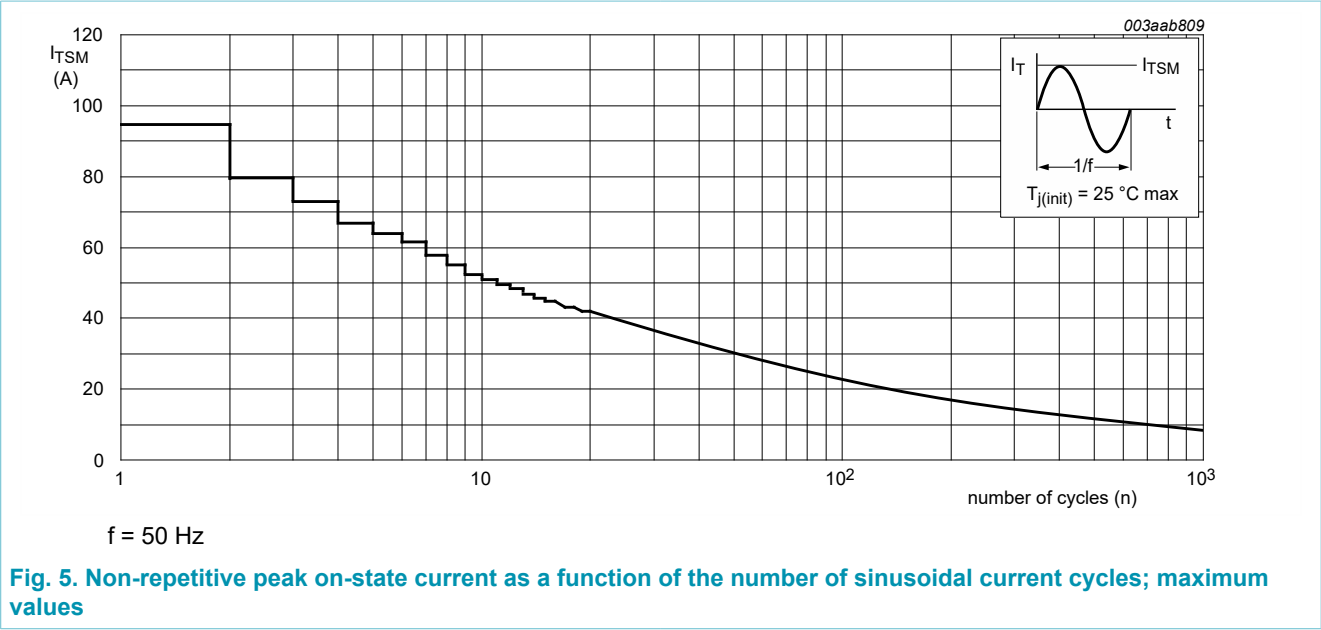


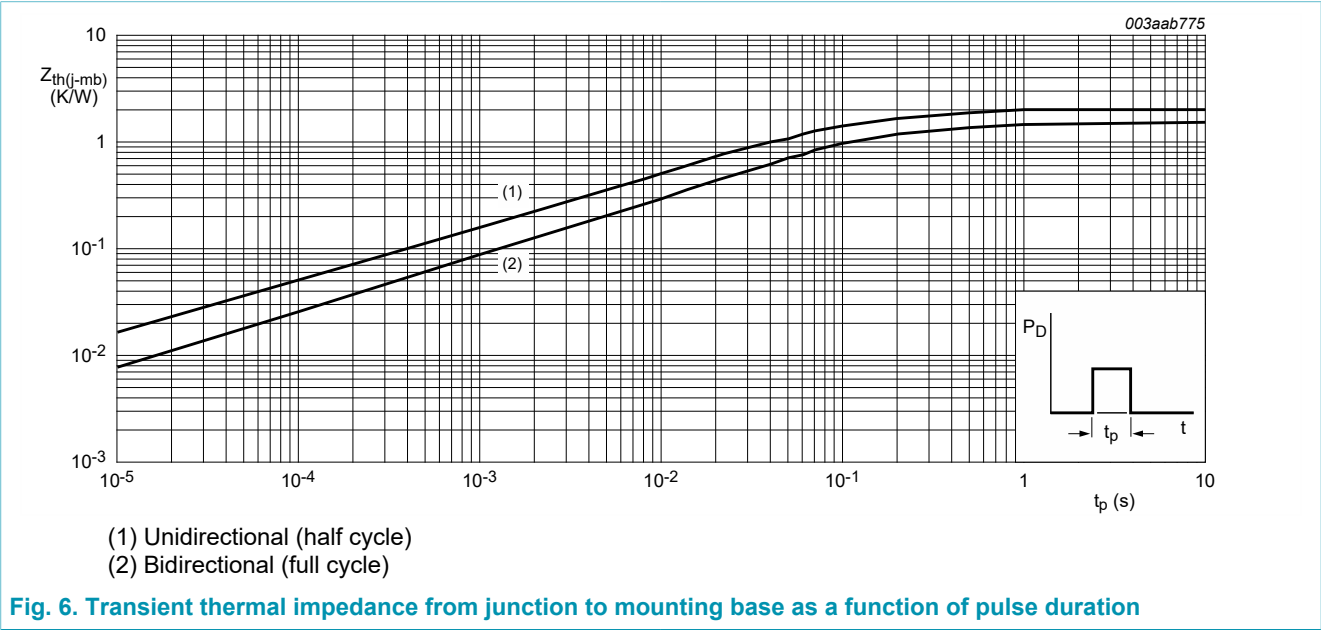
Fig. 2. RMS on-state current as a function of surge duration; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

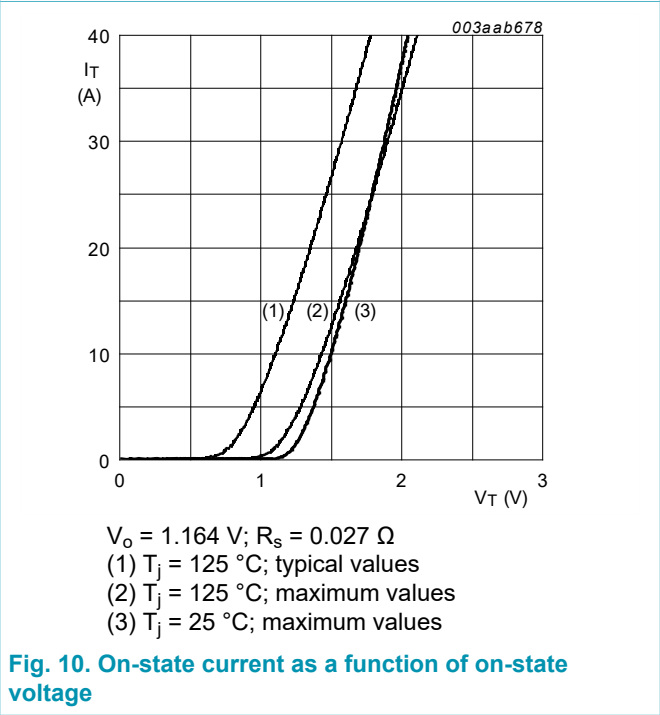
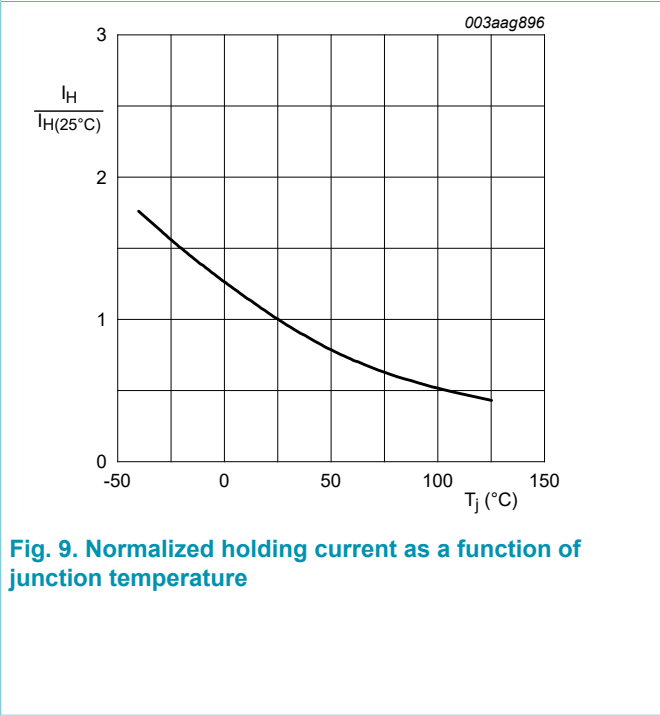
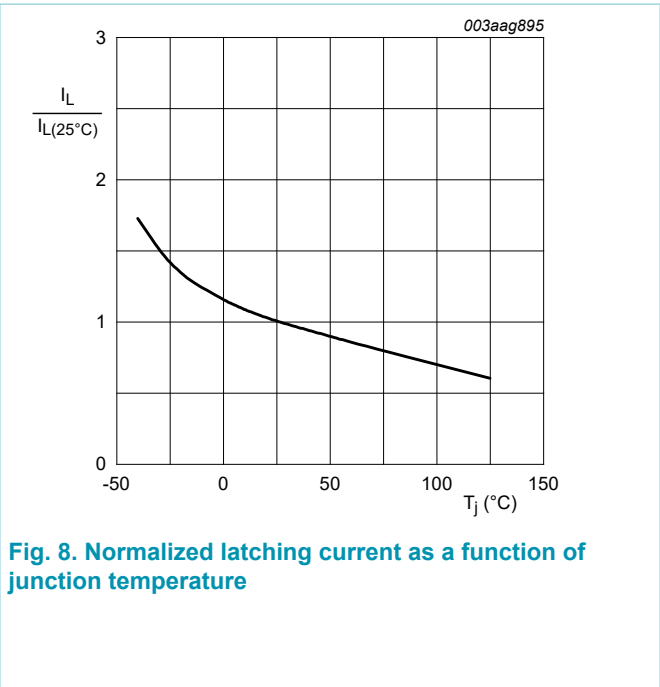
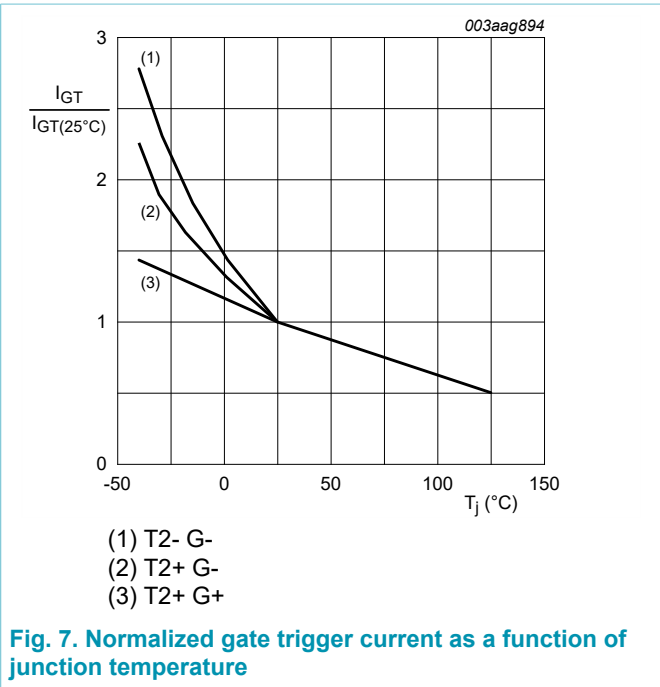
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	full cycle; Fig. 6		-	-	1.5	K/W
		half cycle; Fig. 6		-	-	2	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	in free air		-	60	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	2	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	2	-	50	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	2	-	50	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	-	60	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	-	90	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	-	60	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	-	60	mA
V_T	on-state voltage	$I_T = 15\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	1.3	1.6	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	0.8	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 11	0.25	0.4	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential circuit; gate open circuit	1000	2000	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 12\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit	30	-	-	A/ms



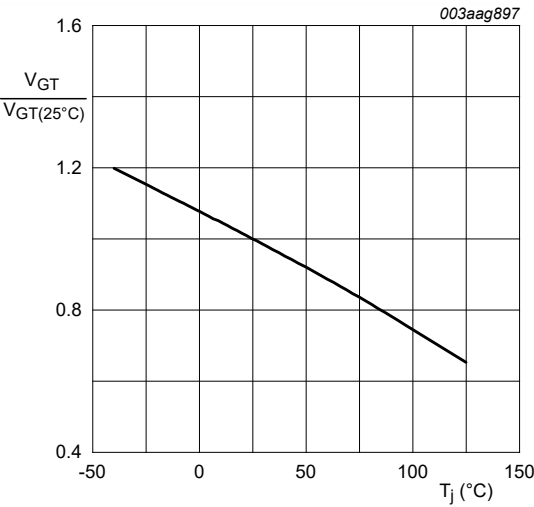


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

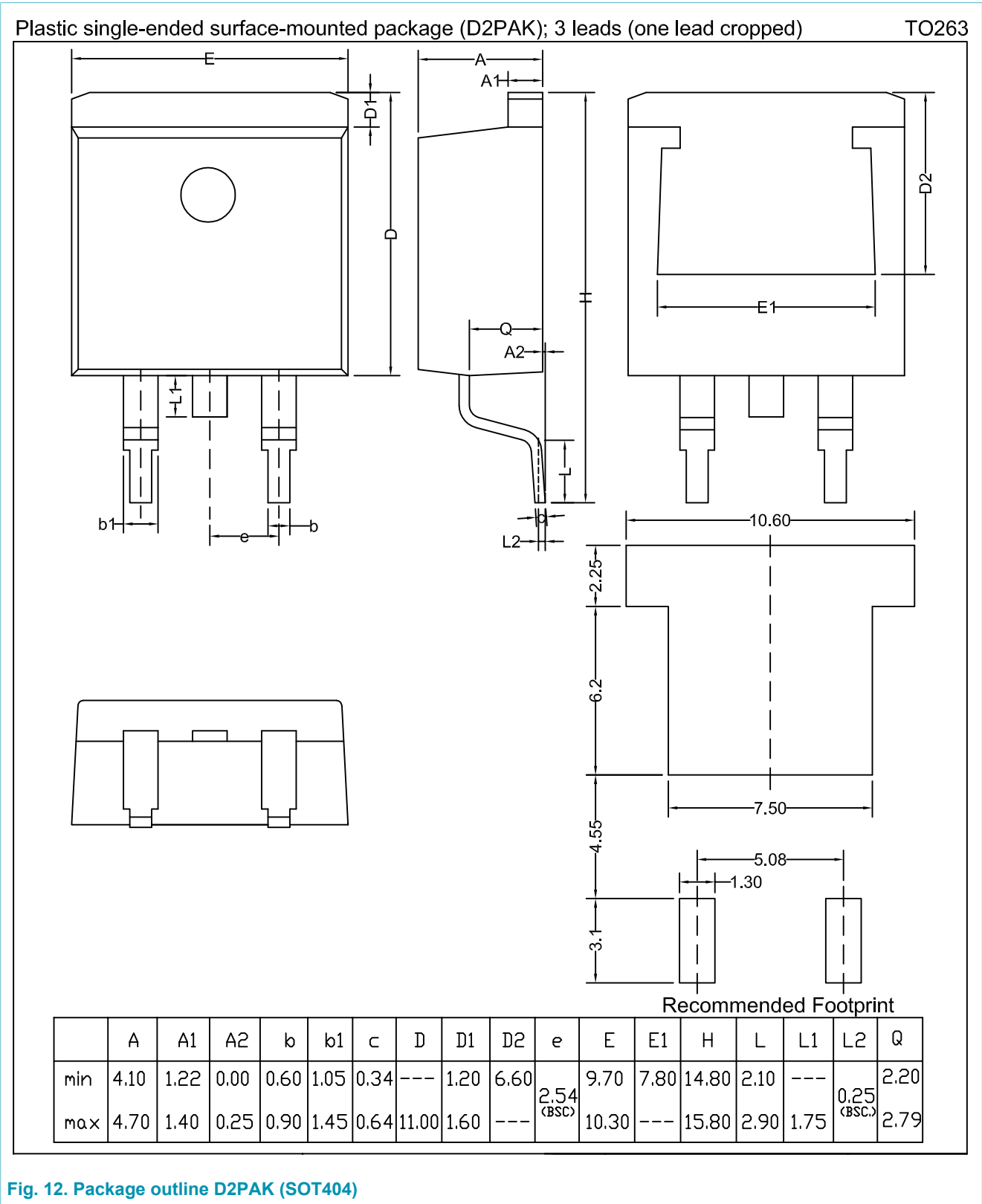


Fig. 12. Package outline D2PAK (SOT404)

11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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12. Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Limiting values..... 3

8. Thermal characteristics..... 6

9. Characteristics..... 7

10. Package outline..... 10

11. Legal information..... 11

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