



PSMN1R0-30YLC

N-channel 30 V 1.15 mΩ logic level MOSFET in LPAK using NextPower technology

15 January 2015

Product data sheet

1. General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads
- Ultra low R_{ds(on)} and low parasitic inductance

3. Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	30	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; Fig. 2	[1]	-	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	272	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	1.1	1.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	0.85	1.15	mΩ

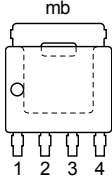
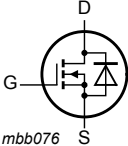
N-channel 30 V 1.15 mΩ logic level MOSFET in LPAK using
NextPower technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; Fig. 14 ; Fig. 15	-	14.6	26	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; Fig. 15 ; Fig. 14	-	50	70	nC

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-30YLC	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-30YLC	1C030L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V

**N-channel 30 V 1.15 mΩ logic level MOSFET in LPAK using
NextPower technology**

Symbol	Parameter	Conditions		Min	Max	Unit
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	272	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	100	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	[1]	-	100	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	1450	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)		960	-	V
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1450	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(initial)} = 25 °C; I _D = 100 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped; Fig. 4		-	259	mJ

[1] Continuous current is limited by package.

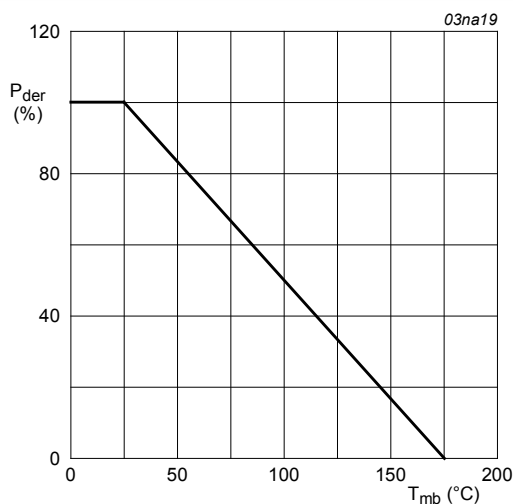


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

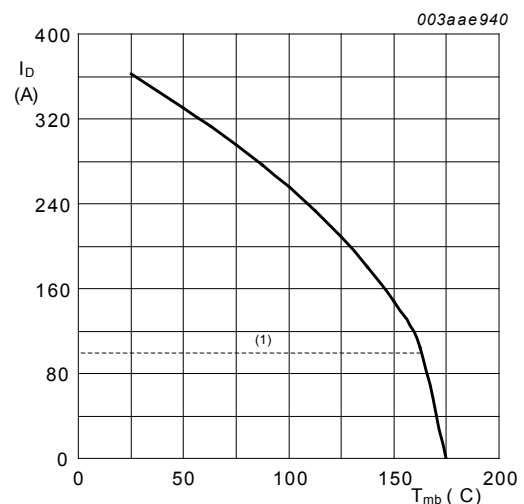


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10\text{ V}$$

(1) Capped at 100 A due to package.

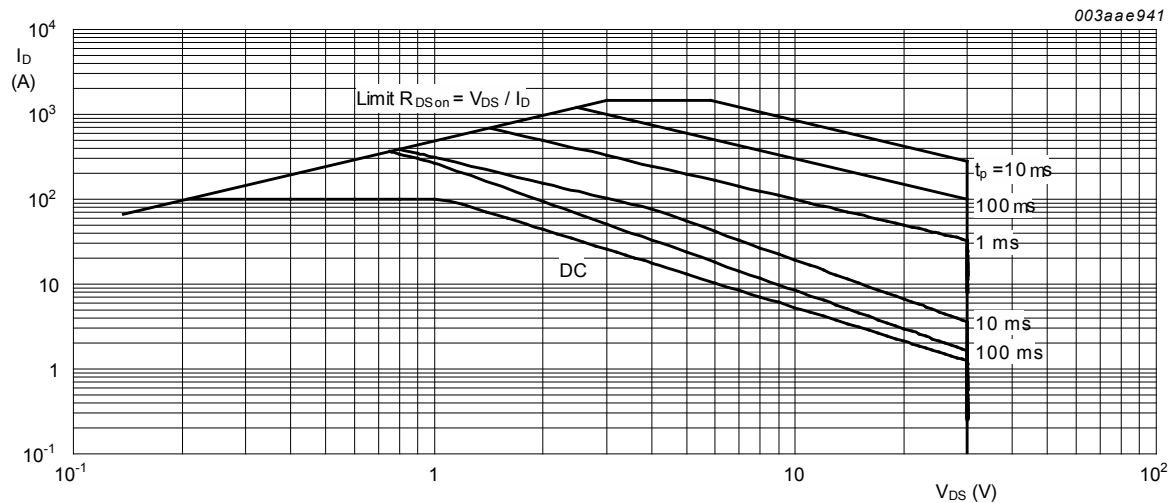


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

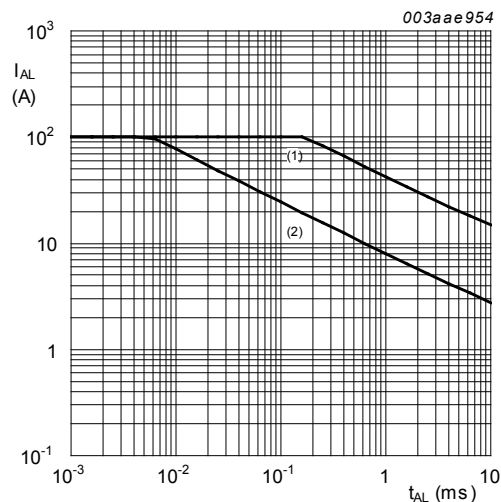


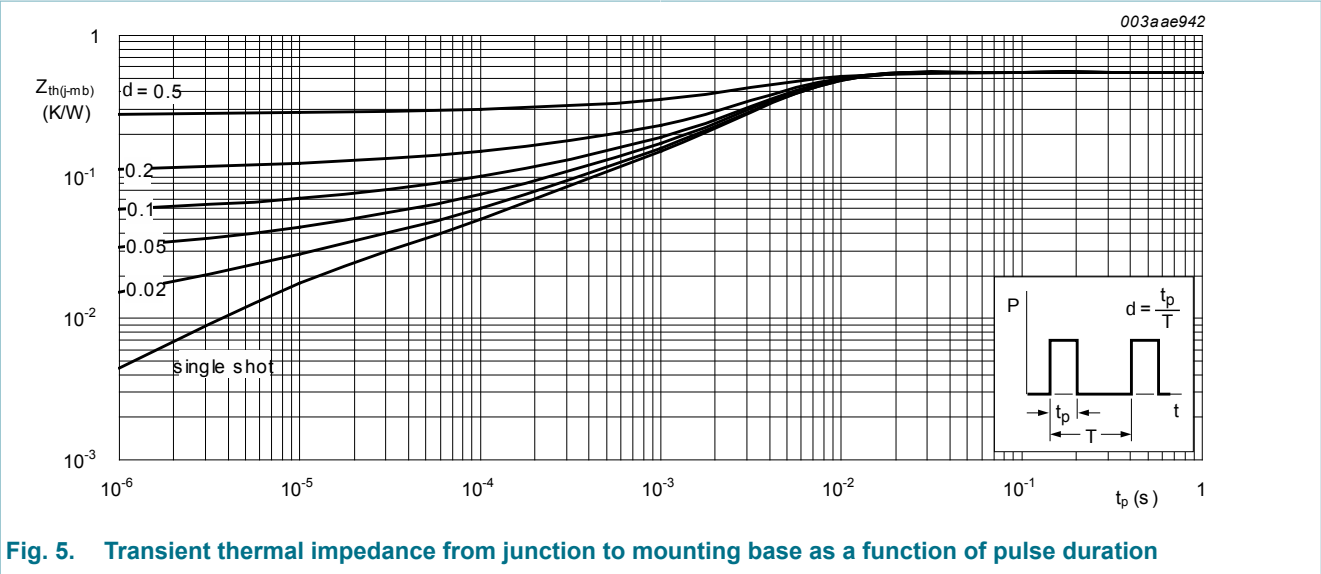
Fig. 4. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(t_{rit})} = 25^{\circ}\text{C}$; (2) $T_{j(t_{rit})} = 100^{\circ}\text{C}$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.55	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	30	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; Fig. 10	1.05	1.41	1.95	V
		I _D = 10 mA; V _{DS} = V _{GS} ; T _J = 150 °C; Fig. 11	0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; Fig. 11	-	-	2.25	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _J = 25 °C	-	-	1	μA
		V _{DS} = 30 V; V _{GS} = 0 V; T _J = 150 °C	-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _J = 25 °C	-	-	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _J = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _J = 25 °C; Fig. 12	-	1.1	1.4	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _J = 150 °C; Fig. 12; Fig. 13	-	-	2.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 12	-	0.85	1.15	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 150 °C; Fig. 12; Fig. 13	-	-	1.85	mΩ

**N-channel 30 V 1.15 mΩ logic level MOSFET in LPAK using
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_G	gate resistance	$f = 1 \text{ MHz}$		-	1.1	2.2	Ω
Dynamic characteristics							
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 10 \text{ V}$; Fig. 14 ; Fig. 15		-	103.5	145	nC
		$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; Fig. 15 ; Fig. 14		-	50	70	nC
		$I_D = 0 \text{ A}$; $V_{DS} = 0 \text{ V}$; $V_{GS} = 10 \text{ V}$; Fig. 15		-	96.5	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; Fig. 14 ; Fig. 15		-	12.9	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge			-	10.1	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge			-	2.8	-	nC
Q_{GD}	gate-drain charge			-	14.6	26	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; Fig. 14		-	2.2	-	V
C_{iss}	input capacitance	$V_{DS} = 15 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 16		3322	6645	9968	pF
C_{oss}	output capacitance			605	1210	1815	pF
C_{rss}	reverse transfer capacitance			240	481	842	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 15 \text{ V}$; $R_L = 0.6 \Omega$; $V_{GS} = 4.5 \text{ V}$; $R_{G(\text{ext})} = 4.7 \Omega$		-	44	-	ns
t_r	rise time			-	77	-	ns
$t_{d(\text{off})}$	turn-off delay time			-	108	-	ns
t_f	fall time			-	60	-	ns
Q_{oss}	output charge	$V_{GS} = 0 \text{ V}$; $V_{DS} = 15 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$		-	35.2	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 17		-	0.8	1.1	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 15 \text{ V}$		-	45	-	ns
Q_r	recovered charge			-	67	-	nC
t_a	reverse recovery rise time	$I_S = 25 \text{ A}$; $dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 15 \text{ V}$; Fig. 18		-	28.5	-	ns
t_b	reverse recovery fall time			-	16.5	-	ns

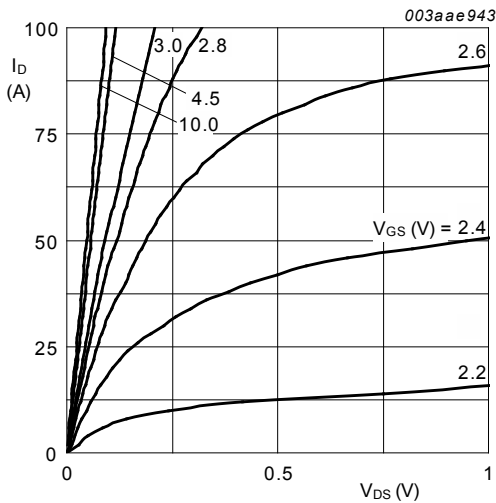


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_J = 25^{\circ}\text{C}$

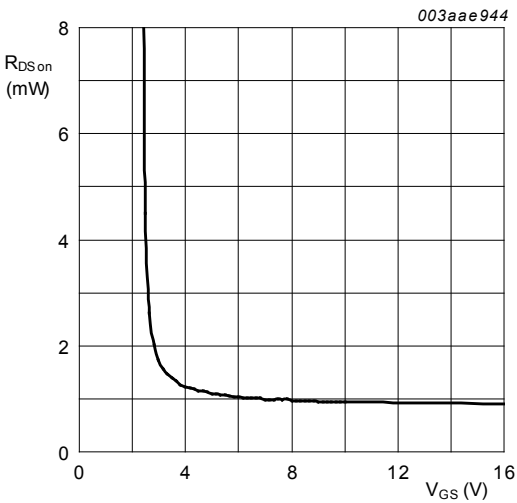


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_J = 25^{\circ}\text{C}; I_D = 25\text{A}$

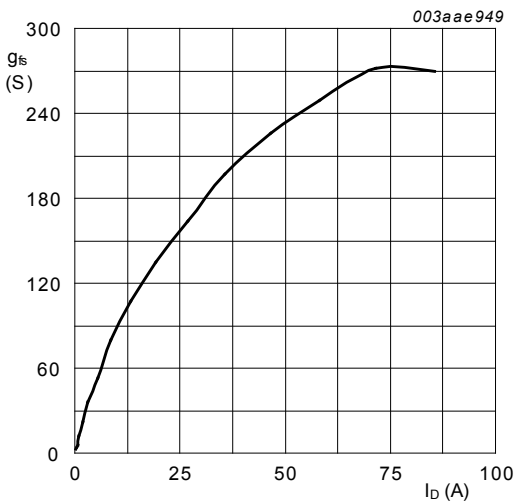


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_J = 25^{\circ}\text{C}; V_{DS} = 10\text{V}$

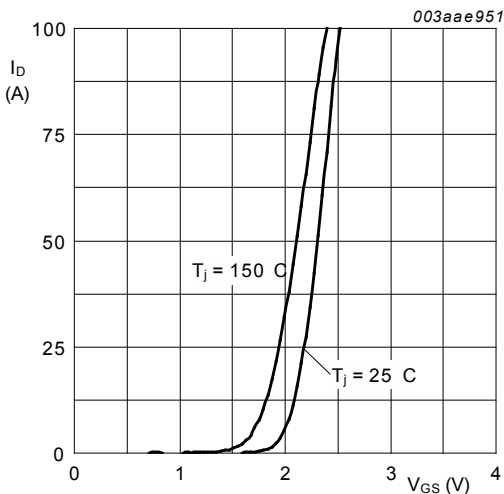


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

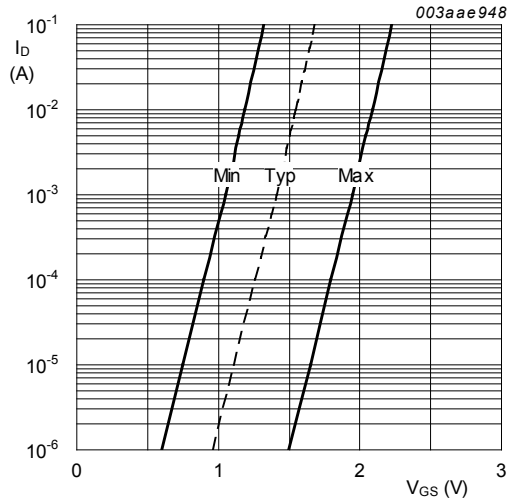


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

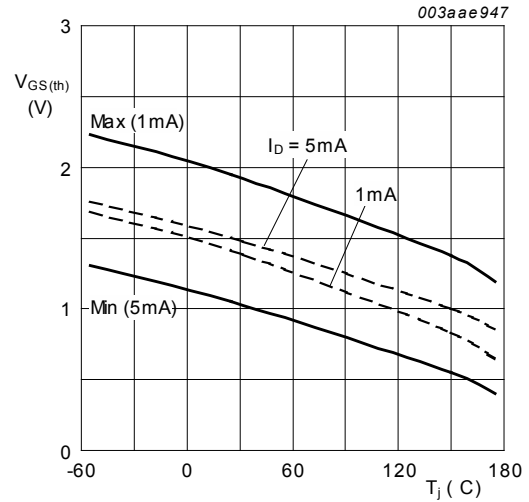


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$V_{DS} = V_{GS}$$

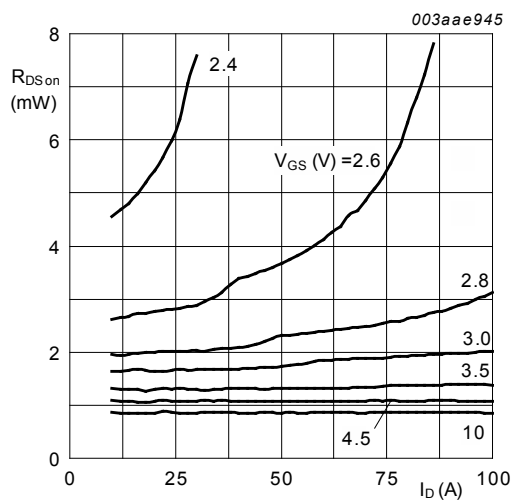


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

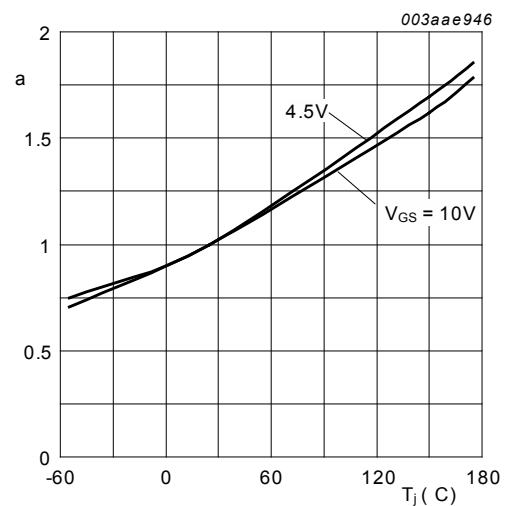


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

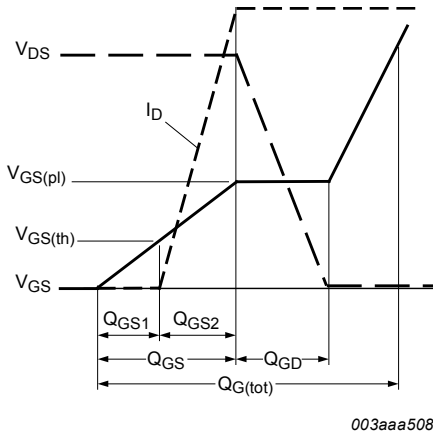


Fig. 14. Gate charge waveform definitions

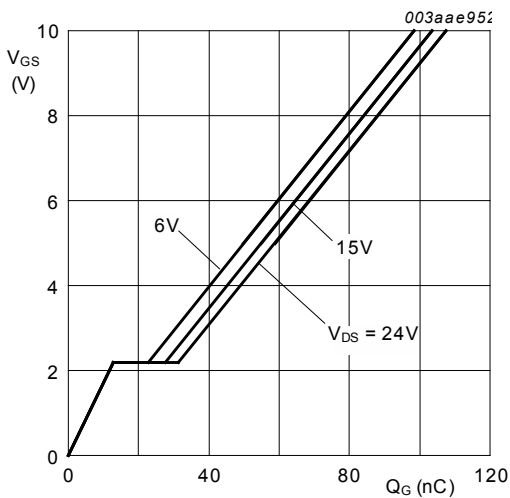


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^{\circ}C; I_D = 25A$

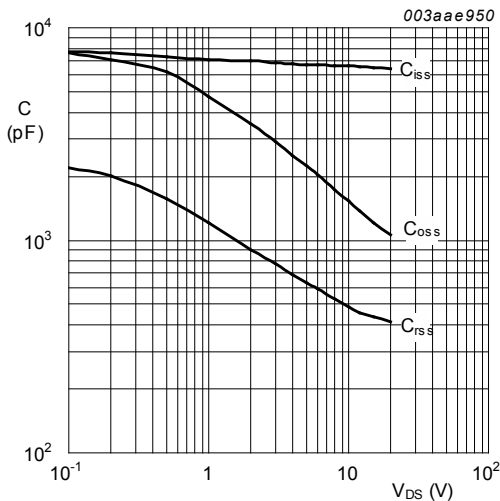


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

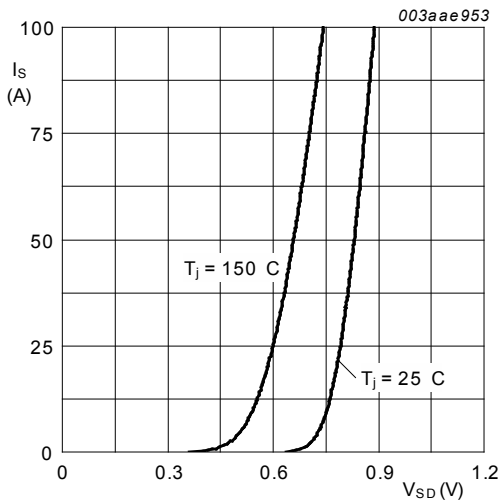


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

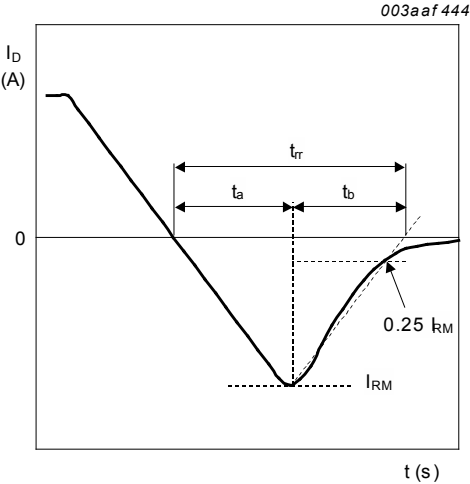


Fig. 18. Reverse recovery timing definition

11. Package outline

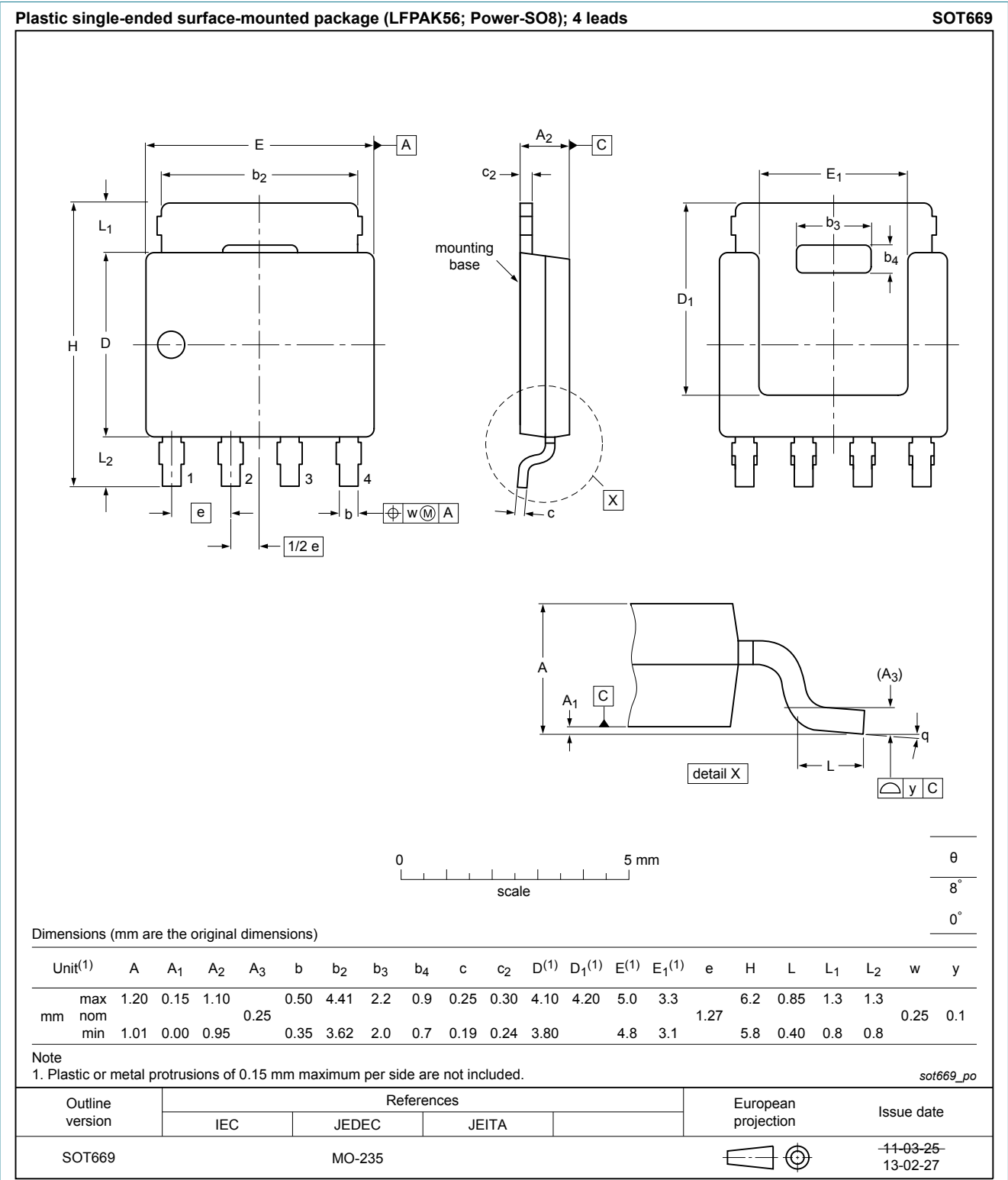


Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	4
10	Characteristics	5
11	Package outline	11
12	Legal information	12
12.1	Data sheet status	12
12.2	Definitions	12
12.3	Disclaimers	12
12.4	Trademarks	13

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