

PSMN4R0-40YS

N-channel LFPAK 40 V 4.2 mΩ standard level MOSFET Rev. 02 — 12 July 2010 Product da

Product data sheet

1. **Product profile**

1.1 General description

Standard level N-channel MOSFET in LFPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package

1.3 Applications

- DC-to-DC convertors
- Lithium-ion battery protection
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	40	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	-	-	100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	106	W
T _j	junction temperature		-55	-	175	°C
Static char	acteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_j = 100 \text{ °C}; \text{ see } \frac{\text{Figure } 12}{}$	-	-	5.6	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 ^{\circ}\text{C}; \text{ see } \frac{\text{Figure } 12}{\text{Figure } 13};$ see Figure 13	-	3.2	4.2	mΩ



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Dynamic ch	aracteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$	-	7	-	nC
Q _{G(tot)}	total gate charge	V _{DS} = 20 V; see <u>Figure 14;</u> see <u>Figure 15</u>	-	38	-	nC
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$V_{GS} = 10 \text{ V; } T_{j(init)} = 25 \text{ °C;}$ $I_D = 100 \text{ A; } V_{sup} \le 40 \text{ V;}$ unclamped; $R_{GS} = 50 \Omega$	-	-	77	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		_
2	S	source	mb	D
3	S	source		
4	G	gate	G—VE	
mb	D	drain	1 2 3 4	mbb076 S
			SOT669 (LFPAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R0-40YS	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _i ≥ 25 °C; T _i ≤ 175 °C	-	40	V
V _{DGR}	drain-gate voltage	$T_i \ge 25$ °C; $T_i \le 175$ °C; $R_{GS} = 20$ kΩ	-	40	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	$V_{GS} = 10 \text{ V; } T_{mb} = 100 \text{ °C; see } \frac{\text{Figure 1}}{\text{Model}}$	-	83	Α
		$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$	-	100	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; see Figure 3	-	472	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	106	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drain	n diode				
Is	source current	T _{mb} = 25 °C	-	100	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	472	Α
Avalanche ru	uggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 40 V; unclamped; R_{GS} = 50 Ω	-	77	mJ

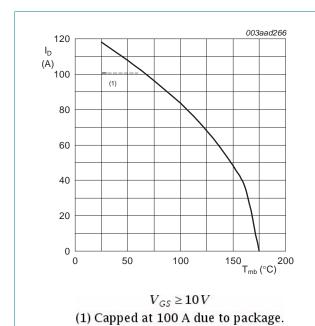
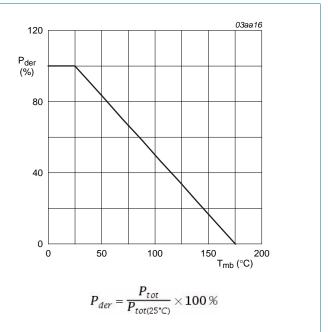
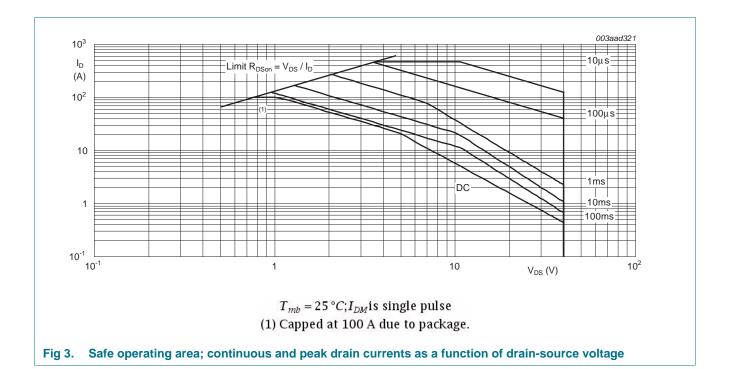


Fig 1. Continuous drain current as a function of mounting base temperature



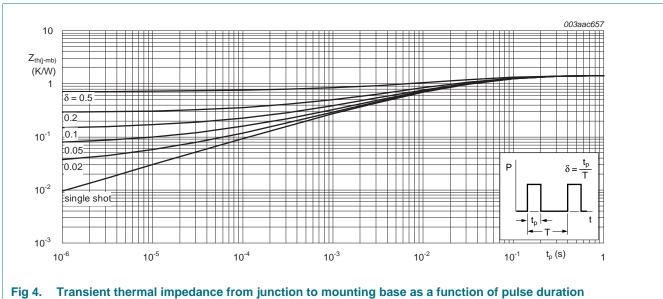
ig 2. Normalized total power dissipation as a function of mounting base temperature



Thermal characteristics

Table 5. **Thermal characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.54	1.42	K/W



6. Characteristics

Table 6. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	36	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	40	-	-	V
V _{GS(th)} gate-source th voltage	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ °C}$; see Figure 10; see Figure 11	-	-	4.6	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 175$ °C; see Figure 10; see Figure 11	1	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 25$ °C; see <u>Figure 10</u> ; see <u>Figure 11</u>	2	3	4	V
I _{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	3	μΑ
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 125 °C	-	-	40	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ °C};$ see Figure 12	-	-	5.6	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ °C};$ see Figure 12	-	-	8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C};$ see Figure 12; see Figure 13	-	3.2	4.2	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz	-	0.62	-	Ω
Dynamic ch	aracteristics					
Q _{G(tot)}	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	31	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V};$	-	38	-	nC
Q _{GS}	gate-source charge	see Figure 14; see Figure 15	-	12	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	$I_D = 25 \text{ A}$; $V_{DS} = 20 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 14	-	7	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	5	-	nC
Q_{GD}	gate-drain charge	$I_D = 25 \text{ A}$; $V_{DS} = 20 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 14; see Figure 15	-	7	-	nC
V _{GS(pI)}	gate-source plateau voltage	$I_D = 25 \text{ A}$; $V_{DS} = 20 \text{ V}$; see <u>Figure 14</u>	-	4.8	-	V
C _{iss}	input capacitance	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	2410	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	504	-	pF
C _{rss}	reverse transfer capacitance		-	266	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 20 \text{ V}; R_L = 0.8 \Omega; V_{GS} = 10 \text{ V};$	-	18	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	19	-	ns
t _{d(off)}	turn-off delay time		-	34	-	ns
t _f	fall time		-	12	-	ns

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 Table 6.
 Characteristics ...continued

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-drain	diode					
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see <u>Figure 17</u>	-	0.83	1.2	V
t _{rr}	reverse recovery time	$I_S = 50 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	42	-	ns
Q _r	recovered charge	$V_{DS} = 20 \text{ V}$	-	45	-	nC

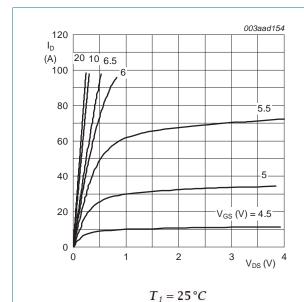


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

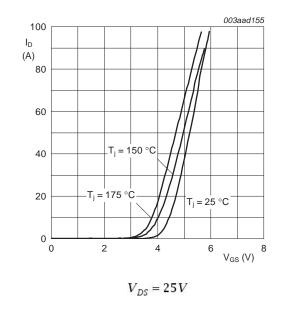


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

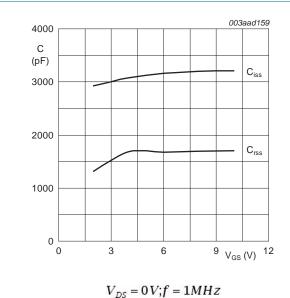
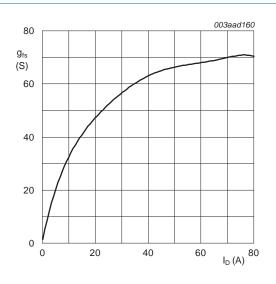


Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



 $T_j = 25 \,^{\circ}C; V_{DS} = 25 \, V$

Fig 8. Forward transconductance as a function of drain current; typical values

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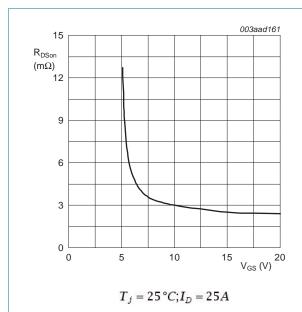
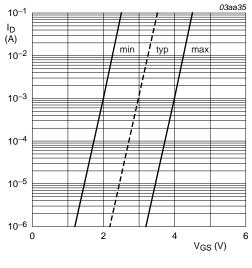


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $T_j = 25 \,^{\circ}C; V_{DS} = 5V$

Fig 10. Sub-threshold drain current as a function of gate-source voltage

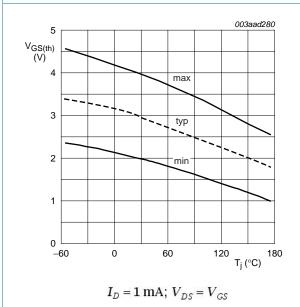


Fig 11. Gate-source threshold voltage as a function of junction temperature

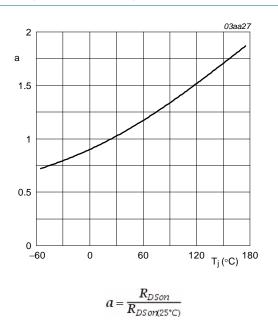
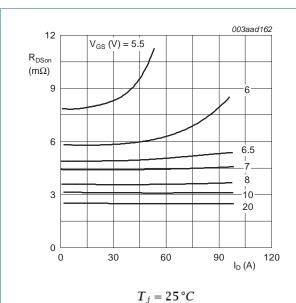


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



V_{GS}(pl)

V_{GS}(th)

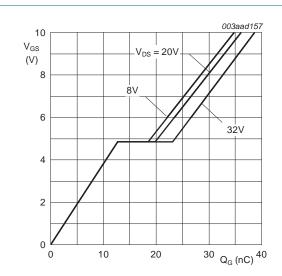
V_{GS}

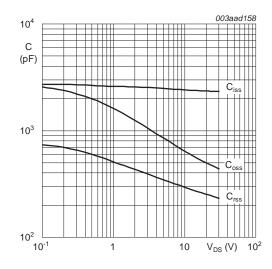
Q_{GS1}
Q_{GS2}
Q_G(tot)

003aaa508

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

Fig 14. Gate charge waveform definitions





 $T_j=25\,^{\circ}C; I_D=25A$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical

 $V_{GS} = 0V; f = 1MHz$



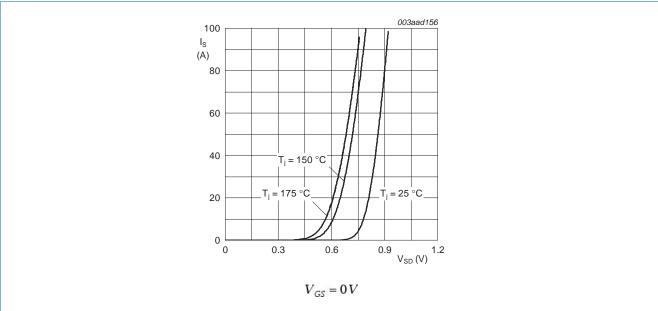


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads

SOT669

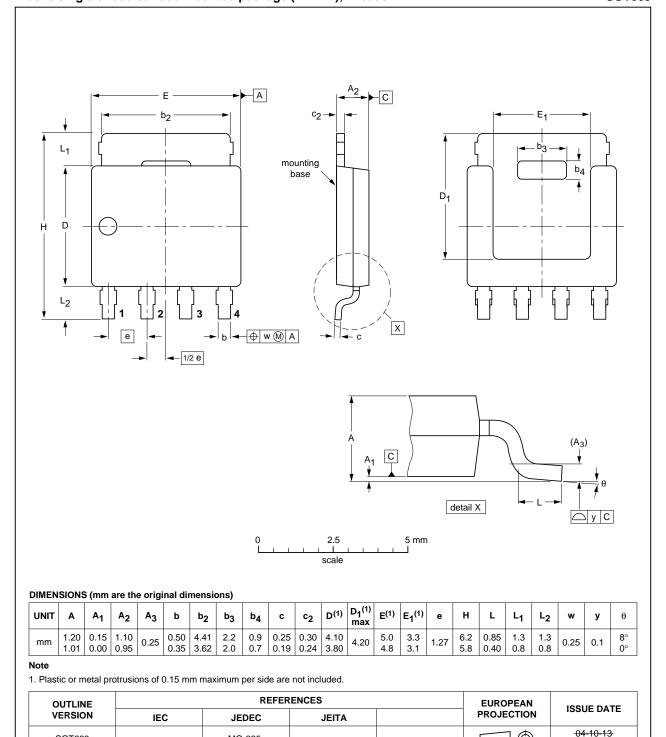


Fig 18. Package outline SOT669 (LFPAK)

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MO-235

06-03-16

SOT669

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN4R0-40YS v.2	20100712	Product data sheet	-	PSMN4R0-40YS v.1
Modifications:	 Various changes 	to content.		
PSMN4R0-40YS v.1	20090625	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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PSMN4R0-40YS

Nexperia

N-channel LFPAK 40 V 4.2 mΩ standard level MOSFET

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