



# FSL306LRN

## Green Mode Fairchild Buck Switch

### Features

- Built-in Avalanche Rugged SenseFET: 650 V
- Fixed Operating Frequency: 50 kHz
- No-Load Power Consumption: < 25 mW at 230 V<sub>AC</sub> with External Bias; <120 mW at 230 V<sub>AC</sub> without External Bias
- No Need for Auxiliary Bias Winding
- Frequency Modulation for Attenuating EMI
- Pulse-by-Pulse Current Limiting
- Ultra-Low Operating Current: 250  $\mu$ A
- Built-in Soft-Start and Startup Circuit
- Adjustable Peak Current Limit
- Built-in Transconductance (Error) Amplifier
- Various Protections: Overload Protection (OLP), Over-Voltage Protection (OVP), Feedback Open Loop Protection (FB\_OLP), AOCP (Abnormal Over-Current Protection), Thermal Shutdown (TSD)
- Fixed 650 ms Restart Time for Safe Auto-Restart Mode of All Protections

### Applications

- SMPS for Home Appliances and Industrial Applications
- SMPS for Auxiliary Power

### Description

The FSL306LRN integrate Pulse Width Modulator (PWM) and SenseFET is specifically designed for high-performance offline buck, buck-boost, and non-isolation flyback Switched Mode Power Supplies (SMPS) with minimal external components. This device integrates a high-voltage power regulator that enables operation without auxiliary bias winding. An internal transconductance amplifier reduces external components for the feedback compensation circuit.

The integrated PWM controller includes: 10 V regulator for no external bias circuit, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), an optimized gate turn-on / turn-off driver, EMI attenuator, Thermal Shutdown (TSD), temperature-compensated precision current sources for loop compensation, and fault-protection circuitry. Protections include: Overload Protection (OLP), Over-Voltage Protection (OVP), Feedback Open Loop Protection (FB\_OLP), and Abnormal Over-Current Protection (AOCP). FSL306LRN offers good soft-start performance during startup.

The internal high-voltage startup switch and the Burst-Mode operation with very low operating current reduce the power loss in Standby Mode. As the result, it is possible to reach power loss of 120 mW without external bias and 25 mW with external bias when input voltage is 230 V<sub>AC</sub>.

### Ordering Information

Part Number	Operating Junction Temperature	PKG	Packing Method	Typical Output Power <sup>(1)</sup>			
				Current Limit	R <sub>DS(ON),MAX</sub>	85 V <sub>AC</sub> ~ 265 V <sub>AC</sub> & Open Frame <sup>(2)</sup>	
						Buck Application <sup>(3)</sup>	Flyback Application
FSL306LRN	-40°C ~ 125°C	7-DIP	Rail	0.45 A	18 $\Omega$	3 W	7 W

#### Notes:

1. The junction temperature can limit the maximum output power.
2. Maximum practical continuous power in an open-frame design at 50°C ambient.
3. Based on 15 V output voltage condition. Output voltage can limit the maximum output power.

## Application Diagrams

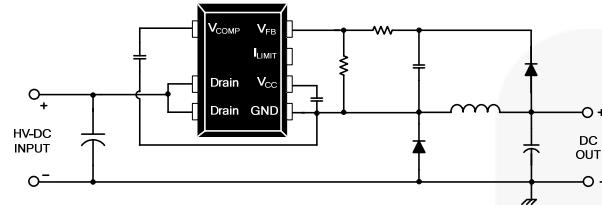


Figure 1. Buck Converter Application

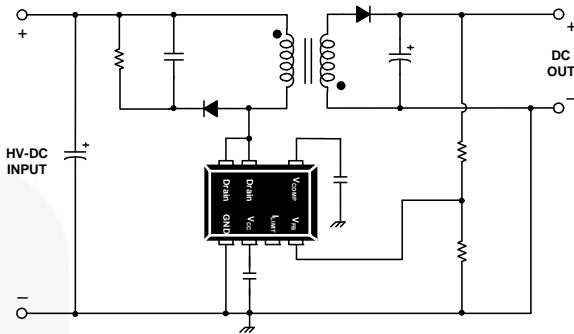


Figure 2. Non-Isolation Flyback Converter Application

## Block Diagram

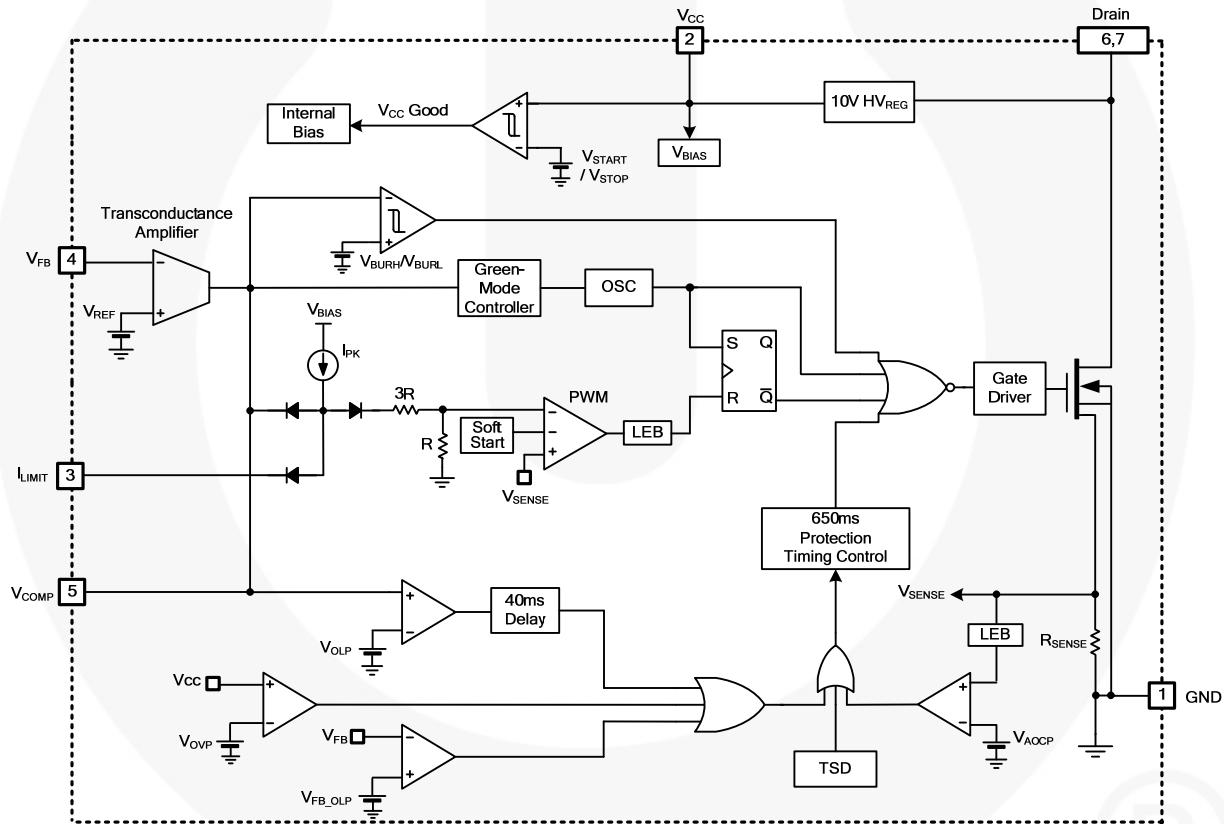


Figure 3. Internal Block Diagram

## Pin Configuration

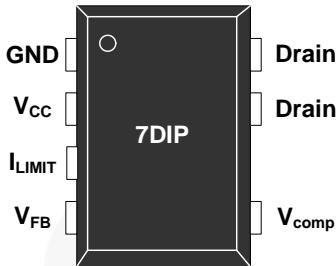


Figure 4. Pin Configuration

## Pin Definitions

Pin #	Name	Description
1	GND	<b>Ground.</b> SenseFET source terminal on the primary side and internal control ground.
2	V <sub>CC</sub>	<b>Positive Supply Voltage Input.</b> This pin is the positive supply input, which provides the internal operating current for startup and steady-state operation. This pin voltage is regulated to 10 V, without the external bias circuit, via internal switch (see <i>Figure 3</i> ). When the external bias voltage is higher than 10 V, it disables the internal high-voltage regulator and reduces power consumption.
3	I <sub>LIMIT</sub>	<b>Peak Current Limit.</b> Adjusts the peak current limit of the SenseFET. The internal 50 $\mu$ A current source is diverted to the parallel combination of an internal 46 k $\Omega$ (3R + R) resistors and any external resistor to GND on this pin to determine the peak current limit.
4	V <sub>FB</sub>	<b>Feedback Voltage.</b> Inverting input of the transconductance amplifier. This pin controls converter output voltage by outputting a current proportional to the difference between the reference voltage and the output voltage divided by external resistors.
5	V <sub>COMP</sub>	<b>Comp Voltage.</b> Output of the transconductance amplifier. The compensation networks are placed between the V <sub>COMP</sub> and GND pins to achieve stability and good dynamic performance.
6,7	Drain	<b>Drain.</b> High-voltage power SenseFET drain connection. In addition, during startup and steady-state operation; the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V <sub>CC</sub> pin. Once V <sub>CC</sub> reaches 8 V, all internal blocks are activated. The internal high-voltage current source is enabled until V <sub>CC</sub> reaches 10 V. After that, the internal high-voltage regulator turns on and off regularly to maintain V <sub>CC</sub> at 10 V.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
$V_{DS}$	Drain Pin Voltage	-0.3	650.0	V
$V_{CC}$	Supply Voltage	-0.3	26.0	V
$V_{COMP}$	$V_{COMP}$ Pin Voltage	-0.3	Internally Clamped Voltage <sup>(4)</sup>	V
$V_{FB}$	Feedback Voltage	-0.3	12.0	V
$I_{LIMIT}$	Current Limit Pin Voltage	-0.3	12.0	V
$I_{DM}$	Drain Current Pulsed <sup>(5)</sup>		2.8	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>(6)</sup>		10.5	mJ
$P_D$	Total Power Dissipation		1.25	W
$T_J$	Operating Junction Temperature <sup>(7)</sup>	-40	125	$^\circ\text{C}$
	Maximum Junction Temperature		150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-55	150	$^\circ\text{C}$

**Notes:**

4.  $V_{COMP}$  is clamped by internal clamping diode (11 V,  $I_{CLAMP\_MAX} < 100 \mu\text{A}$ )
5. Repetitive rating: pulse width is limited by maximum junction temperature.
6. L=10 mH, starting  $T_J=25^\circ\text{C}$ .
7. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

## Thermal Impedance

$T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Value	Unit
$\theta_{JA}$	Junction-to-Ambient Thermal Impedance <sup>(8)</sup>	100	$^\circ\text{C/W}$

**Notes:**

8. JEDEC recommended environment, JESD51-2, and test board, JESD51-3, with minimum land pattern.

## ESD Capability

Symbol	Parameter	Value	Unit
ESD	Human Body Model, JESD22-A114 <sup>(9)</sup>	4	kV
	Charged Device Model, JESD22-C101 <sup>(9)</sup>	2	

**Notes:**

9. Meets JEDEC standards JESD 22-A114 and JESD 22-C101.

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>SenseFET Section</b>						
$BV_{DSS}$	Drain Source Breakdown Voltage	$V_{CC} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	650			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 520 \text{ V}$ , $T_A = 125^\circ\text{C}$			250	$\mu\text{A}$
$R_{DS(\text{ON})}$	Drain-Source On-State Resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 0.3 \text{ A}$		12	18	$\Omega$
$C_{ISS}$	Input Capacitances	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$		97		$\text{pF}$
$C_{OSS}$	Output Capacitance	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$		13.6		$\text{pF}$
$C_{RSS}$	Reverse Transfer Capacitance	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$		2.4		$\text{pF}$
$t_r$	Rise Time	$V_{DD} = 325 \text{ V}$ , $I_D = 0.7 \text{ A}$		7.6		ns
$t_f$	Fall Time	$V_{DD} = 325 \text{ V}$ , $I_D = 0.7 \text{ A}$		26.1		ns
<b>Control Section</b>						
$f_{\text{OSC}}$	Switching Frequency	$V_{COMP} = 2.5 \text{ V}$	45	50	55	kHz
$f_M$	Frequency Modulation <sup>(10)</sup>	$V_{COMP} = 2.5 \text{ V}$ , Randomly		$\pm 3$		kHz
$t_{\text{on,max}}$	Maximum Turn-On Time	$V_{COMP} = 2.5 \text{ V}$	11.2	13.3	15.4	$\mu\text{s}$
$V_{\text{START}}$	UVLO Threshold Voltage	$V_{COMP} = 0 \text{ V}$ , $V_{CC}$ Sweep	7.2	8.0	8.8	V
$V_{\text{STOP}}$		After Turn On	6.3	7.0	7.7	V
$I_{PK}$	Current Limit Source Current	$V_{COMP} = 2.5 \text{ V}$	35	50	65	$\mu\text{A}$
$t_{\text{SS}}$	Soft-Start Time	$V_{COMP} = 2.5 \text{ V}$	7	10	13	ms
<b>Burst Mode Section</b>						
$V_{\text{BURH}}$	Burst-mode HIGH Threshold Voltage	$V_{CC} = 15 \text{ V}$ , $V_{COMP}$ Increase	0.58	0.65	0.72	V
$V_{\text{BURL}}$	Burst-mode LOW Threshold Voltage	$V_{CC} = 15 \text{ V}$ , $V_{COMP}$ Decrease	0.52	0.59	0.66	V
$HYS_{\text{BUR}}$	Burst-mode Hysteresis			60		mV
<b>Protection Section</b>						
$I_{\text{LIM}}$	Peak Current Limit	$V_{COMP} = 2.5 \text{ V}$ , $di/dt = 300 \text{ mA}/\mu\text{s}$	0.40	0.45	0.50	A
$t_{\text{CLD}}$	Current Limit Delay <sup>(10)</sup>				200	ns
$V_{\text{OLP}}$	Overload Protection	$V_{COMP}$ Increase	2.7	3.0	3.3	V
$V_{\text{AOCP}}$	Abnormal Over-Current Protection <sup>(10)</sup>	$V_{COMP} = 2.5 \text{ V}$	0.8	1.0	1.2	V
$t_{\text{LEB}}$	Leading-Edge Blanking Time <sup>(10)</sup>			200		ns
$V_{\text{FB\_OLP}}$	FB Open Loop Protection	$V_{FB}$ Decrease	0.4	0.5	0.6	V
$V_{\text{OVP}}$	Over-Voltage Protection	$V_{CC}$ Increase	23.0	24.5	26.0	V
$T_{\text{SD}}$	Thermal Shutdown Temperature <sup>(10)</sup>		125	135	150	$^\circ\text{C}$
$HYS_{\text{TSD}}$	TSD Hysteresis Temperature <sup>(10)</sup>			60		$^\circ\text{C}$
$t_{\text{DELAY}}$	Over Load Protection Delay <sup>(10)</sup>	$V_{COMP} > 3 \text{ V}$		40		ms
$t_{\text{RESTART}}$	Restart Time After Protection <sup>(10)</sup>			650		ms
<b>Transconductance Amplifier Section</b>						
$G_m$	Transconductance of Error Amplifier		190	240	290	$\mu\text{mho}$
$V_{\text{REF}}$	Voltage Feedback Reference		2.45	2.50	2.55	V
$I_{\text{EA,SR}}$	Output Sourcing Current	$V_{FB} = V_{\text{REF}} - 0.05 \text{ V}$		-12		$\mu\text{A}$
$I_{\text{EA,SK}}$	Output Sink Current	$V_{FB} = V_{\text{REF}} + 0.05 \text{ V}$		12		$\mu\text{A}$

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## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>High-Voltage Regulator Section</b>						
$V_{\text{HVREG}}$	HV Regulator Voltage	$V_{\text{COMP}} = 0 \text{ V}$ , $V_{\text{DRAIN}} = 40 \text{ V}$	9	10	11	V
<b>Total Device Section</b>						
$I_{\text{OP1}}$	Operating Supply Current (Control Part Only, without Switching)	$0 \text{ V} < V_{\text{COMP}} < V_{\text{BURL}}$		0.25	0.35	mA
$I_{\text{OP2}}$	Operating Supply Current (While Switching)	$V_{\text{BURL}} < V_{\text{COMP}} < V_{\text{OLP}}$		0.8	1.3	mA
$I_{\text{CH}}$	Startup Charging Current	$V_{\text{CC}} = 0 \text{ V}$ , $V_{\text{DRAIN}} > 40 \text{ V}$		6		mA
$I_{\text{START}}$	Startup Current	$V_{\text{CC}} = \text{Before } V_{\text{START}}$ , $V_{\text{COMP}} = 0 \text{ V}$		120	155	$\mu\text{A}$
$V_{\text{DRAIN}}$	Minimum Drain Supply Voltage	$V_{\text{CC}} = V_{\text{COMP}} = 0 \text{ V}$ , $V_{\text{DRAIN}}$ Increase		35		V

**Notes:**

10. Though guaranteed by design, they are not 100% tested in production.

## Typical Performance Characteristics

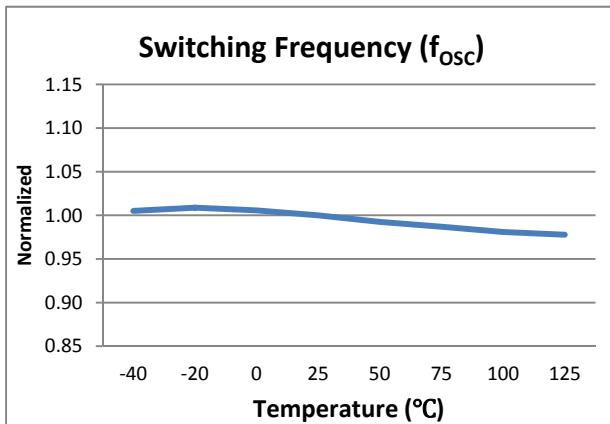


Figure 5. Operating Frequency vs. Temperature

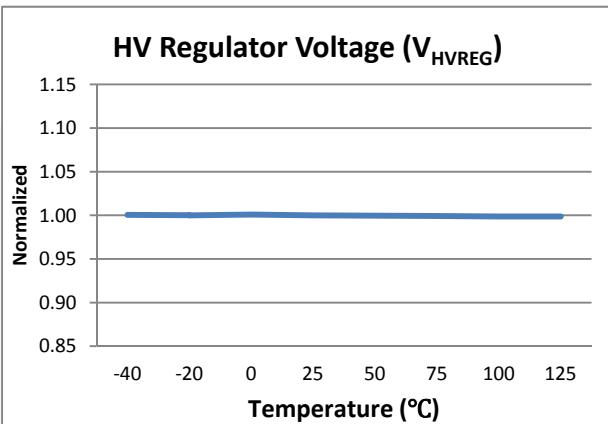


Figure 6. HV Regulator Voltage vs. Temperature

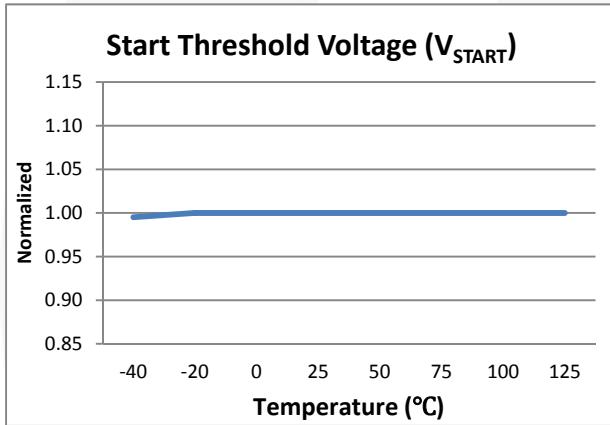


Figure 7. Start Threshold Voltage vs. Temperature

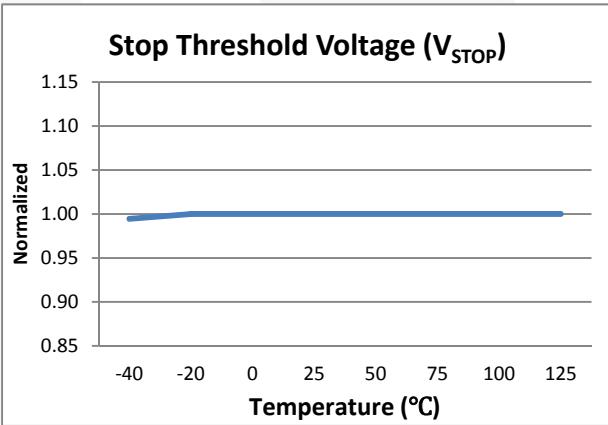


Figure 8. Stop Threshold Voltage vs. Temperature

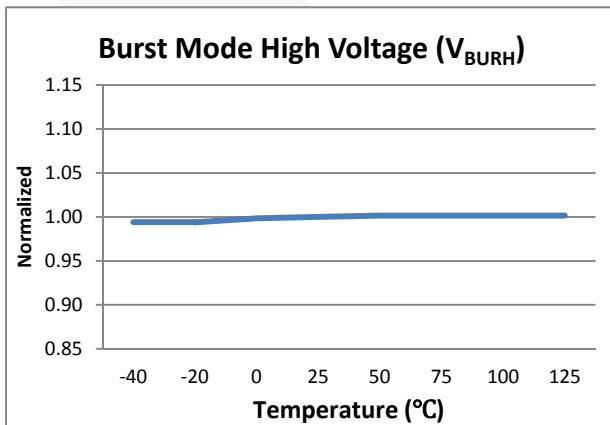


Figure 9. Burst Mode High Voltage vs. Temperature

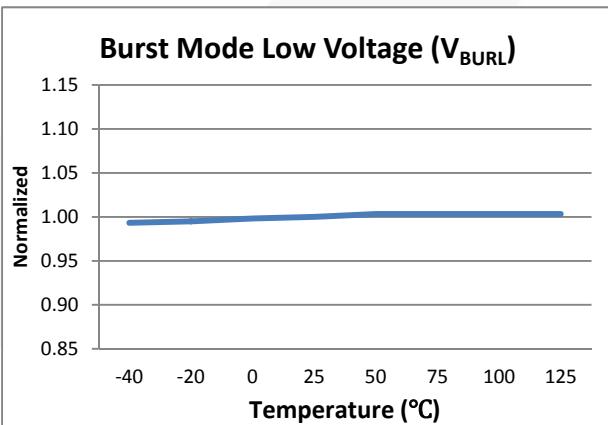


Figure 10. Burst Mode Low Voltage vs. Temperature

## Typical Performance Characteristics (Continued)

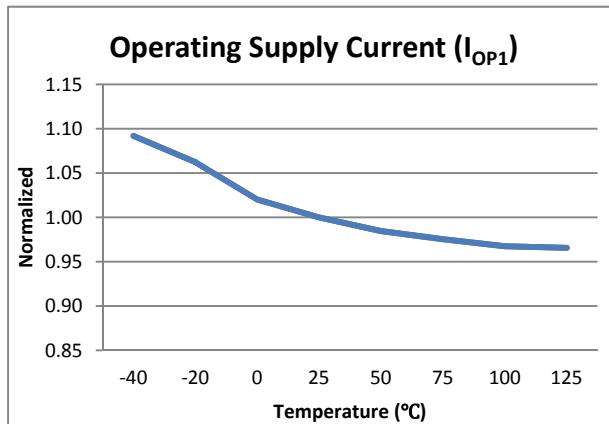


Figure 11. Operating Supply Current 1 vs. Temperature

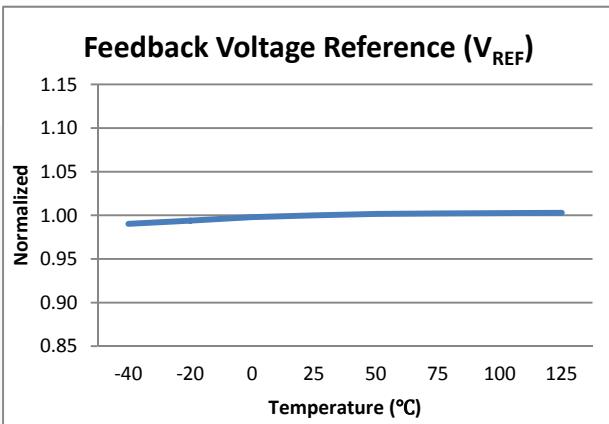


Figure 12. Feedback Voltage Reference vs. Temperature

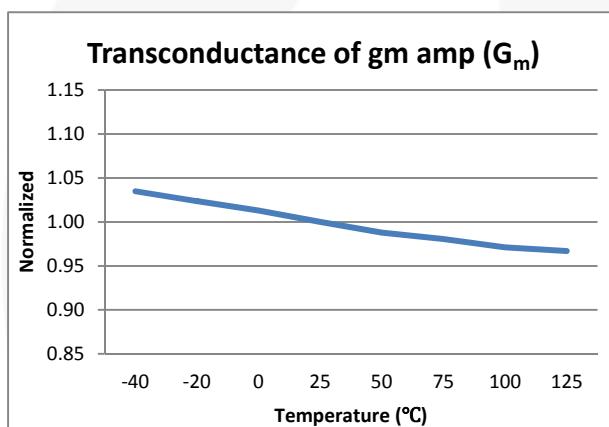


Figure 13. Transconductance of gm Amplifier vs. Temperature

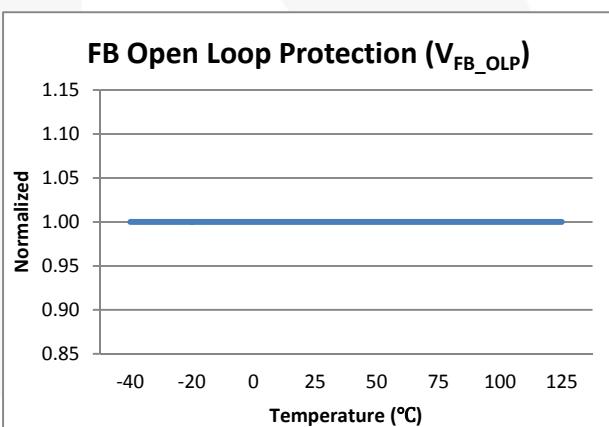


Figure 14. FB Open Loop Protection Voltage vs. Temperature

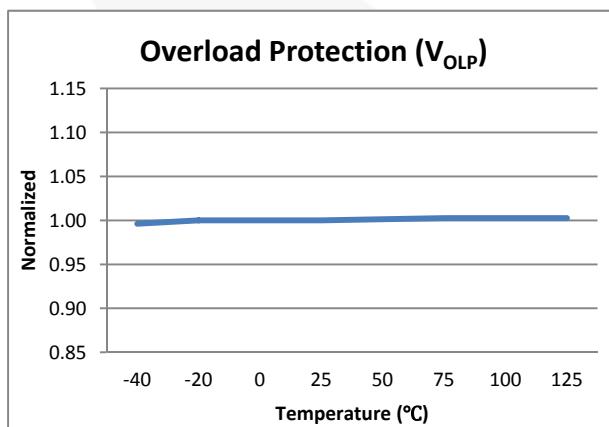


Figure 15. Overload Protection vs. Temperature

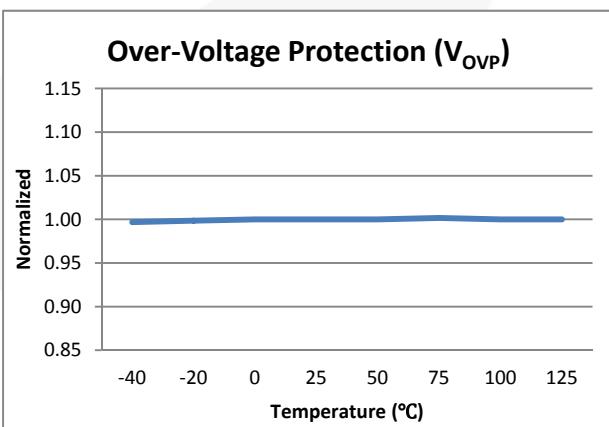


Figure 16. Over-Voltage Protection vs. Temperature

## Functional Description

### 1. Startup and High-Voltage Regulator

During startup, an internal high-voltage current source ( $I_{CH}$ ) of the high-voltage regulator supplies the internal bias current ( $I_{START}$ ) and charges the external capacitor ( $C_A$ ) connected to the  $V_{CC}$  pin, as illustrated in Figure 17. This internal high-voltage current source is enabled until  $V_{CC}$  reaches 10 V. During steady-state operation, this internal high-voltage regulator ( $HV_{REG}$ ) maintains the  $V_{CC}$  with 10 V and provides operating current ( $I_{OP}$ ) for all internal circuits. Therefore, FSL306LRN needs no external bias circuit. The high-voltage regulator is disabled when the external bias is higher than 10 V.

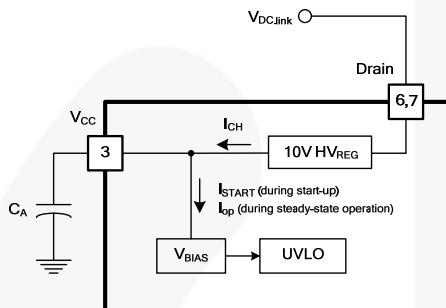


Figure 17. Startup and  $HV_{REG}$  Block

### 2. Oscillator Block

The oscillator frequency is set internally and the FSL306LRN has a random frequency fluctuation function. Fluctuation of the switching frequency can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the range of the frequency variation. The range of frequency variation is fixed internally; however, its selection is randomly chosen by the combination of an external feedback voltage and an internal free-running oscillator. This randomly chosen switching frequency effectively spreads the EMI noise near switching frequency and allows the use of a cost-effective inductor instead of an AC input line filter to satisfy world-wide EMI requirements.

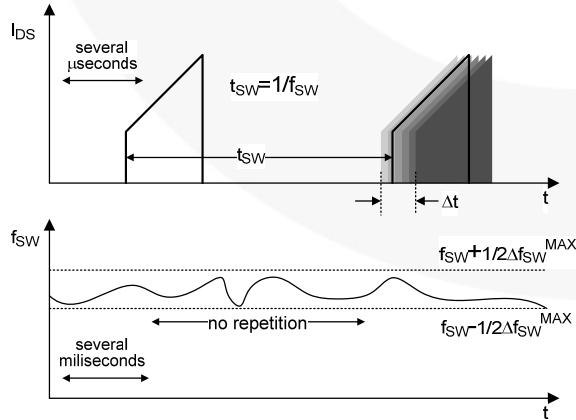


Figure 18. Frequency Fluctuation Waveform

### 3. Feedback Control

FSL306LRN employs current-mode control with a transconductance amplifier for feedback control, as shown in Figure 19. Two resistors are typically used on the  $V_{FB}$  pin to sense output voltage. An external compensation circuit is recommended on the  $V_{COMP}$  pin to control output voltage. A built-in transconductance amplifier accurately controls output voltage without external components, such as Zener diode and transistor.

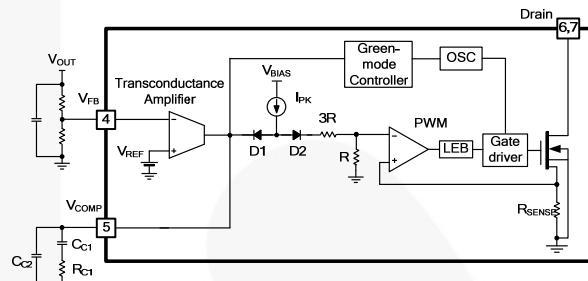


Figure 19. Pulse Width Modulation (PWM) Circuit

#### 3.1 Transconductance Amplifier (gm Amplifier)

The output of the transconductance amplifier sources and sinks the current, respectively, to and from the compensation circuit connected on the  $V_{COMP}$  pin (see Figure 20). This compensated  $V_{COMP}$  pin voltage controls the switching duty cycle by comparing with the voltage across the  $R_{SENSE}$ . When the feedback pin voltage exceeds the internal reference voltage ( $V_{REF}$ ) of 2.5 V; the transconductance amplifier sinks the current from the compensation circuit,  $V_{COMP}$  is pulled down, and the duty cycle is reduced. This typically occurs when input voltage is increased or output load is decreased. A two-pole and one-zero compensation network is recommended for optimal output voltage control and AC dynamics. Typically 220 nF, 220 kΩ, and 330 pF are used for  $C_{C1}$ ,  $R_{C1}$ , and  $C_{C2}$ , respectively.

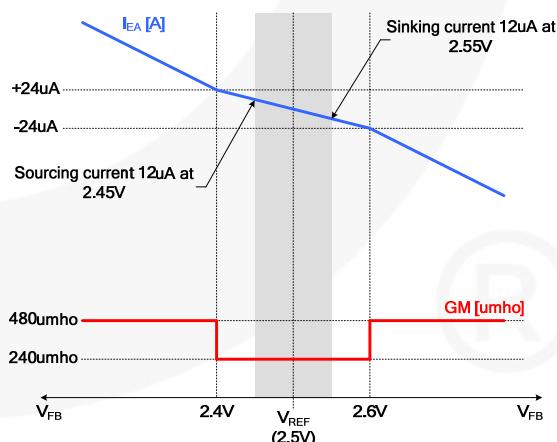


Figure 20. Characteristics of gm Amplifier

#### 3.2 Pulse-by-pulse Current Limit

Because current-mode control is employed, the peak current flowing through the SenseFET is limited by the inverting input of PWM comparator, as shown in Figure 19. Assuming that 50  $\mu$ A current source flows only through the internal resistors ( $3R + R = 46$  kΩ), the

cathode voltage of diode D2 is about 2.4 V. Since D1 is blocked when  $V_{COMP}$  exceeds 2.4 V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current of the SenseFET is limited.

### 3.3 Leading Edge Blanking (LEB)

At the instant the internal SenseFET is turned on; primary-side capacitance and secondary-side rectifier diode reverse recovery of flyback application, the freewheeling diode reverse recovery, and other parasitic capacitance of buck application typically cause a high-current spike through the SenseFET. Excessive voltage across the sensing resistor ( $R_{SENSE}$ ) leads to incorrect feedback operation in the current-mode control. To counter this effect, the FSL306LRN has a Leading-Edge Blanking (LEB) circuit (see Figure 19). This circuit inhibits the PWM comparator for a short time ( $t_{LEB}$ ) after the SenseFET is turned on.

## 4. Protection Circuits

The protective functions include Overload Protection (OLP), Over-Voltage Protection (OVP), Under-Voltage Lockout (UVLO), Feedback Open Loop Protection (FB\_OLP), Abnormal Over-Current Protection (AOCP), and Thermal Shutdown (TSD). All of the protections operate in Auto-Restart Mode. Since these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing cost and PCB space. If a fault condition occurs, switching is terminated and the SenseFET remains off. At the same time, internal protection timing control is activated to decrease power consumption and stress on passive and active components during Auto-Restart. When internal protection timing control is activated,  $V_{CC}$  is regulated with 10 V through the internal high-voltage regulator until switching is terminated. This internal protection timing control continues until restart time (650 ms) is counted. After counting to 650 ms, the internal high-voltage regulator is disabled and  $V_{CC}$  is decreased. When  $V_{CC}$  reaches the UVLO stop voltage  $V_{STOP}$  (7 V), the protection is reset and the internal high-voltage current source charges the  $V_{CC}$  capacitor via the drain pin again. When  $V_{CC}$  reaches the UVLO start voltage,  $V_{START}$  (8 V), the FSL306LRN resumes normal operation. In this manner, Auto-Restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

### 4.1 Overload Protection (OLP)

Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, even when the SMPS operates normally, the OLP circuit can be enabled during the load transition or startup. To avoid this undesired operation, an internal fixed delay (40 ms) circuit determines whether it is a transient situation or a true overload situation (see Figure 21). The current-mode feedback path limits the maximum power current and, when the output consumes more than this maximum power, the output voltage ( $V_O$ ) decreases below its rated voltage. This reduces feedback pin voltage, which increases the output current of the internal transconductance amplifier. Eventually  $V_{COMP}$  is increased. When  $V_{COMP}$  reaches 3 V, the internal fixed OLP delay (40 ms) is

activated. After this delay, the switching operation is terminated, as shown in Figure 22.

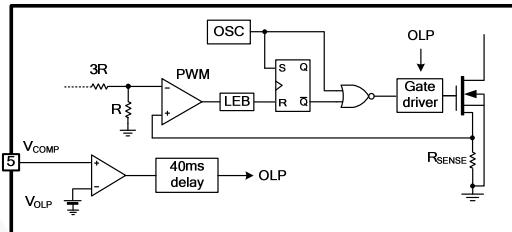


Figure 21. Overload Protection Internal Circuit

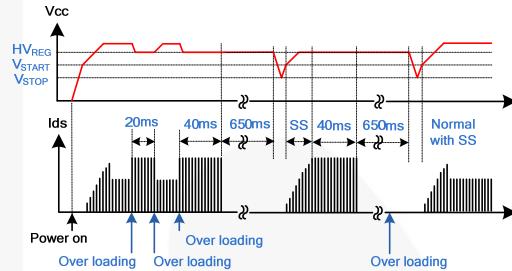


Figure 22. Overload Protection (OLP) Waveform

### 4.2 Abnormal Over-Current Protection (AOCP)

When output is shorted at high input voltage, much higher drain current peak than pulse-by-pulse current limit can flow through the SenseFET because turn on time is the same as the minimum turn-on time of FSL306LRN. Even OLP is occasionally not enough to protect the FSL306LRN in that abnormal case, since severe current stress is imposed on the SenseFET until OLP is triggered. FSL306LRN includes the internal Abnormal Over-Current Protection (AOCP) circuit shown in Figure 23. The voltage across the  $R_{SENSE}$  is compared with a preset AOCP level ( $V_{AOCP}$ ) after  $t_{LEB}$  and, if the voltage across the  $R_{SENSE}$  is greater than the AOCP level, the set signal is triggered after four switching times by an internal 2-bit counter, shutting down the SMPS, as shown in Figure 24. This LEB time can inhibit mis-triggering due to the leading-edge spike.

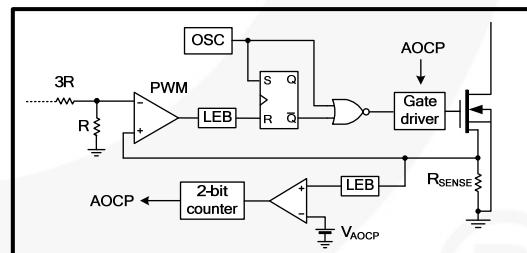


Figure 23. AOCP Circuit

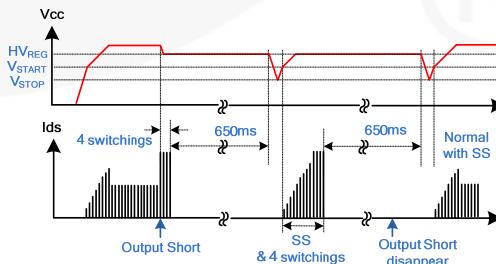


Figure 24. AOCP Waveform

### 4.3 Thermal Shutdown (TSD)

The SenseFET and control IC integrated on the same package makes it easier to detect the temperature of the SenseFET. When the junction temperature exceeds 135°C, thermal shutdown is activated. The FSL306LRN is restarted after the temperature decreases to 60°C.

### 4.4 Over-Voltage Protection (OVP)

If any feedback loop components fail due to a soldering defect,  $V_{COMP}$  climbs up in manner similar to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the OLP is triggered. In this case, excessive energy is provided to the output and the output voltage may exceed the rated voltage before the OLP is activated. To prevent this situation, an Over-Voltage Protection (OVP) circuit is employed. In general, output voltage can be monitored through  $V_{CC}$  and, when  $V_{CC}$  exceeds 24.5 V, OVP is triggered, resulting in termination of switching operation. To avoid undesired activation of OVP during normal operation,  $V_{CC}$  should be designed below 24.5 V (see Figure 25).

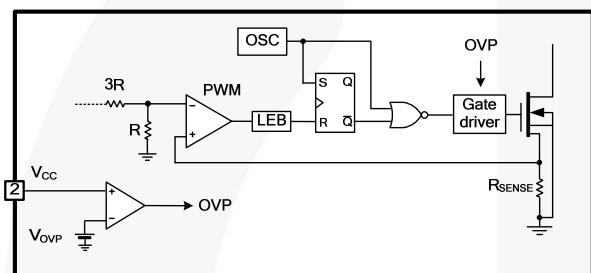


Figure 25. Over Voltage Protection Circuit

### 4.5 Feedback Open Loop Protection (FB\_OLP)

In the event of a feedback loop failure, especially a shorted lower-side resistor of the feedback pin; not only does  $V_{COMP}$  rise in a similar manner to the overload situation, but  $V_{FB}$  starts to drop to IC ground level. Although OLP and OVP also can protect the SMPS in this situation, FB\_OLP can reduce stress on SenseFET more. If there is no FB\_OLP, output voltage is much higher than rated voltage before OLP or OVP trigger. When  $V_{FB}$  drops below 0.5 V, FB\_OLP is activated, switching off. To avoid undesired activation during startup, this function is disabled during soft-start time.

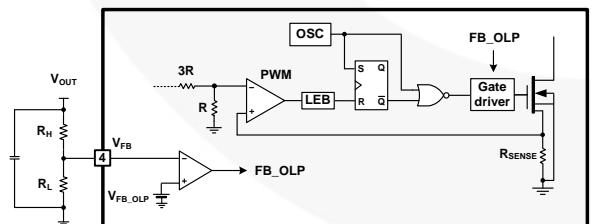


Figure 26. Feedback Open-loop Protection Circuit

### 5. Soft-Start

The internal soft-start circuit slowly increases the SenseFET current after it starts. The typical soft-start time is 10 ms, as shown in Figure 27, where progressive increments of the SenseFET current are allowed during startup. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is gradually increased to smoothly establish the required output voltage. Soft-start also helps to prevent transformer saturation and reduces stress on the secondary diode.

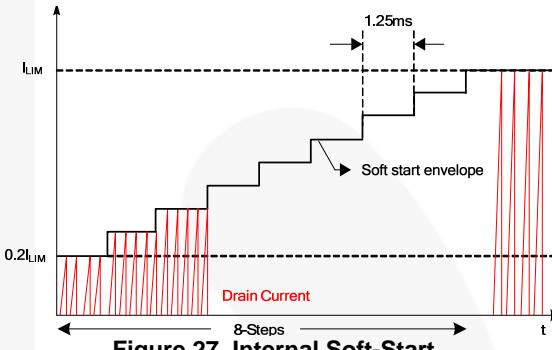


Figure 27. Internal Soft-Start

### 6. Burst Mode Operation

To minimize power dissipation in Standby Mode, the FSL306LRN enters Burst Mode. As the load decreases, the comp voltage ( $V_{COMP}$ ) decreases. As shown in Figure 28, the device automatically enters Burst Mode when the feedback voltage drops below  $V_{BURL}$ . At this point, switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes  $V_{COMP}$  to rise. Once it passes  $V_{BURH}$ , switching resumes.  $V_{COMP}$  then falls and the process repeats. Burst Mode alternately enables and disables switching of the SenseFET and reduces switching loss in Standby Mode.

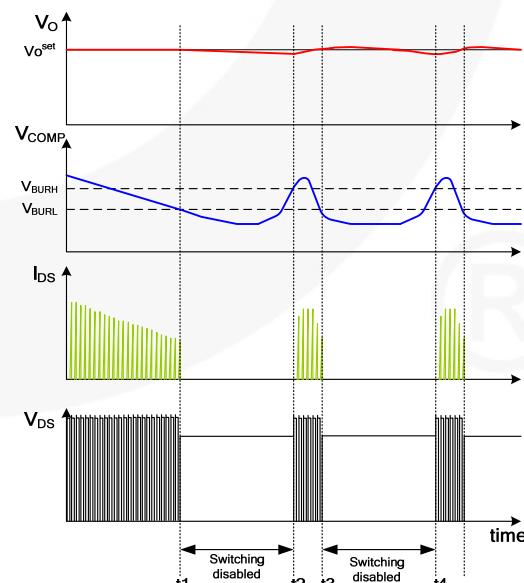


Figure 28. Burst Mode Operation

## 7. Green Mode Operation

As output load condition is reduced, the switching loss becomes the largest power loss factor. FSL306LRN uses the  $V_{COMP}$  pin voltage to monitor output load condition. As output load decreases,  $V_{COMP}$  decreases and switching frequency declines, as shown in Figure 29. Once  $V_{COMP}$  drops to under 1.9 V, switching frequency starts to decrease from 50 kHz. When  $V_{COMP}$  falls to 0.8 V, decreasing switching frequency is stopped at 22 kHz and maintains this frequency before Burst Mode operation.

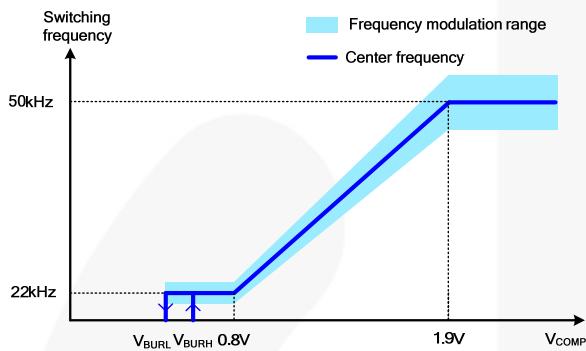


Figure 29. Green Mode Operation

## 8. Adjusting Current Limit

As shown in Figure 30, a combined  $46\text{ k}\Omega$  internal resistance ( $3R + R$ ) is connected to the inverting lead on the PWM comparator. An external resistance of  $R_X$  on the  $I_{LIMIT}$  pin forms a parallel resistance with the  $46\text{ k}\Omega$  when the internal diodes are biased by the main current source of  $50\text{ }\mu\text{A}$ . For example, FSL306LRN has a typical SenseFET peak current limit of  $0.45\text{ A}$ . Current limit can be adjusted to  $0.3\text{ A}$  by inserting  $R_X$  between the  $I_{LIMIT}$  pin and the ground. The value of the  $R_X$  can be estimated by the following equation:

$$0.45\text{ A} : 0.3\text{ A} = (46\text{ k}\Omega + R_X) : R_X \quad (1)$$

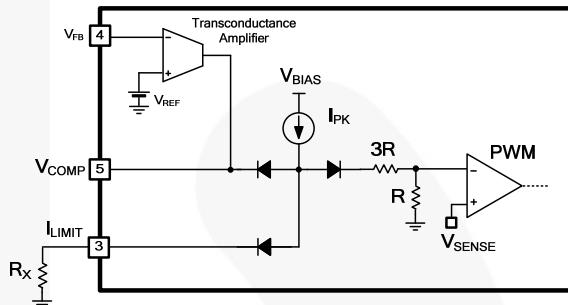


Figure 30. Current Limit Adjustment

## Typical Application Circuit

Application	Input Voltage	Rated Output	Rated Power
Auxiliary Power	85 ~ 300 V <sub>AC</sub>	12 V (150 mA)	2.05 W
Power Supply		5 V (50 mA)	

### Key Design Notes:

- Small current rating inductors (L1 & L2), an SMD-type resistor (R1), and an additional AC rectifying diode (D2) are placed for good EMI performance.
- External bias circuitry, a SMD-type resistor (R2), and a small-signal diode (D5) reduce power loss of the internal high-voltage regulator.

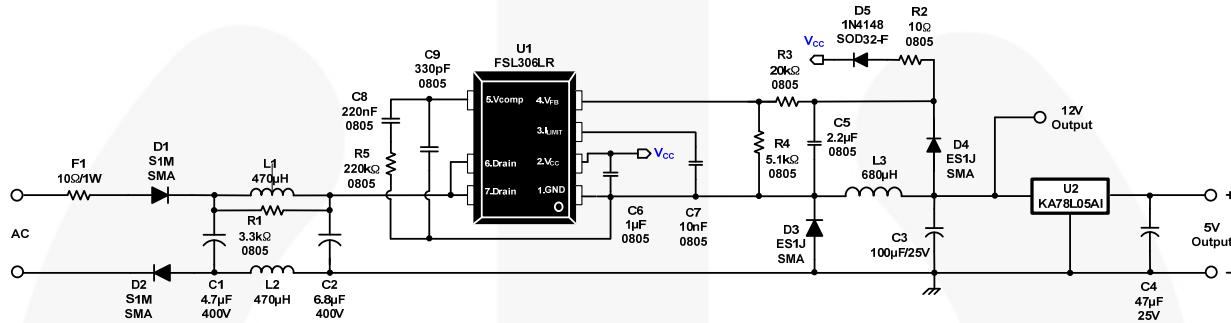


Figure 31. Schematic

Table 1. Bill of Materials

Part	Value	Note	Part	Value	Note
<b>Fuse</b>			<b>Diode</b>		
F1	10 W	1 W, Fusible Resistor	D1	S1M	1 A / 1000 V General-Purpose Rectifier
					Fairchild Semiconductor
<b>Resistor</b>			D2	S1M	1 A / 1000 V General-Purpose Rectifier
R1	3.3 kΩ	SMD 0805, 5%			Fairchild Semiconductor
R2	10 Ω	SMD 0805, 5%	D3	ES1J	1 A / 600 V Ultra-Fast Recovery Rectifier
R3	20 kΩ	SMD 0805, 1%			Fairchild Semiconductor
R4	5.1 kΩ	SMD 0805, 1%	D4	ES1J	1 A / 600 V Ultra-Fast Recovery Rectifier
R5	220 kΩ	SMD 0805, 5%			Fairchild Semiconductor
<b>Capacitor</b>			D5	1N4148	High Conductance Fast Diode
C1	4.7 μF / 400 V	Electrolytic			Fairchild Semiconductor
C2	6.8 μF / 400 V	Electrolytic	U1	FSL306LRN	0.1 A / 5 V Positive Voltage Regulator
C3	100 μF / 25 V	Electrolytic			Fairchild Semiconductor
<b>Inductor</b>			U2	KA78L05AIMTF	0.1 A / 5 V Positive Voltage Regulator
C4	47 μF / 25 V	Electrolytic			Fairchild Semiconductor
C5	2.2 μF	SMD 0805	L1	470 μH	SYNTON
C6	1 μF	SMD 0805	L2	470 μH	SYNTON
C7	10 nF	SMD 0805	L3	680 μH	PKS-0807-681K
C8	220 nF	SMD 0805			3L Electronic
C9	330 pF	SMD 0805			

## Physical Dimensions

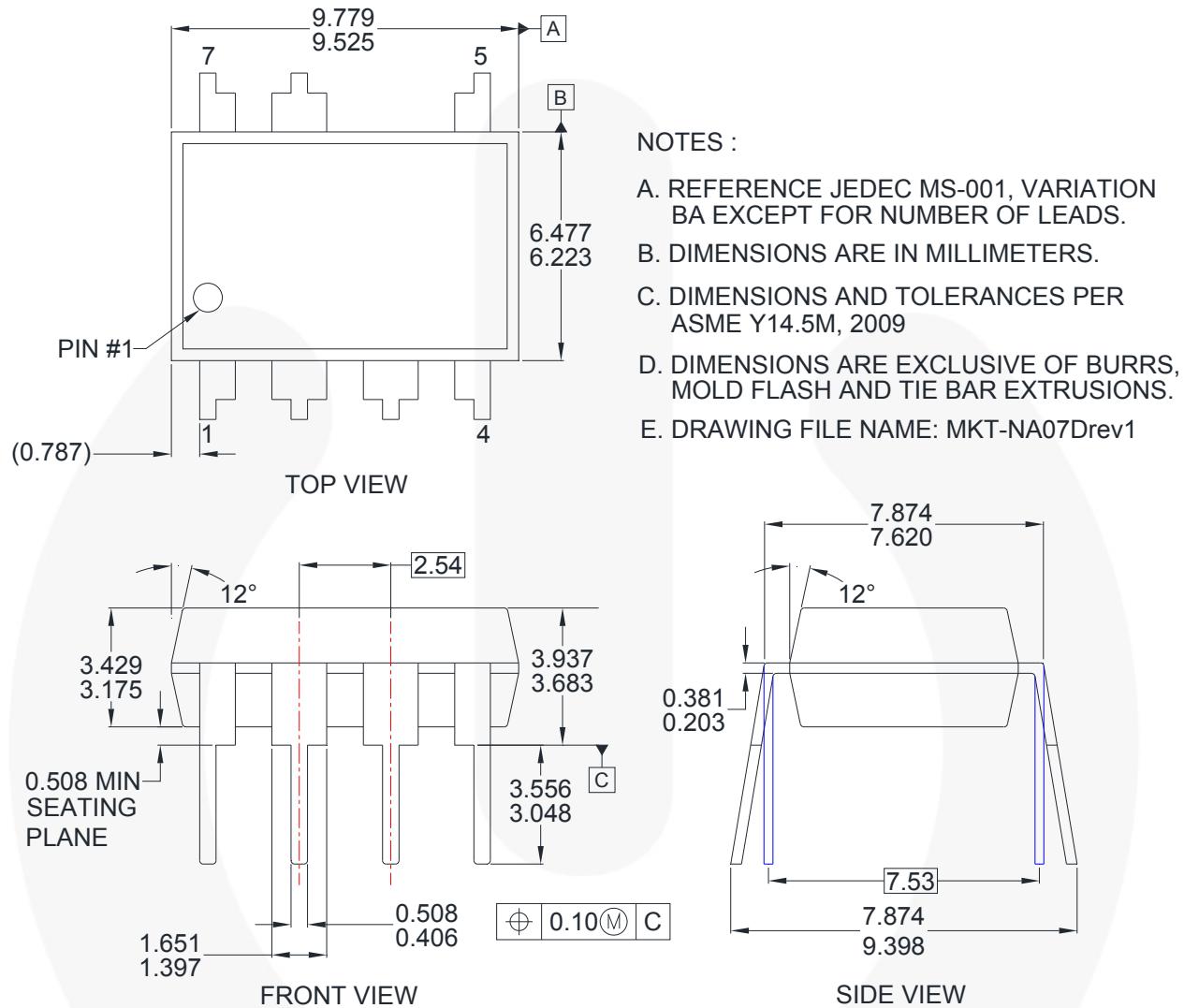


Figure 32. 7-Lead, Molded Dual Inline Package (MDIP), JEDEC MS-001, .300 inch Wide

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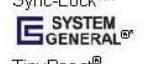
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