# ESD8351, SZESD8351

# ESD Protection Diodes

## Low Capacitance ESD Protection Diode for High Speed Data Line

The ESD8351 Series ESD protection diodes are designed to protect high speed data lines from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

### Features

- Low Capacitance (0.55 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (Level 4)
  ISO 10605
- Low ESD Clamping Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- USB 2.0
- eSATA

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating Junction Temperature Range | $T_J$ | −55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Lead Solder Temperature − Maximum (10 Seconds) | $T_L$ | 260 | °C |
| IEC 61000−4−2 Contact (ESD)<br>IEC 61000−4−2 Air (ESD)<br>ISO 10605 330 pF / 2 kΩ Contact | ESD<br>ESD<br>ESD | ±15<br>±15<br>±30 | kV<br>kV<br>kV |
| Maximum Peak Pulse Current 8/20 μs @ $T_A$ = 25°C | $I_{pp}$ | 5.0 | A |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

ON Semiconductor®

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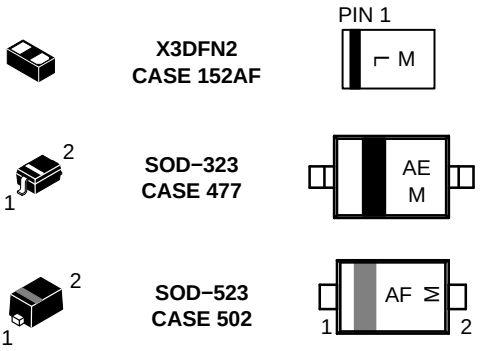
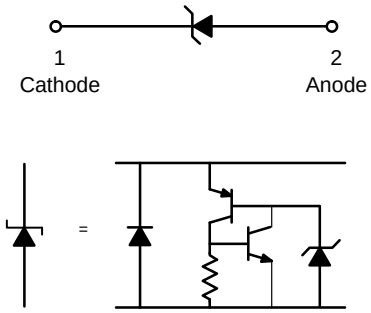
**MARKING DIAGRAMS**




X, XX = Specific Device Code
M = Date Code

**PIN CONFIGURATION AND SCHEMATIC**



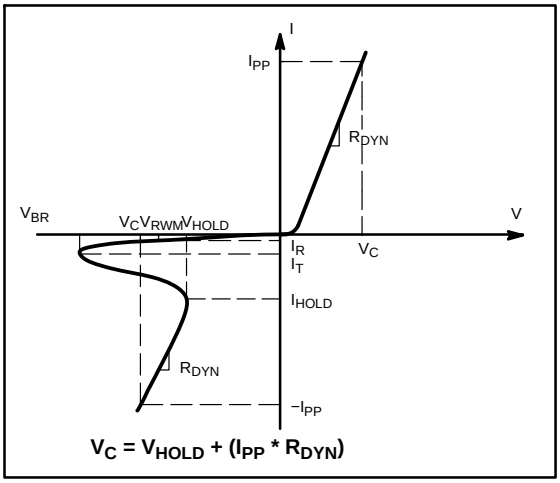

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

## ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $V_{RWM}$ | Working Peak Voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |
| $V_{HOLD}$ | Holding Reverse Voltage |
| $I_{HOLD}$ | Holding Reverse Current |
| $R_{DYN}$ | Dynamic Resistance |
| $I_{PP}$ | Maximum Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$<br>$V_C = V_{HOLD} + (I_{PP} * R_{DYN})$ |




## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Reverse Working Voltage | $V_{RWM}$ | I/O Pin to GND | | | 3.3 | V |
| Breakdown Voltage | $V_{BR}$ | $I_T$ = 1 mA, I/O Pin to GND | 5.5 | 7.0 | 7.8 | V |
| Reverse Leakage Current | $I_R$ | $V_{RWM}$ = 3.3 V, I/O Pin to GND | | | 500 | nA |
| Holding Reverse Voltage | $V_{HOLD}$ | I/O Pin to GND | | 1.15 | | V |
| Holding Reverse Current | $I_{HOLD}$ | I/O Pin to GND | | 20 | | mA |
| Clamping Voltage TLP (Note 2) See Figures 1 through 11 | $V_C$ | $I_{PP}$ = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air) | | 6.5 | | V |
| | | $I_{PP}$ = 16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±15 kV Air) | | 11.2 | | |
| Clamping Voltage (Note 3) | $V_C$ | $I_{PP}$ = 5 A } $t_p$ = 8 x 20 μs | | 8.2 | | V |
| Dynamic Resistance | $R_{DYN}$ | Pin1 to Pin2<br>Pin2 to Pin1 | | 0.62<br>0.59 | | Ω |
| Junction Capacitance | $C_J$ | $V_R$ = 0 V, f = 1 Mhz<br>$V_R$ = 0 V, f = 2.5 Ghz | | 0.37<br>0.35 | 0.55<br>0.45 | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see Figures 8 and 9 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 4 ns, averaging window; $t_1$ = 30 ns to $t_2$ = 60 ns.
3. Non−repetitive current pulse at $T_A$ = 20°C, per IEC 61000−4−5 waveform.

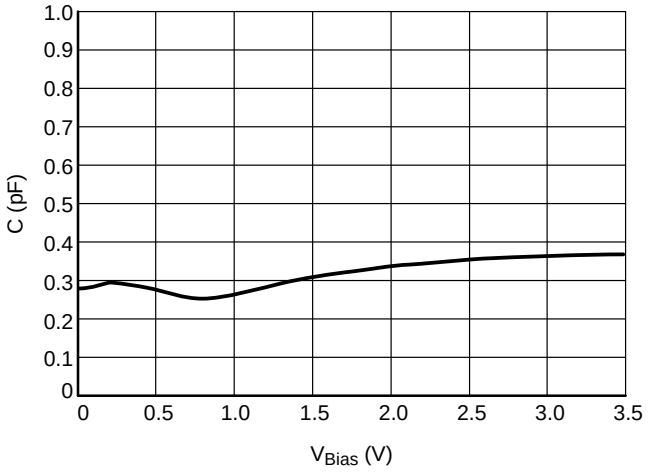



**Figure 1. CV Characteristics**

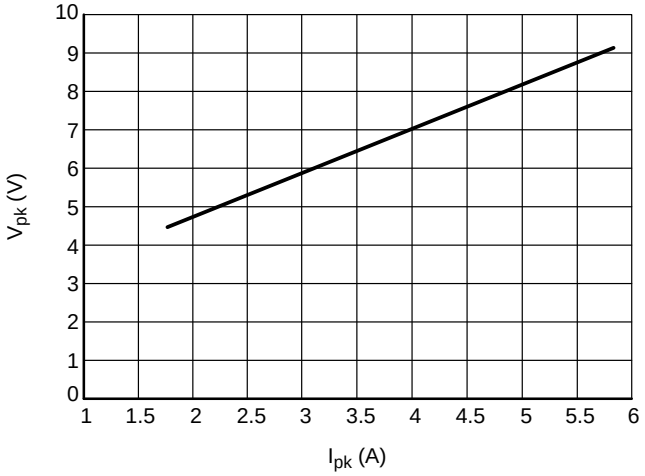



**Figure 2. Clamping Voltage vs Peak Pulse Current ( $t_p$ = 8/20 μs)**

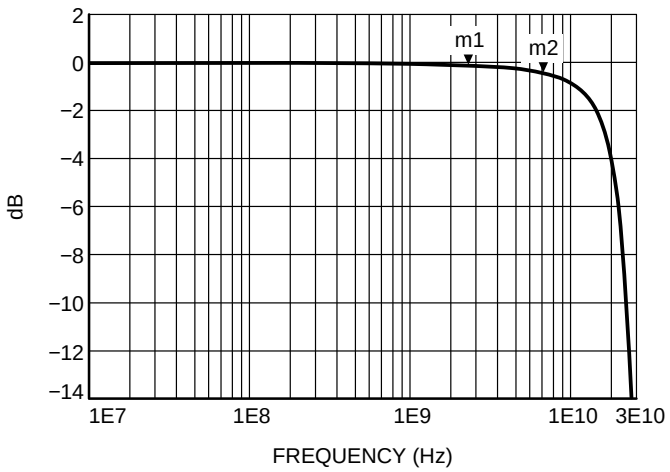



**Figure 3. RF Insertion Loss**

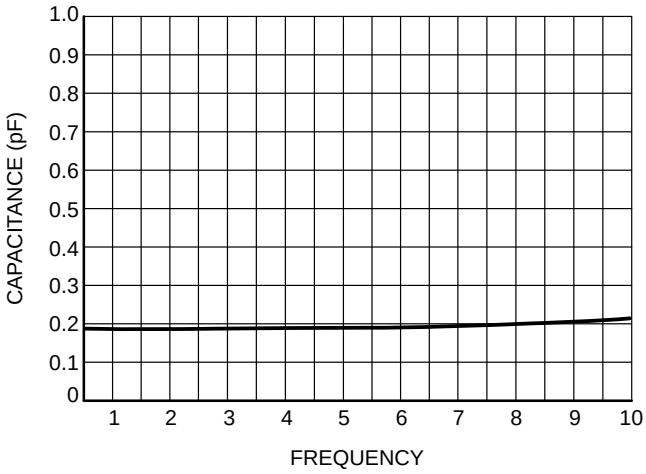



**Figure 4. Capacitance over Frequency**

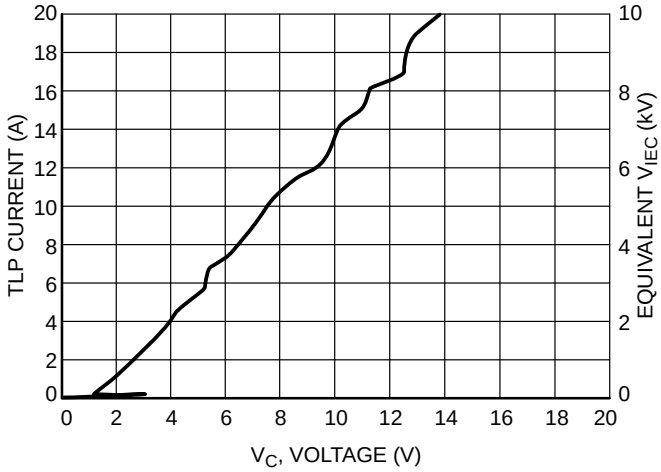



**Figure 5. Positive TLP I−V Curve**

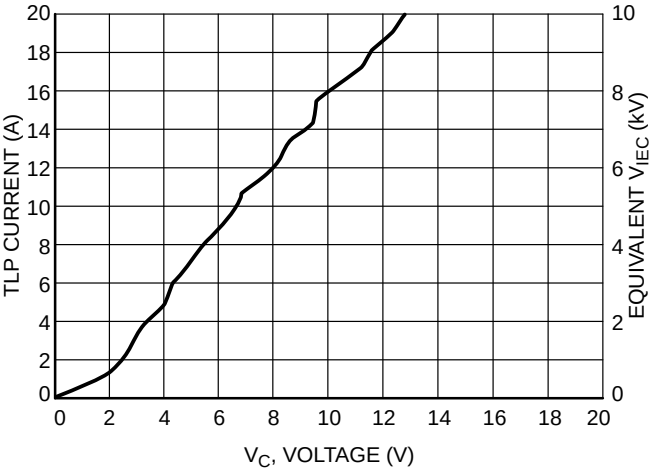



**Figure 6. Negative TLP I−V Curve**

### Latch−Up Considerations

ON Semiconductor's 8000 series of ESD protection devices utilize a snap−back, SCR type structure. By using this technology, the potential for a latch−up condition was taken into account by performing load line analysis of common high speed serial interfaces. Example load lines for latch−up free applications and applications with the potential for latch−up are shown below with a generic IV characteristic of a snapback, SCR type structured device overlaid on each. In the latch−up free load line case, the IV characteristic of the snapback protection device intersects the load−line in one unique point ($V_{OP}$, $I_{OP}$). This is the only stable operating point of the circuit and the system is therefore latch−up free. In the non−latch up free load line case, the IV characteristic of the snapback protection device intersects the load−line in two points ($V_{OPA}$, $I_{OPA}$) and ($V_{OPB}$, $I_{OPB}$). Therefore in this case, the potential for latch−up exists if the system settles at ($V_{OPB}$, $I_{OPB}$) after a transient. Because of this, ESD8351 Series should not be used for HDMI applications – ESD8104 or ESD8040 have been designed to be acceptable for HDMI applications without latch−up. Please refer to Application Note AND9116/D for a more in−depth explanation of latch−up considerations using ESD8000 series devices.

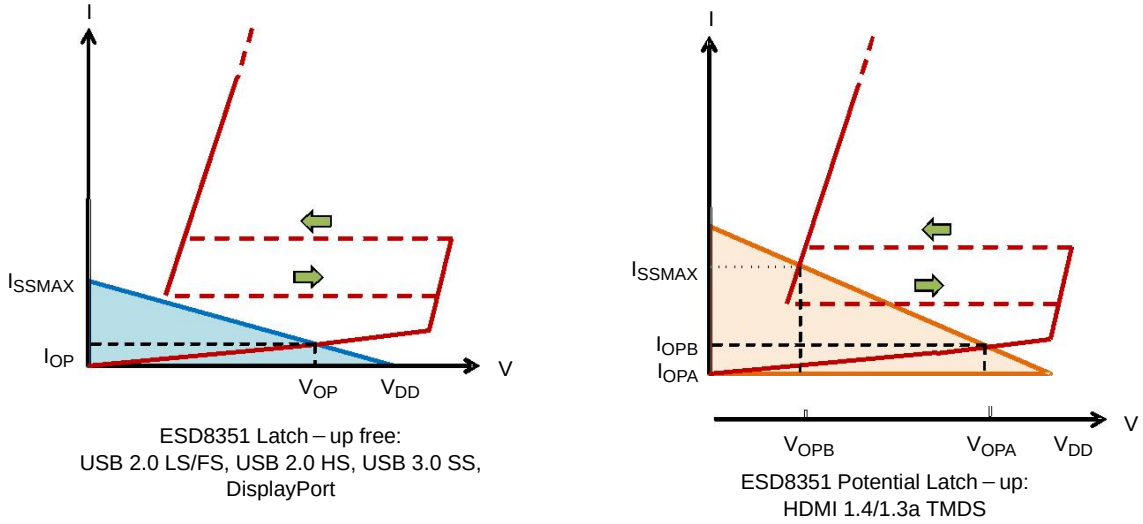



**Figure 7. Example Load Lines for Latch−up Free Applications and Applications with the Potential for Latch−up**

**Table 1. SUMMARY OF SCR REQUIREMENTS FOR LATCH−UP FREE APPLICATIONS**

| Application | VBR (min) (V) | IH (min) (mA) | VH (min) (V) | ON Semiconductor ESD8000 Series Recommended PN |
|---|---|---|---|---|
| HDMI 1.4/1.3a TMDS | 3.465 | 54.78 | 1.0 | ESD8104, ESD8040 |
| USB 2.0 LS/FS | 3.301 | 1.76 | 1.0 | ESD8004, ESD8351 |
| USB 2.0 HS | 0.482 | N/A | 1.0 | ESD8004, ESD8351 |
| USB 3.0 SS | 2.800 | N/A | 1.0 | ESD8004, ESD8006, ESD8351 |
| DisplayPort | 3.600 | 25.00 | 1.0 | ESD8004, ESD8006, ESD8351 |

**IEC 61000−4−2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

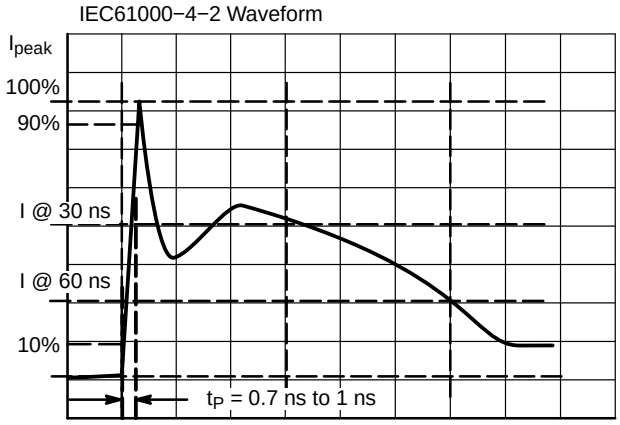



**Figure 8. IEC61000−4−2 Spec**

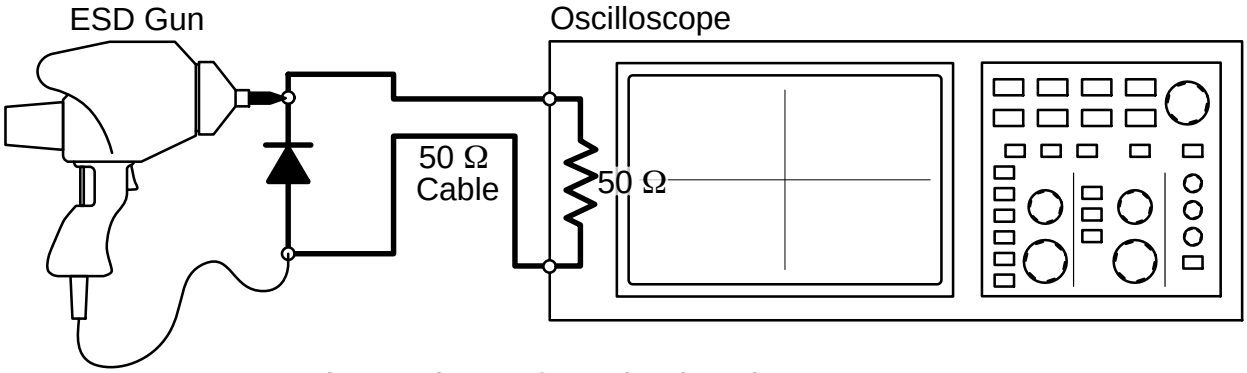



**Figure 9. Diagram of ESD Clamping Voltage Test Setup**

**The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.**

**ESD Voltage Clamping**

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 10. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 11 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

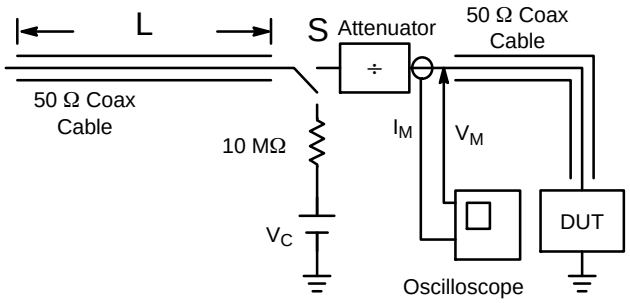



**Figure 10. Simplified Schematic of a Typical TLP System**

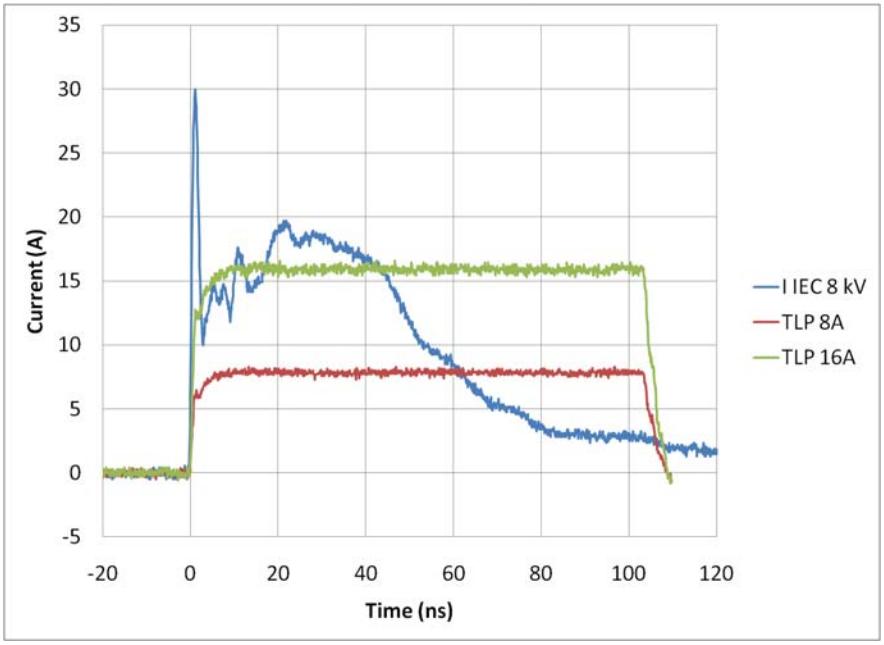



**Figure 11. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms**

## ORDERING INFORMATION

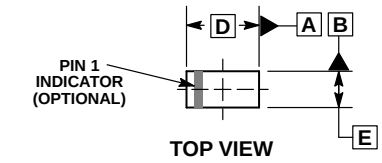
| Device | Package | Shipping† |
|---|---|---|
| ESD8351HT1G,<br>SZESD8351HT1G* | SOD−323<br>(Pb−Free) | 3000 / Tape & Reel |
| ESD8351XV2T1G,<br>SZESD8351XV2T1G* | SOD−523<br>(Pb−Free) | 3000 / Tape & Reel |
| ESD8351XV2T5G,<br>SZESD8351XV2T5G* | | 8000 / Tape & Reel |
| ESD8351MUT5G | X3DFN2<br>(Pb−Free) | 10000 / Tape & Reel |
| SZESD8351MUT5G* | X3DFN2<br>(Pb−Free) | 15000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

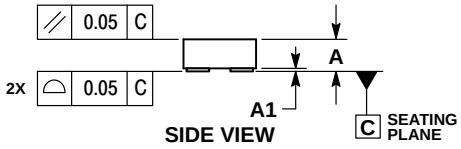
*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

## PACKAGE DIMENSIONS

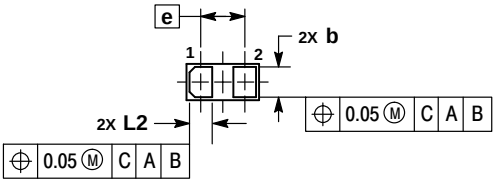
**X3DFN2, 0.62x0.32, 0.355P, (0201)**
CASE 152AF
ISSUE A




TOP VIEW




SIDE VIEW

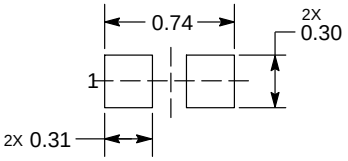



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.25 | 0.33 |
| A1 | −−− | 0.05 |
| b | 0.22 | 0.28 |
| D | 0.58 | 0.66 |
| E | 0.28 | 0.36 |
| e | 0.355 BSC | |
| L2 | 0.17 | 0.23 |

**RECOMMENDED MOUNTING FOOTPRINT***



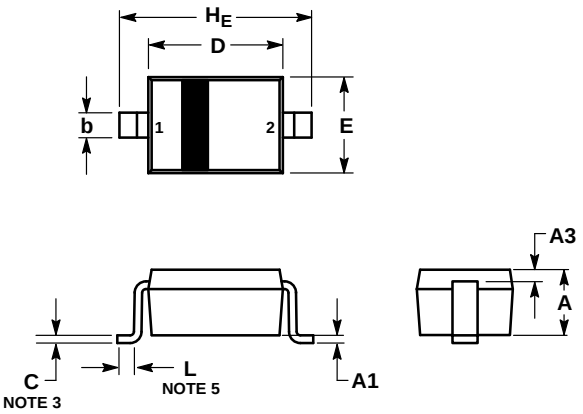

DIMENSIONS: MILLIMETERS

See Application Note AND8398/D for more mounting details

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

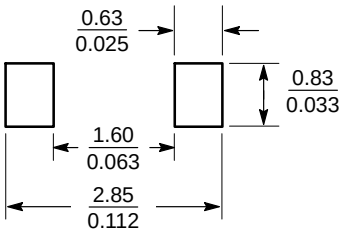
**SOD−323**
CASE 477−02
ISSUE H




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS SPECIFIED PER L/F DRAWING WITH SOLDER PLATING.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DIMENSION L IS MEASURED FROM END OF RADIUS.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.040 |
| A1 | 0.00 | 0.05 | 0.10 | 0.000 | 0.002 | 0.004 |
| A3 | | 0.15 REF | | | 0.006 REF | |
| b | 0.25 | 0.32 | 0.4 | 0.010 | 0.012 | 0.016 |
| C | 0.089 | 0.12 | 0.177 | 0.003 | 0.005 | 0.007 |
| D | 1.60 | 1.70 | 1.80 | 0.062 | 0.066 | 0.070 |
| E | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| L | 0.08 | | | 0.003 | | |
| $H_E$ | 2.30 | 2.50 | 2.70 | 0.090 | 0.098 | 0.105 |

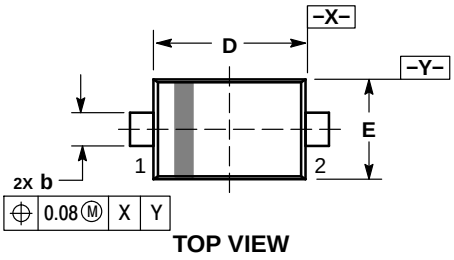
## SOLDERING FOOTPRINT*



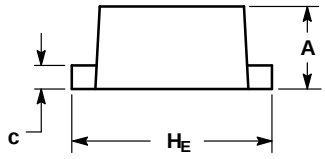

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

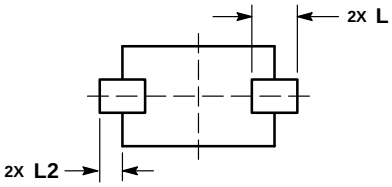
**SOD−523**
CASE 502
ISSUE E




**TOP VIEW**




**SIDE VIEW**

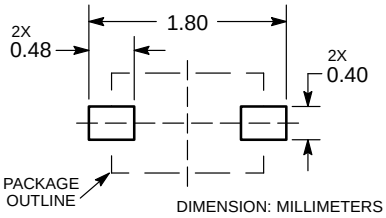



**BOTTOM VIEW**

NOTES:
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
7. CONTROLLING DIMENSION: MILLIMETERS.
8. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
9. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.50 | 0.60 | 0.70 |
| b | 0.25 | 0.30 | 0.35 |
| c | 0.07 | 0.14 | 0.20 |
| D | 1.10 | 1.20 | 1.30 |
| E | 0.70 | 0.80 | 0.90 |
| $H_E$ | 1.50 | 1.60 | 1.70 |
| L | 0.30 REF | | |
| L2 | 0.15 | 0.20 | 0.25 |

**RECOMMENDED SOLDERING FOOTPRINT***




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



**PUBLICATION ORDERING INFORMATION**

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**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
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